Document Title

32K x8 bit 2.7~5.5V Low Power CMOS slow SRAM

Revision History

Revision No	History	Draft Date	Remark
00	Revision History Insert Revised - Datasheet format change - PDIP package type insert - Pin configuration change	Jul.07.2000	Final
01	Marking Information Add Revised - AC Test Condition Add : 5pF Test Load - tCLZ Value Change : 15ns - > 10ns - tOLZ Value Change : 10ns - > 5ns	Dec.04.2000	Final
02	Changed Logo - HYUNDAI -> hynix	Apr.30.2001	Final

DESCRIPTION

The GM76C256CW is a high-speed, low power and 32,786 X 8-bits CMOS Static Random Access Memory fabricated using Hynix's high performance CMOS process technology. It is suitable for use in low voltage operation and battery back-up application. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt.

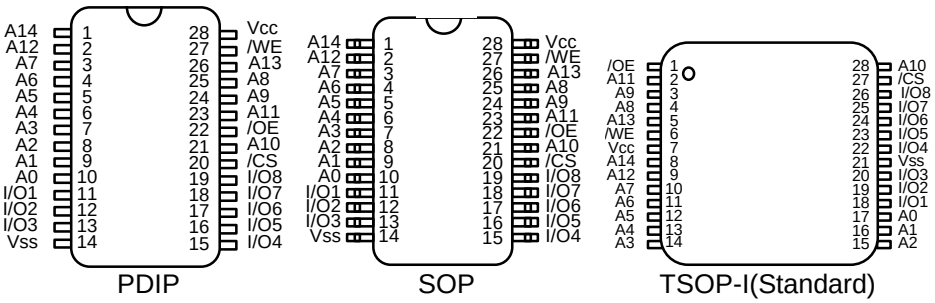
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
  - 2.0V(min.) data retention
- Standard pin configuration
  - 28 pin 600mil PDIP
  - 28 pin 330mil SOP
  - 28 pin 8x13.4 mm TSOP-I (Standard)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (°C)
				L	LL	
GM76C256CW	5.0	55/70	10	40	20	0~70(Normal)
	3.0	120/150	2	20	10	

Note 1. Current value is max.

PIN CONNECTION

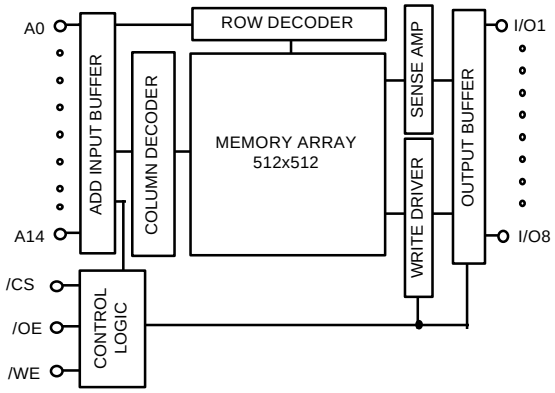


PDIP SOP TSOP-I(Standard)

PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
GM76C256CL-W	55/70	L-part	0 to 70°C	PDIP
GM76C256CLL-W	55/70	LL-part	0 to 70°C	PDIP
GM76C256CLFW-W	55/70	L-part	0 to 70°C	SOP
GM76C256CLLFW-W	55/70	LL-part	0 to 70°C	SOP
GM76C256CLT-W	55/70	L-part	0 to 70°C	TSOP-I Standard
GM76C256CLLT-W	55/70	LL-part	0 to 70°C	TSOP-I Standard

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit
Vcc, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.3 to 7.0	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 •10	°C•sec

Note

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Vcc = 5V			Vcc = 2.7 ~ 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Vcc	Power Supply Voltage	4.5	5.0	5.5	2.7	3.0	5.5	V
Vss	Ground	0	0	0	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.3	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.8	-0.3(1)	-	0.4	V

Note

1. V_{IL} = -3.0V for pulse width less than 50ns

TRUTH TABLE

/CS	/WE	/OE	Mode	I/O Operation
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note

1. H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

Vcc = 3V ±10%,5V ±10%, T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	Test Condition		Vcc = 3V¡ 1 10%			Vcc = 5V¡ 1 10%			Unit
				Min	Typ	Max	Min	Typ	Max	
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc		-1	-	1	-1	-	1	uA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	-1	-	1	uA
Icc	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	0.6	2	-	7	10	mA
I_{CC1}	Average Operating Current	/CS = V_{IL}, $I_{I/O}$ = 0mA, Min. Duty Cycle = 100%, V_{IN} = V_{IH} or V_{IL}		-	-	30	-	-	70	mA
		/CS = V_{IL}, $I_{I/O}$ =0mA, Cycle = 1us, V_{IN} = V_{IH} or V_{IL}		-	-	5	-	-	10	mA
I_{SB}	TTL Standby Current (TTL Inputs)	/CS= V_{IH}, V_{IN} = V_{IH} or V_{IL}		-	-	0.3	-	-	1	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	/CS≥Vcc-0.2V, V_{IN}≥Vcc-0.2V or V_{IN}≤Vss+0.2V	L			20	-	-	40	uA
			LL			10	-	-	20	uA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA				0.4	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA		2.2			2.4	-	-	V

Note : Typical values are at Vcc =3.0V/5.0V, T_A = 25°C

AC CHARACTERISTICS(I)

Vcc = 3V ±10%, T_A = 0°C to 70°C (Normal) unless otherwise specified.

#	Symbol	Parameter	-55		-70		Unit
			Min.	Max.	Min.	Max.	
	READ CYCLE						
1	tRC	Read Cycle Time	120	-	150	-	ns
2	tAA	Address Access Time	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	55	-	60	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	40	0	50	ns
8	tOHZ	Out Disable to Output in High Z	0	40	0	50	ns
9	tOH	Output Hold from Address Change	10	-	10	-	ns
	WRITE CYCLE						
10	tWC	Write Cycle Time	120	-	150	-	ns
11	tCW	Chip Selection to End of Write	100	-	120	-	ns
12	tAW	Address Valid to End of Write	100	-	120	-	ns
13	tAS	Address Set-up Time	0	-	0	-	ns
14	tWP	Write Pulse Width	65	-	70	-	ns
15	tWR	Write Recovery Time	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	40	0	50	ns
17	tDW	Data to Write Time Overlap	40	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	ns
19	tOW	Output Active from End of Write	10	-	15	-	ns

AC CHARACTERISTICS(II)

Vcc = 5V ±10%, T_A = 0°C to 70°C (Normal) unless otherwise specified.

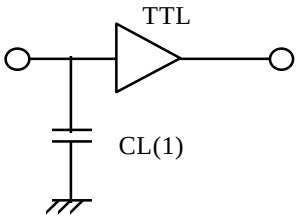
#	Symbol	Parameter	-55		-70		Unit
			Min.	Max.	Min.	Max.	
	READ CYCLE						
1	tRC	Read Cycle Time	55	-	70	-	ns
2	tAA	Address Access Time	-	55	-	70	ns
3	tACS	Chip Select Access Time	-	55	-	70	ns
4	tOE	Output Enable to Output Valid	-	30	-	35	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	20	0	25	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	ns
9	tOH	Output Hold from Address Change	5	-	10	-	ns
	WRITE CYCLE						
10	tWC	Write Cycle Time	55	-	70	-	ns
11	tCW	Chip Selection to End of Write	50	-	65	-	ns
12	tAW	Address Valid to End of Write	50	-	60	-	ns
13	tAS	Address Set-up Time	0	-	0	-	ns
14	tWP	Write Pulse Width	45	-	50	-	ns
15	tWR	Write Recovery Time	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C (Normal) unless otherwise specified.

Parameter		Value
Input Pulse Level	5V	0.6V to 2.4V
	3V	0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ,tOLZ,tCHZ,tOHZ,tWHZ,tOW	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

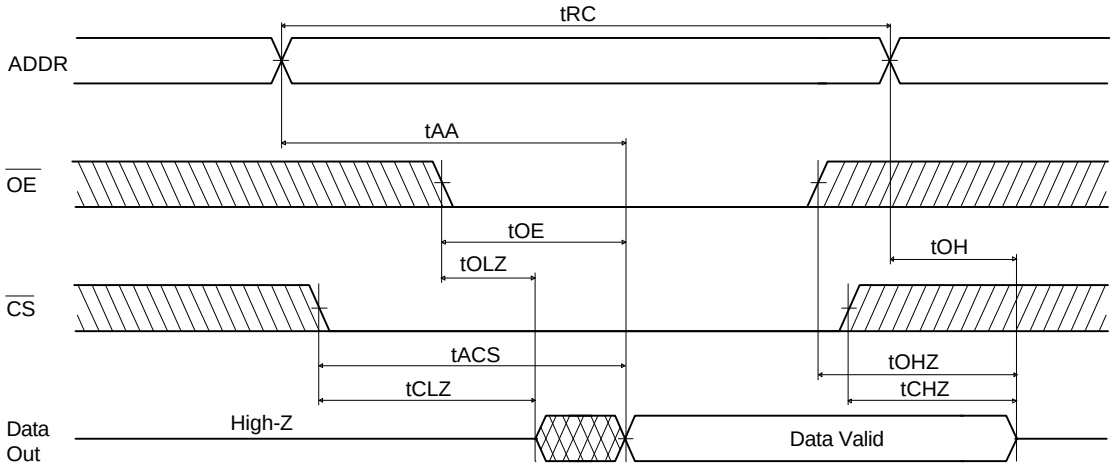
T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

TIMING DIAGRAM

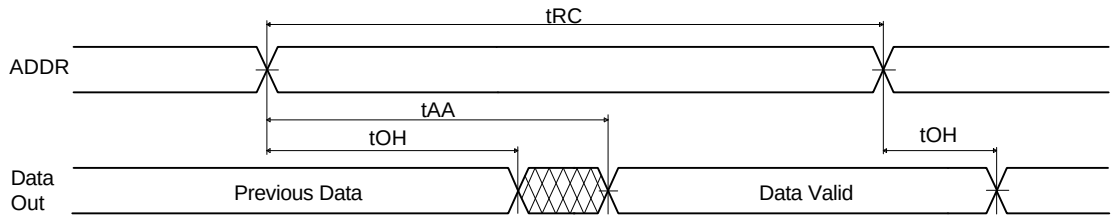
READ CYCLE 1



Note(READ CYCLE):

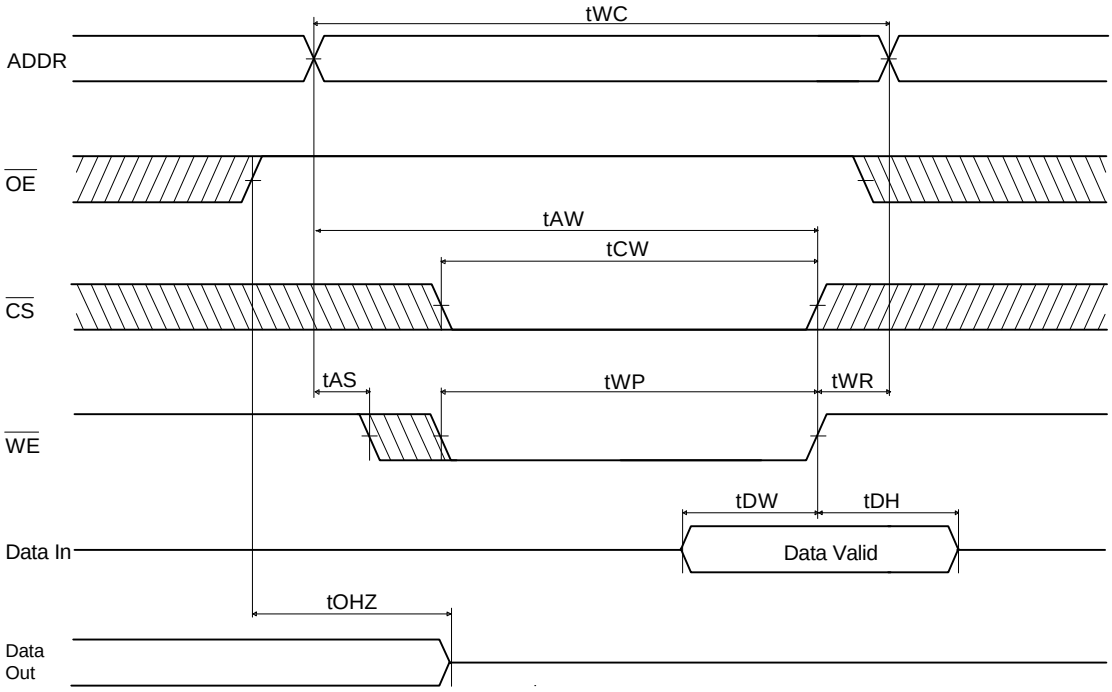
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and arenot referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

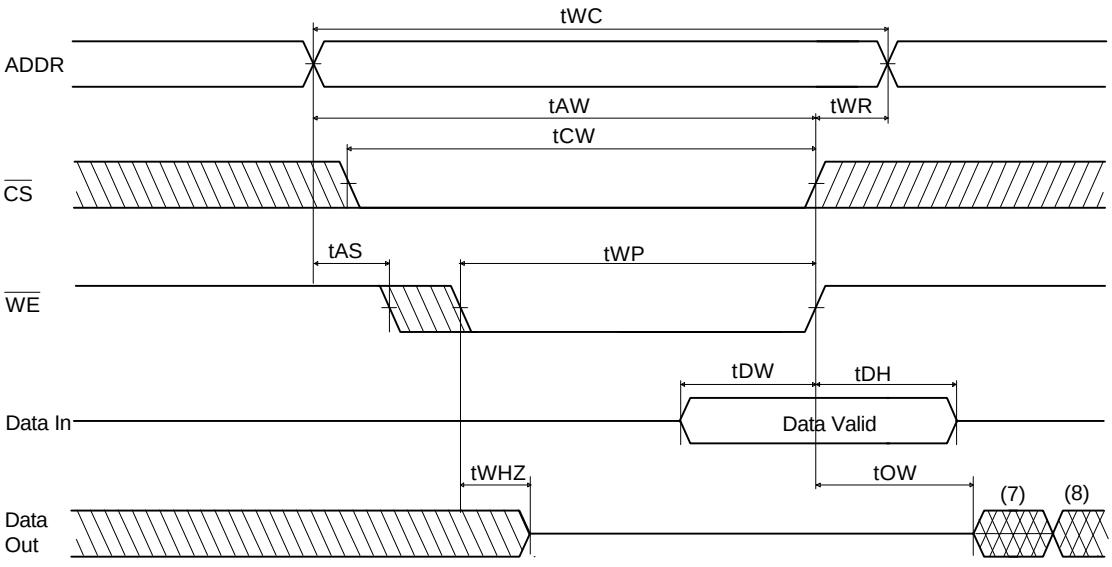


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS= V_{IL}.
3. /OE =V_{IL}.

WRITE CYCLE 1(/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):
1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of the latest written data in this write cycle.
8. DOUT is the read data of the new address.

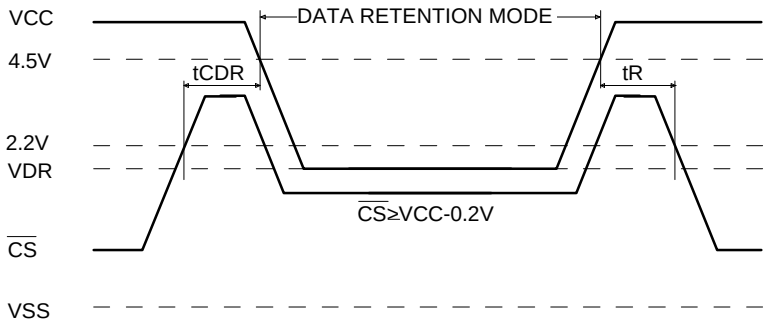
DATA RETENTION CHARACTERISTIC

Ta=0°C to 70°C (Normal)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
VDR	Vcc for Data Retention	CS≥Vcc-0.2V, VIN≥Vcc-0.2V or VIN≤Vss+0.2V		2.0	-	-	V
ICCDR	Data Retention Current	Vcc=3.0V, /CS≥Vcc-0.2V, VIN≥Vcc-0.2V or VIN≤Vss+0.2V	L	-	1	50	uA
			LL	-	0.5	10	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			tRC(2)	-	-	ns

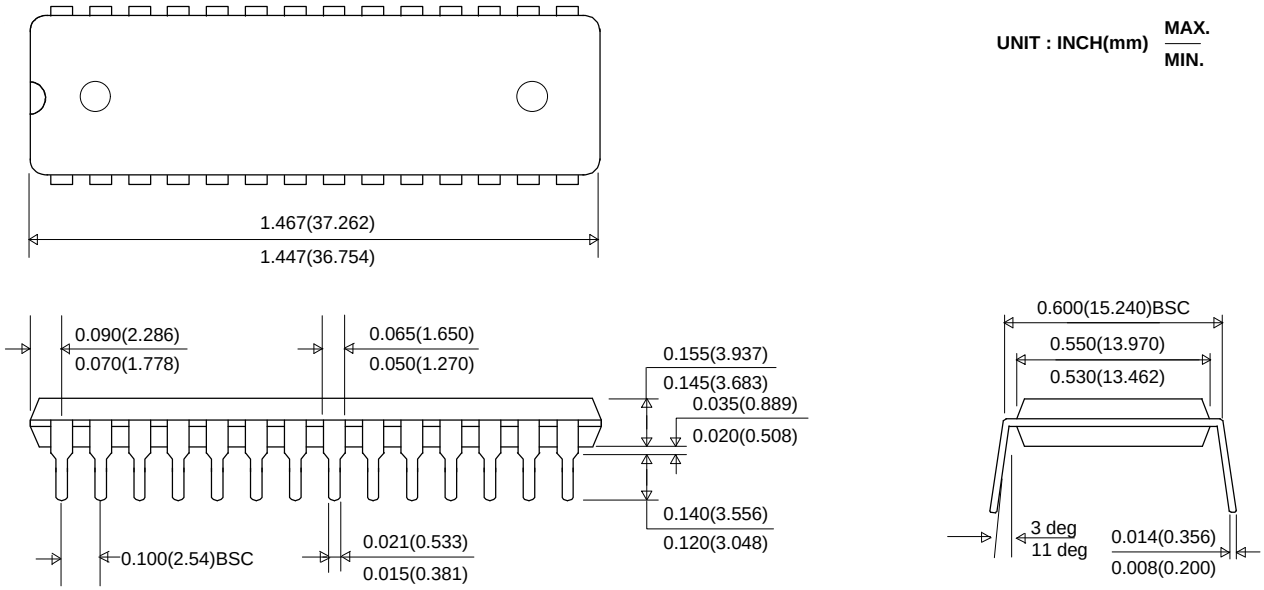
Notes
1. Typical values are under the condition of TA = 25°C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

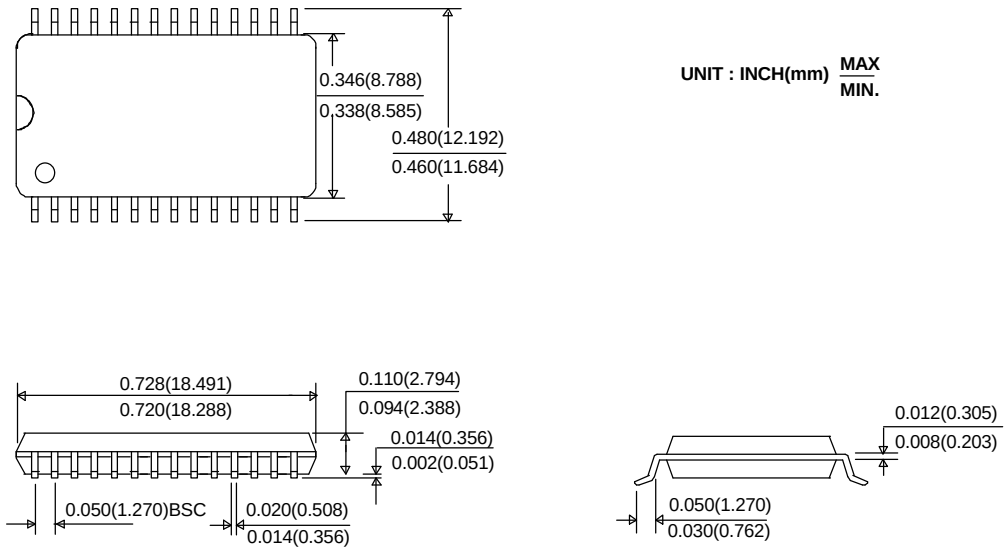


PACKAGE INFORMATION

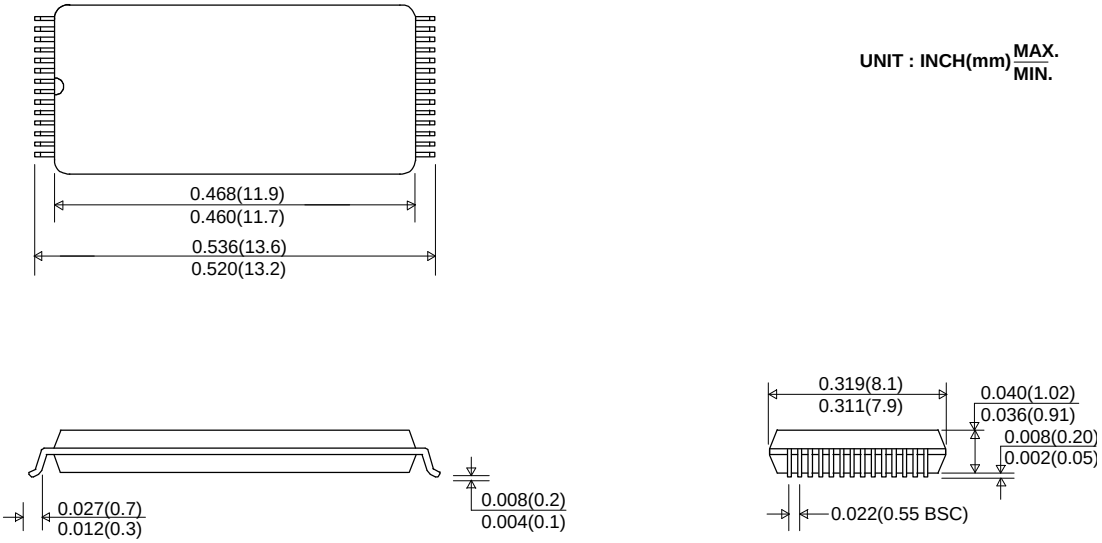
28pin 600mil Dual In-Line Package(Blank)



28pin 330mil Small Outline Package(FW)



28pin 8x13.4mm Thin Small Outline Package Standard(T)



MARKING INFORMATION

Package	Marking Example
PDIP	HYUNDAI GM76C256Ccc-ssW yywwKOREA
SOP	HYUNDAI GM76C256CccFWssW yywwKOREA
TSOP-I	HYUNDAI GM76C256CccTssW yywwKOREA

Index

- **HYUNDAI** : Hynix Logo
- **KOREA** : Origin Country
- **GM76C256C** : Part Name
- **cc** : Power Consumption
  - L : Low Power
  - LL : Low Low Power
- **Blank / FW / T** : Package Type
  - Blank : DIP
  - FW : SOP
  - T : TSOP-I
- **ss** : Speed
  - 55 : 55ns
  - 70 : 70ns
- **W** : Wide Voltage
- **yy** : Year (ex : 00 = year 2000, 01 = year 2001)
- **ww** : Work Week (ex : 12 = ww12)

Note

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item