DALLAS SEMICONDUCTOR CORP 50E D 2614130 0004656 5 DAL

DALLAS SEMICONDUCTOR

DS1225D/E
64K Nonvolatile SRAM

T-46-23-37

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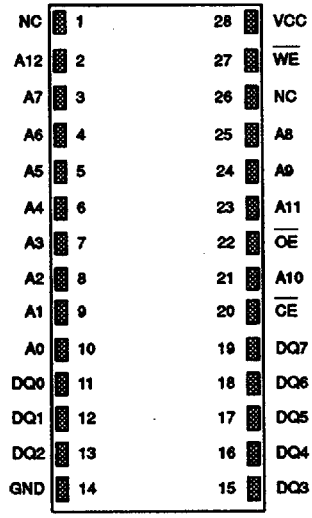
FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, or 120 ns read access times
- Read cycle time equals write cycle time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-Pin Encapsulated Package
(740 Mil Flush Bottom)

PIN DESCRIPTION

A0 - A12	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

NOTE: Pins 1 & 26 missing by design

DESCRIPTION

The DS1225D and DS1225E are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225D/E also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225D/E executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225D/E are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225E provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1225D provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225D/E constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1225D and 4.75 volts for the DS1225E.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225D Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
DS1225E Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10% for DS1225D)
(0°C to 70°C; V_{CC}=5V ± 5% for DS1225E)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE}$>V_{IH} <V_{CC}	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=100ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=100ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1225D)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1225E)	V_{TP}	4.25	4.37	4.5	V	

DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground.

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V + 10% for DS1225D)
(0°C to 70°C; V_{CC}=5.0V ± 5% for DS1225E)

		DS1225D/E-70		DS1225D/E-85		DS1225D/E-100		DS1225D/E-120			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70		85		100		120		ns	
Access Time	t_{ACC}		70		85		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		25		25		25	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		120		ns	
Write Pulse Width	t_{WP}	55		65		75		90		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		25		25		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		50		ns	4
Data Hold Time	t_{DH}	10		10		10		10		ns	4

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

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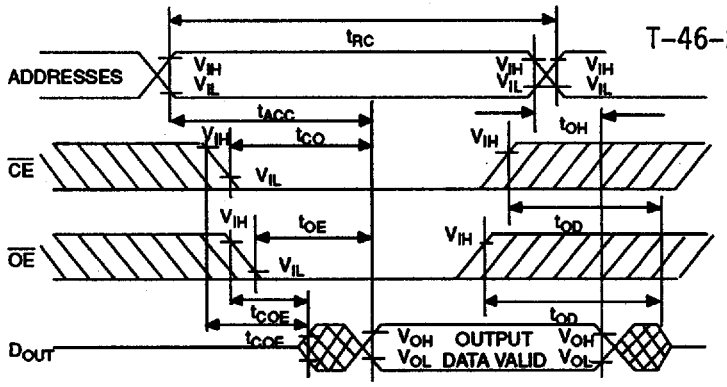
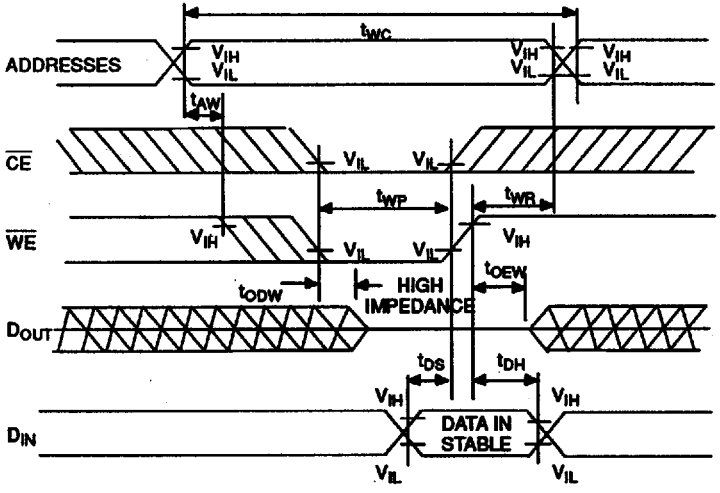
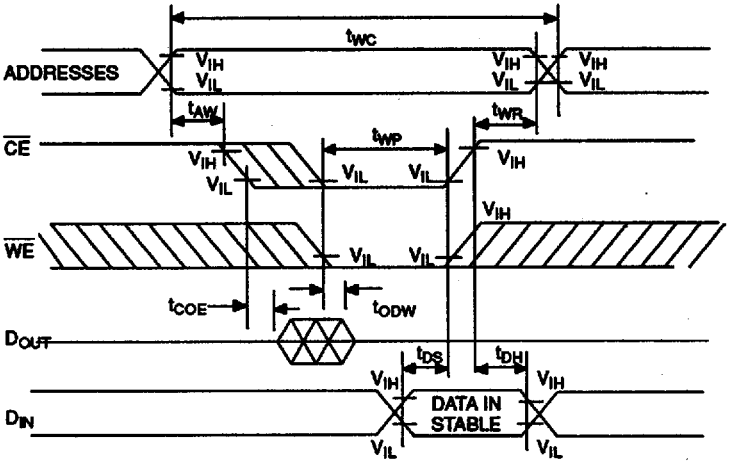
READ CYCLE (1)



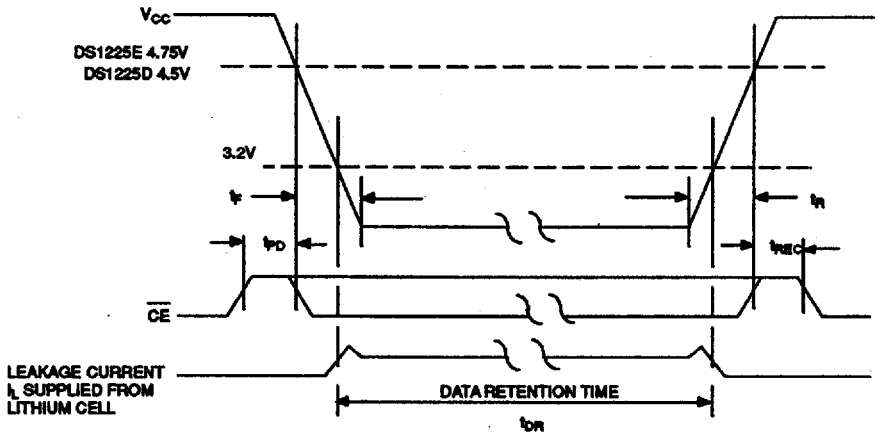
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1225E
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1225D
t_R	V_{CC} Slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		µs	DS1225E
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	DS1225D
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

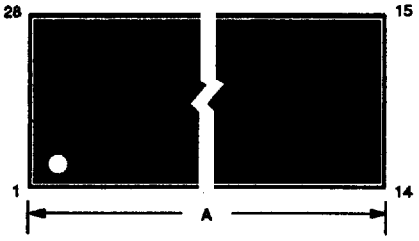
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

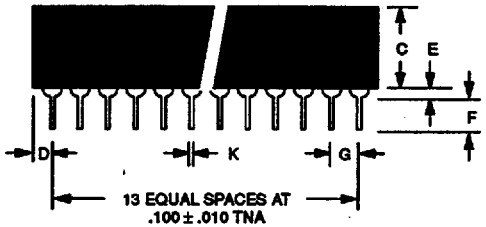
WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

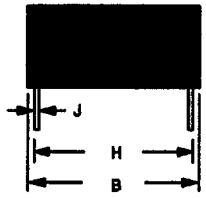
NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225D/E is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

DS1225D/E NONVOLATILE SRAM 28-PIN 740 MIL MODULE







PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.520 38.61	1.540 39.12
B IN. MM	0.695 17.65	0.720 18.29
C IN. MM	0.350 8.89	0.375 9.53
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53