

## QUARTZ CRYSTAL OSCILLATOR

**■ GENERAL DESCRIPTION**

The NJU6338 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

This series are classed into three groups A to D, H to L and Q to T according to their oscillation frequency range mentioned in the line-up table.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors(Cg, Cd), therefore, it requires no external component except quartz crystal.

The 3-stage divider generates  $f_o$ ,  $f_o/2$ ,  $f_o/4$  and  $f_o/8$  and only one frequency selected by internal circuits is output.

The 3-state output buffer is TTL compatible and capable of 10 TTL driving.

The difference between NJU6338 and NJU6331 series is only pin configuration.

**■ FEATURES**

- Operating Voltage. -- 4.0~6.0V
- Maximum Oscillation Frequency (See Line-Up Table)
- Low Operating Current
- High Fan-out -- TTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)
  - Only one frequency out of  $f_o$ ,  $f_o/2$ ,  $f_o/4$  and  $f_o/8$  output
- Oscillation Capacitors Cg and Cd on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP / EMP 8
- C-MOS Technology

**■ LINE-UP TABLE**

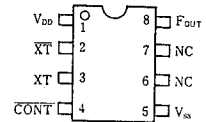
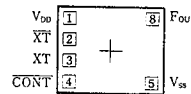
Type No.	Recommended Osc. Freq.	Output Freq.	Cg, Cd
NJU6338A 6338B 6338C 6338D	From 20 to 35MHz	$f_o$ $f_o/2$ $f_o/4$ $f_o/8$	28pF
NJU6338H 6338J 6338K 6338L	From 30 to 50MHz	$f_o$ $f_o/2$ $f_o/4$ $f_o/8$	20pF
NJU6338Q 6338R 6338S 6338T	From 45 to 75MHz	$f_o$ $f_o/2$ $f_o/4$ $f_o/8$	17pF

**■ PACKAGE OUTLINE**


NJU6338XC



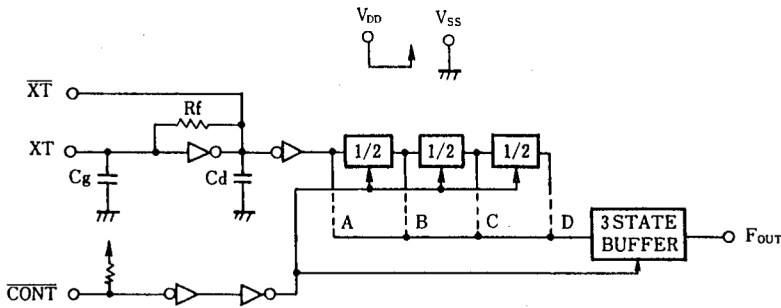
NJU6338XE

**■ PIN CONFIGURATION/PAD LOCATION**

**■ COORDINATES**

 Unit:  $\mu\text{m}$ 

No.	PAD	X	Y
1	V <sub>DD</sub>	-408	248
2	XT	-408	81
3	XT	-408	-86
4	CONT	-408	-248
5	V <sub>SS</sub>	464	-248
8	F <sub>OUT</sub>	464	248

Chip Size : 1.29 X 0.8mm  
 Chip Center : X=0 $\mu\text{m}$ , Y=0 $\mu\text{m}$   
 Chip Thickness : 400 $\mu\text{m}$ ±30 $\mu\text{m}$   
 (Note) No. 6 and 7 terminals are only for package type information. There are no PAD on the chip.

**■ BLOCK DIAGRAM**

**■ TERMINAL DESCRIPTION**

NO.	SYMBOL	F U N C T I O N						
1	$V_{DD}$	+ 5V						
2	$\overline{XT}$	Quartz Crystal Connecting Terminals						
3	XT							
4	$\overline{CONT}$	3-State Output Control and Divider Reset						
		<table border="1"> <thead> <tr> <th>CONT</th> <th><math>F_{OUT}</math></th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Output either one frequency from <math>f_0</math>, <math>f_0/2</math>, <math>f_0/4</math> and <math>f_0/8</math></td> </tr> <tr> <td>L</td> <td>Output High Impedance and Divider Reset</td> </tr> </tbody> </table>	CONT	$F_{OUT}$	H	Output either one frequency from $f_0$ , $f_0/2$ , $f_0/4$ and $f_0/8$	L	Output High Impedance and Divider Reset
		CONT	$F_{OUT}$					
H	Output either one frequency from $f_0$ , $f_0/2$ , $f_0/4$ and $f_0/8$							
L	Output High Impedance and Divider Reset							
5	$V_{SS}$	GND						
8	$F_{OUT}$	Output either one frequency from $f_0$ , $f_0/2$ , $f_0/4$ and $f_0/8$						

(Note) Reference the Line-Up Table

**■ ABSOLUTE MAXIMUM RATINGS**

 (  $T_a=25^\circ\text{C}$  )

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT
Supply Voltage	$V_{DD}$	-0.5 ~ +7.0	V
Input Voltage	$V_{IN}$	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	$V_O$	-0.5 ~ $V_{DD}+0.5$	V
Input Current	$I_{IN}$	$\pm 10$	mA
Output Current	$I_O$	$\pm 25$	mA
Power Dissipation	$P_D$	200 (EMP)	mW
Operating Temperature Range	$T_{opr}$	-40 ~ + 85	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 ~ +125	$^\circ\text{C}$

 (Note) Decoupling capacitor should be connected between  $V_{DD}$  and  $V_{SS}$  due to the stabilized operation for the circuit.

## ■ ELECTRICAL CHARACTERISTICS

 ( Ta=25°C, V<sub>DD</sub>=5V )

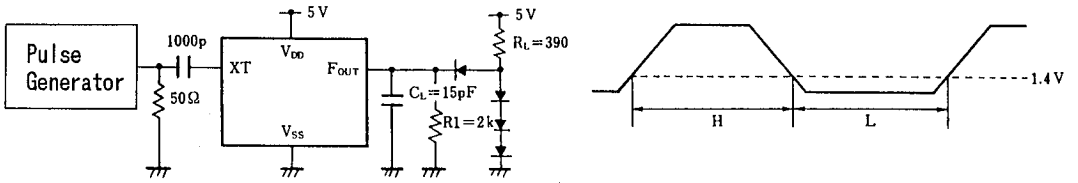
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V <sub>DD</sub>		4		6	V
Operating Current	I <sub>DD1</sub>	A,B,C,D f <sub>osc</sub> =24MHz, No Load			15	mA
	I <sub>DD2</sub>	H,J,K,L f <sub>osc</sub> =48MHz, No Load			20	
	I <sub>DD3</sub>	Q,R,S,T f <sub>osc</sub> =48MHz, No Load			25	
Stand-by Current	I <sub>st</sub>	$\overline{\text{CONT}}, \text{XT}=\text{V}_{\text{SS}}$ , No Load (Note)			1	μA
Input Voltage	V <sub>IH</sub>		3.5		5.0	V
	V <sub>IL</sub>		0		1.5	
Output Current	I <sub>OH</sub>	V <sub>DD</sub> =5V, V <sub>OH</sub> =4.5V	4			mA
	I <sub>OL</sub>	V <sub>DD</sub> =5V, V <sub>OL</sub> =0.5V	16			
Input Current	I <sub>IN</sub>	$\overline{\text{CONT}}$ Terminal, $\overline{\text{CONT}}=\text{V}_{\text{SS}}$	125	250	500	μA
3-St Off-leakage Current	I <sub>oz</sub>	$\overline{\text{CONT}}=\text{V}_{\text{SS}}$ , F <sub>OUT</sub> =V <sub>SS</sub> and V <sub>DD</sub>			±0.1	μA
Internal Capacitor	C <sub>g</sub> , C <sub>d</sub>	A,B,C,D Version, f <sub>osc</sub> =24MHz		28		pF
		H,J,K,L Version, f <sub>osc</sub> =48MHz		20		
		Q,R,S,T Version, f <sub>osc</sub> =48MHz		17		
Maximum Oscillation Frequency	f <sub>MAX</sub>	A,B,C,D Version	35			MHz
		H,J,K,L Version	50			
		Q,R,S,T Version	75			
Output Signal Symmetry	SYM	C <sub>L</sub> =15pF, R <sub>L</sub> =390Ω at 1.4V	45	50	55	%
Output Signal Rise Time	t <sub>r</sub>	C <sub>L</sub> =15pF, R <sub>L</sub> =390Ω, 0.4~2.4V			6	ns
Output Signal Fall Time	t <sub>f</sub>	C <sub>L</sub> =15pF, R <sub>L</sub> =390Ω, 2.4~0.4V			4	ns

 Note ) Excluding input current on  $\overline{\text{CONT}}$  terminal.

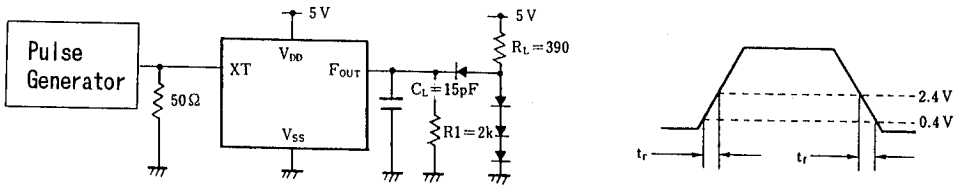
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■ MEASUREMENT CIRCUITS

(1) Output Signal Symmetry ( $C_L=15\text{pF}$ )



(2) Output Signal Rise / Fall Time ( $C_L=15\text{pF}$ )



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# NJU6338 Series

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MEMO

**[CAUTION]**

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