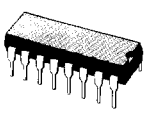
SGS-THOMSON MICROELECTRONICS

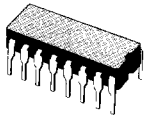
M54/M74HC367
M54/M74HC368

HEX BUS BUFFER (3-STATE)
HC367 NON INVERTING, HC368 INVERTING

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS367/368



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

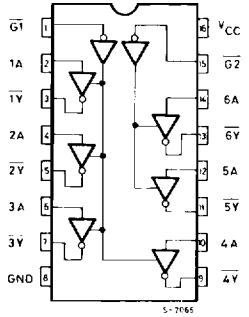
C1R
(Chip Carrier)

ORDER CODES :

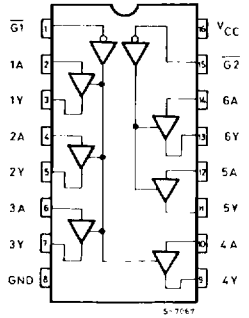
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)

HC368



HC367



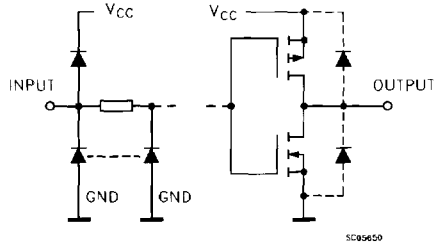
DESCRIPTION

The M54/74HC367 and the M54/74HC368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$) ; the outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).

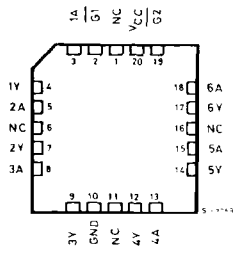
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

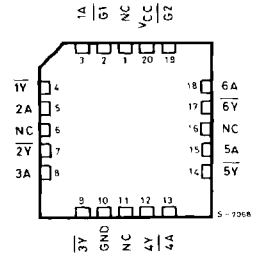


CHIP CARRIER

HC367



HC368



NC = No Internal Connection

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Y n (367)	$\overline{Y}$n (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X = DON'T CARE Z = HIGH IMPEDANCE

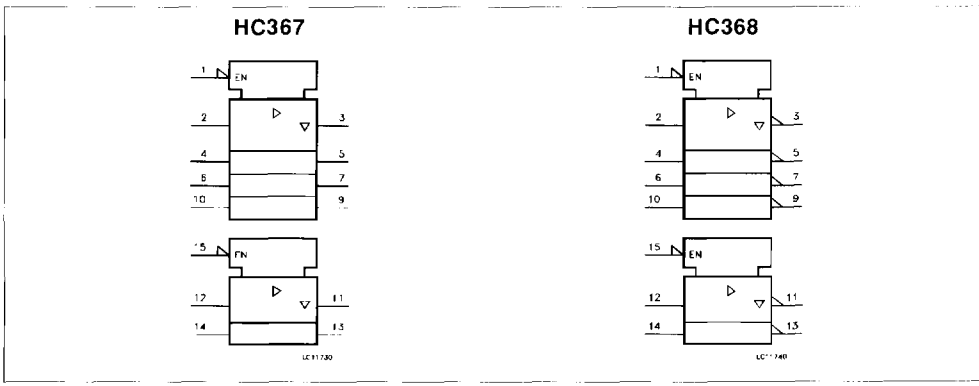
PIN DESCRIPTION (HC367)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC368)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	$\overline{1Y}$ to $\overline{6Y}$	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

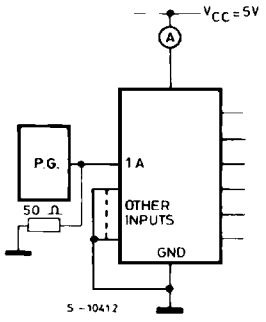
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			30	85		105		130	ns
		4.5				10	17		21		26	
		6.0				9	14		18		22	
		2.0	150			42	105		130		160	ns
		4.5				14	21		26		32	
		6.0				12	18		22		27	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		36	90		115		135	ns
		4.5				11	18		23		27	
		6.0				9	15		20		23	
		2.0	150	R_L = 1 KΩ		49	110		140		165	ns
		4.5				15	22		28		33	
		6.0				13	19		24		28	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		32	95		120		145	ns
		4.5				14	19		24		29	
		6.0				12	16		20		25	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					33						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Channel)

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

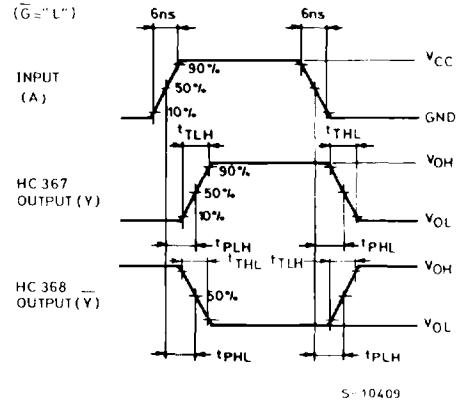
C_{PD} CALCULATION

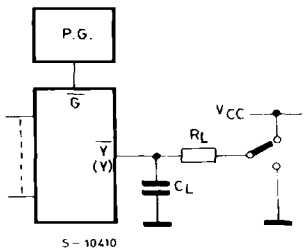
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (opr.) in the test circuit opposite.

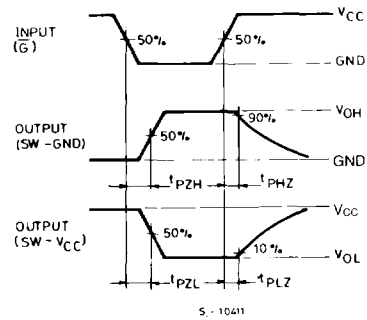
$$C_{PD} = \frac{I_{CC}\,(opr)}{f_{IN} \times V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SWITCHING CHARACTERISTICS TEST WAVEFORM







Note : Such a logic level shall be applied to each input that the output voltage stays in the apposite side to the switch connection level, when the output is enable.