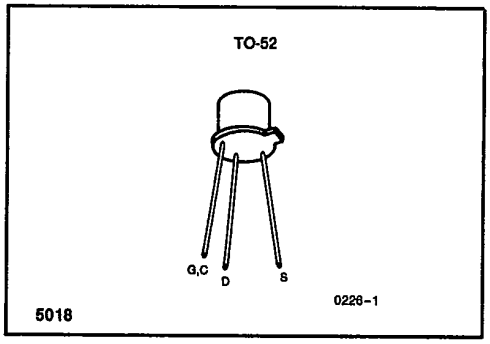
T-35-25

2N5432-2N5434
N-Channel JFET Switch

FEATURES
- Low $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage	−25V
Gate-Drain Voltage	−25V
Gate Current	100mA
Drain Current	400mA
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

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2N5432
2N5433
2N5434

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5432		2N5433		2N5434		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0		−200		−200		−200	pA
		T_A = 150°C		−200		−200		−200	nA
BV_{GSS}	Gate Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0	−25		−25		−25		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = −10V		200		200		200	pA
		T_A = 150°C		200		200		200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 3nA	−4	−10	−3	−9	−1	−4	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0	150		100		30		mA
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 10mA	2	5		7		10	ohm
$V_{DS(on)}$	Drain-Source ON Voltage			50		70		100	mV
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1kHz		5		7		10	ohm
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = 0, V_{GS} = −10V, f = 1MHz		30		30		30	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)			15		15		15	
t_d	Turn-ON Delay Time (Note 2)	V_{DD} = 1.5V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = −12V, $I_{D(on)}$ = 10mA		4		4		4	ns
t_r	Rise Time (Note 2)			1		1		1	
t_{off}	Turn-OFF Delay Time (Note 2)			6		6		6	
t_f	Fall Time (Note 2)			30		30		30	

NOTES: 1. Pulse test required, pulsewidth 300μs, duty cycle≤3%.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

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INTERSIL

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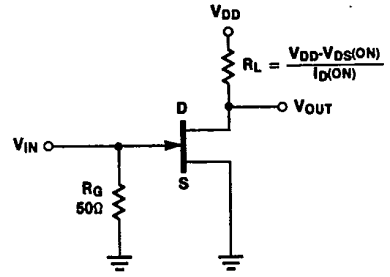

Input Pulse		Sampling Scope	
Rise Time	0.25 ns	Rise Time	0.4 ns
Fall Time	0.75 ns	Input Resistance	10 MΩ
Pulse Width	200 ns	Input Capacitance	1.5 pF
Pulse Rate	550 pps		

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Figure 1: Switching Time, Test Circuit

NOTE: All typical values have been characterized but are not tested.