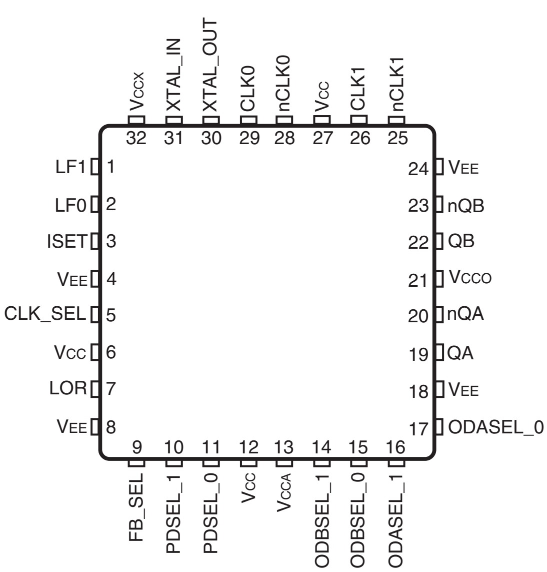
General Description

The ICS813N2532 device uses IDT's fourth generation FemtoClock® NG technology for optimal high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. The ICS813N2532 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation.

The ICS813N2532 is a fully integrated Phase Locked loop utilizing a FemtoClock NG Digital VCXO that provides the low jitter, high frequency SONET/PDH output clock that easily meets OC-48 jitter requirements. This VCXO technology simplifies PLL design by replacing the pullable crystal requirement of analog VCXOs with a fixed 27MHz generator crystal. Jitter attenuation down to 10Hz is provided by an external loop filter. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The device requires the use of an external, inexpensive fundamental mode 27MHz crystal. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

Pin Assignment

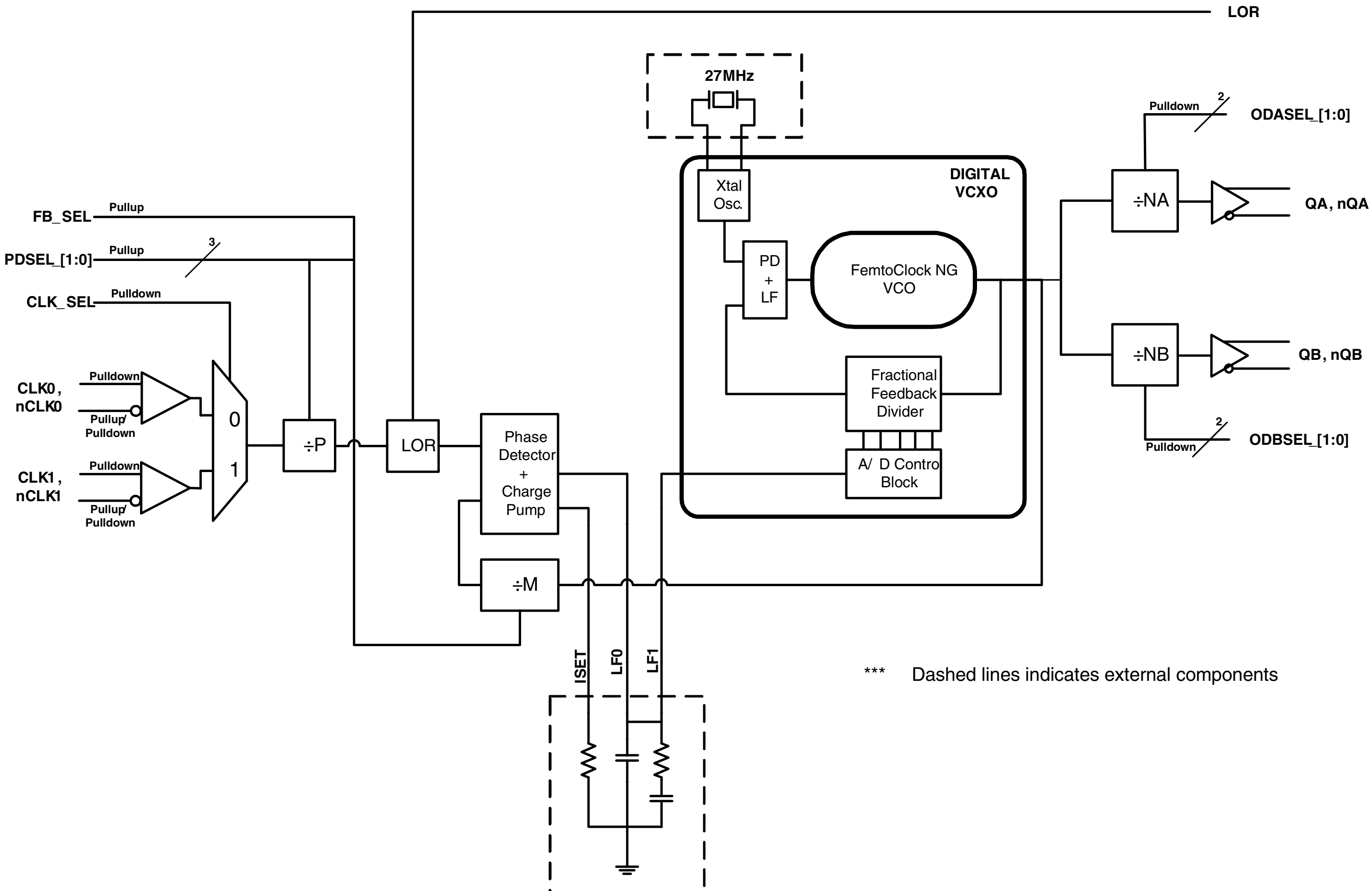


ICS813N2532
32 Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Features

- Fourth generation FemtoClock® NG technology
- Two LVPECL output pairs
- Output frequencies: 19.44MHz, 25MHz, 125MHz, 155.52MHz and 156.25MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Accepts input frequencies from 8kHz to 38.88MHz including 8kHz, 19.44MHz, 25MHz and 38.88MHz
- Crystal interface optimized for a 27MHz, 10pF parallel resonant crystal
- Attenuates the phase jitter of the input clock by using a low-cost fundamental mode crystal
- Customized settings for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock NG frequency multiplier provides low jitter, high frequency output
- Absolute pull range: ±100ppm
- Power supply noise rejection (PSNR): -95dB (typical)
- RMS phase jitter @ 156.25MHz, using a 27MHz crystal (12kHz – 20MHz): 0.6ps (typical)
- RMS phase jitter @ 155.52MHz, using a 27MHz crystal (12kHz – 20MHz): 0.622ps (typical)
- RMS phase jitter @ 125MHz, using a 27MHz crystal (12kHz – 20MHz): 0.6ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



*** Dashed lines indicates external components

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins. LF0 is the output. LF1 is the input.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 8, 18, 24	V_{EE}	Power		Negative supply pins.
5	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTL interface levels.
6, 12, 27	V_{CC}	Power		Core supply pins.
7	LOR	Output		Loss of reference indicator. LVCMOS/LVTTL interface levels.
9	FB_SEL	Input	Pullup	Feedback divider select pin. LVCMOS/LVTTL interface levels. See Table 3B.
10, 11	PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	V_{CCA}	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for Bank B output. See Table 3C. LVCMOS/LVTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for Bank A output. See Table 3C. LVCMOS/LVTTL interface levels.
19, 20	QA, nQA	Output		Differential Bank A clock outputs. LVPECL interface levels.
21	V_{CCO}	Power		Output supply pin.
22, 23	QB, nQB	Output		Differential Bank B clock outputs. LVPECL interface levels.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V_{CCX}	Power		Power supply pin for the crystal oscillator.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Pre-Divider Selection Function Table

Inputs		
PDSEL_1	PDSEL_0	÷P Value
0	0	1
0	1	1944
1	0	2500
1	1	3888 (default)

Table 3C. Output Divider Function Table

Inputs		
ODxSEL_1	ODxSEL_0	÷Nx Value
0	0	128 (default)
0	1	100
1	0	20
1	1	16

NOTE: x denotes A or B.

Table 3B. Feedback Divider Selection Function Table

Input	
FB_SEL	VCO Frequency (MHz)
0	2500
1	2488.32 (default)

Table 3D. Frequency Function Table

Input Frequency (MHz)	÷P Value	FemtoClock NG VCXO Center Frequency (MHz)	÷Nx Value	Output Frequency (MHz)
0.008	1	2488.32	128	19.44
0.008	1	2500	100	25
0.008	1	2500	20	125
0.008	1	2488.32	16	155.52
0.008	1	2500	16	156.25
19.44	1944	2488.32	128	19.44
19.44	1944	2500	100	25
19.44	1944	2500	20	125
19.44	1944	2488.32	16	155.52
19.44	1944	2500	16	156.25
25	2500	2488.32	128	19.44
25	2500	2500	100	25
25	2500	2500	20	125
25	2500	2488.32	16	155.52
25	2500	2500	16	156.25
38.88	3888	2488.32	128	19.44
38.88	3888	2500	100	25
38.88	3888	2500	20	125
38.88	3888	2488.32	16	155.52
38.88	3888	2500	16	156.25

NOTE: x denotes A or B.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.31	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCX}	Crystal Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				300	mA
I_{CCA}	Analog Supply Current				31	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, CLK0, ODASEL_[1:0], ODBSEL_[1:0]	$V_{CC} = V_{IN} = 3.465V$			150	µA
		FB_SEL, PDSEL_[1:0]	$V_{CC} = V_{IN} = 3.465V$			10	µA
I_{IL}	Input Low Current	CLK_SEL, CLK0, ODASEL_[1:0], ODBSEL_[1:0]	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		FB_SEL, PDSEL_[1:0]	$V_{CC} = 3.465$, $V_{IN} = 0V$	-150			µA

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, nCLK0, CLK1, nCLK1	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		nCLK0, nCLK1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE}		$V_{CC} – 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined at the crosspoint.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} – 1.10$		$V_{CCO} – 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} – 2.0$		$V_{CCO} – 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V. See Parameter Measurement Information section, *3.3V Output Load Test Circuit.*

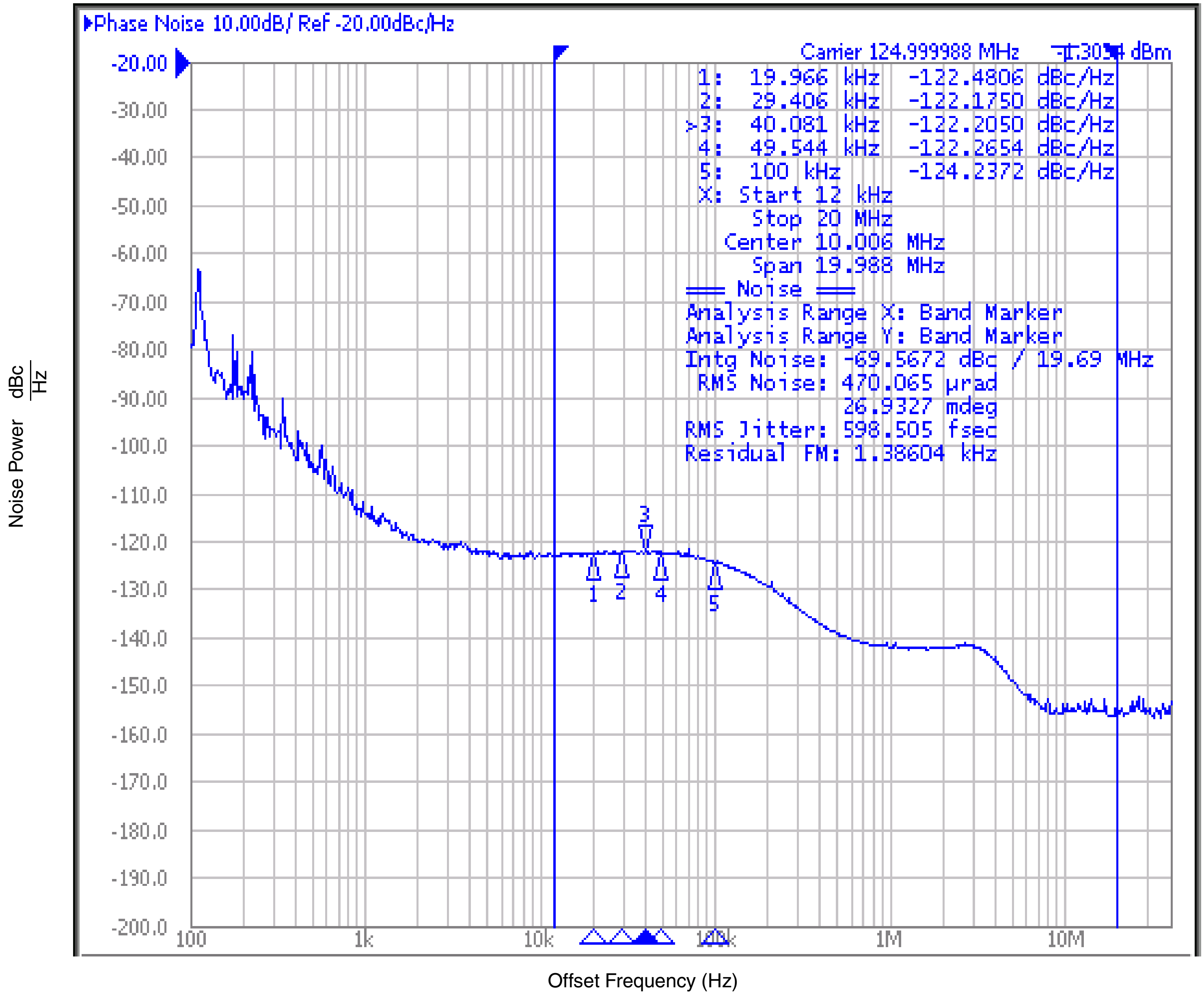
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

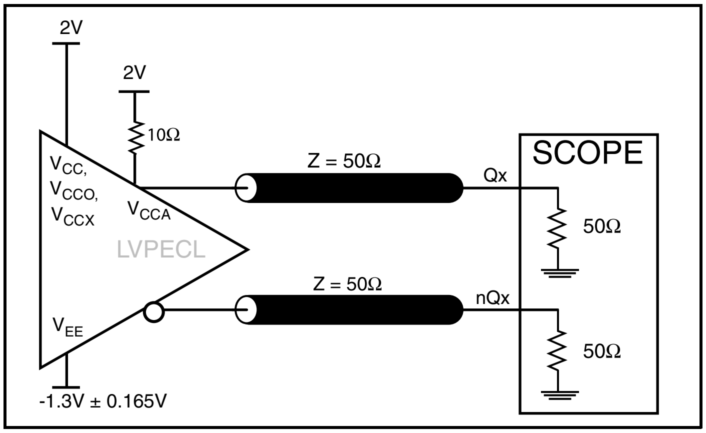
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		0.008		38.88	MHz
f_{OUT}	Output Frequency		19.44		156.25	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	156.25MHz f_{OUT}, 27MHz crystal, Integration Range: 12kHz – 20MHz		0.6		ps
		155.52MHz f_{OUT}, 27MHz crystal, Integration Range: 12kHz – 20MHz		0.622		ps
		125MHz f_{OUT}, 27MHz crystal, Integration Range: 12kHz – 20MHz		0.6		ps
*t*sk(o)	Output Skew; NOTE 2, 3				80	ps
PSNR	Power Supply Noise Rejection; NOTE 4	V_{PP} = 50mV Sine Wave, Range: 10kHz – 10MHz		-95		dB
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	Output-to-Input Phase Lock Time; NOTE 5	Reference Clock Input is ±100ppm from Nominal Frequency		3		s

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with outputs at the same frequency using the loop filter components for the 44Hz loop bandwidth.
Refer to Jitter Attenuator Loop Bandwidth Selection Table.
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: PSNR results achieved by injecting noise on V_{CCA} supply pin with no external filter network.
NOTE 5: Lock Time measured from power-up to stable output frequency.

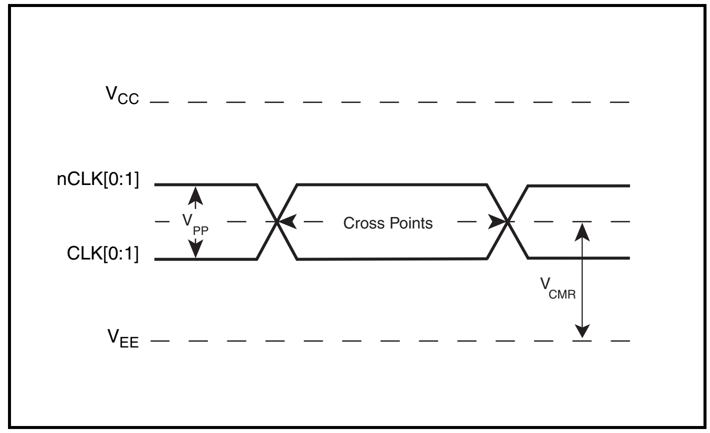
Typical Phase Noise at 125MHz



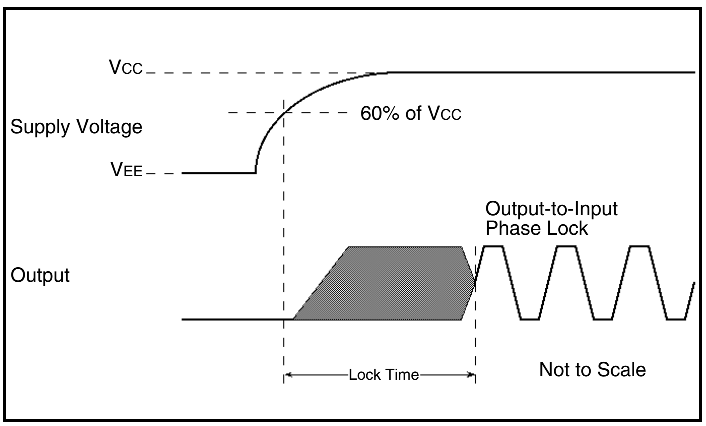
Parameter Measurement Information



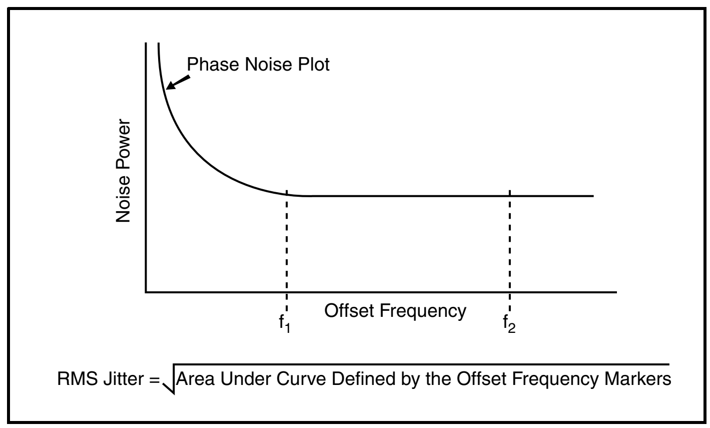
3.3V LVPECL Output Load AC Test Circuit



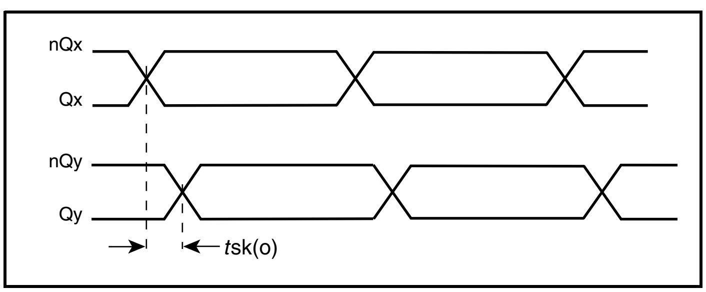
Differential Input Level



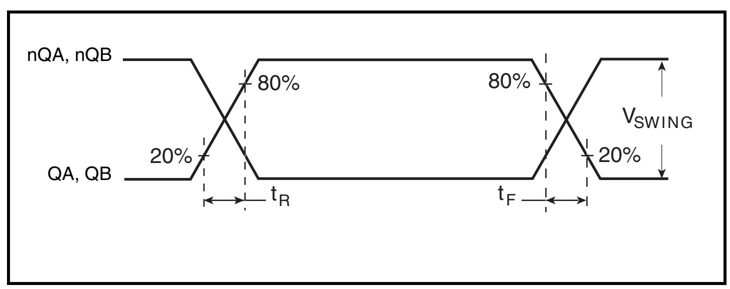
Output-to-Input Phase Lock Time



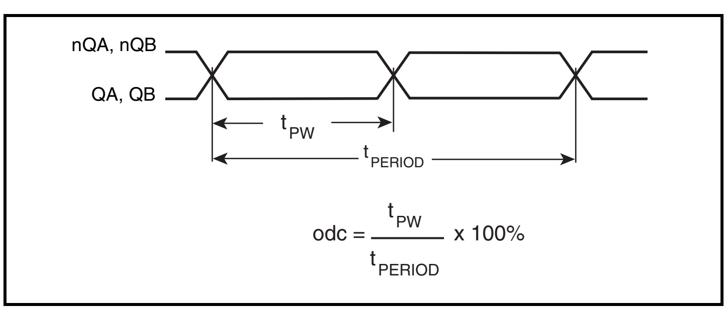
RMS Phase Jitter



Output Skew



LVPECL Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS813N2532 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, V_{CCO} and V_{CCX} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

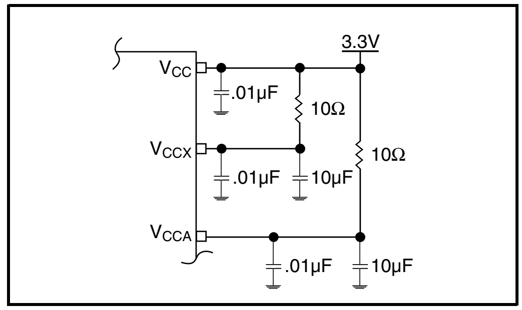


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

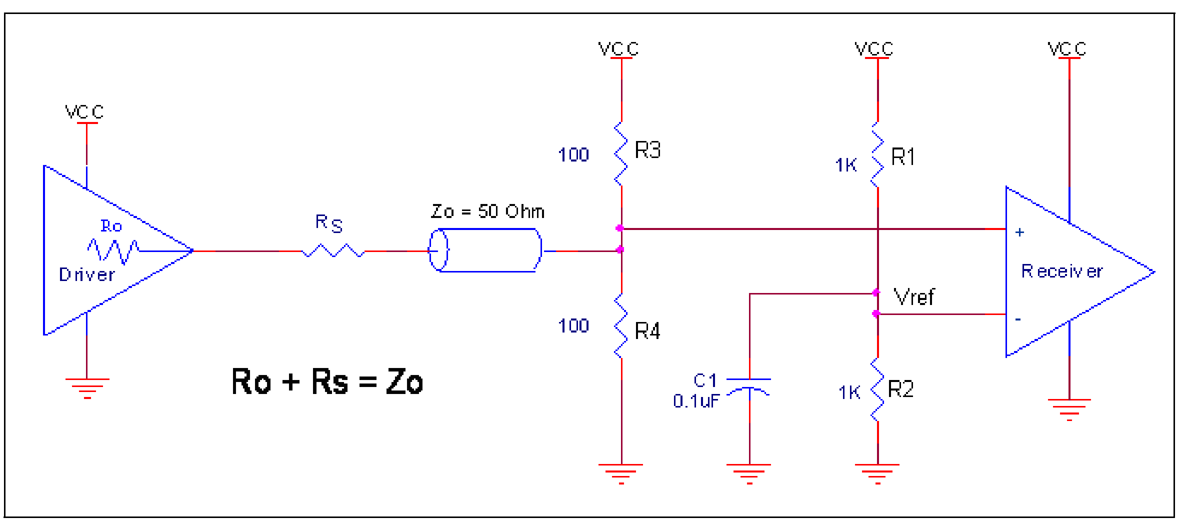


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

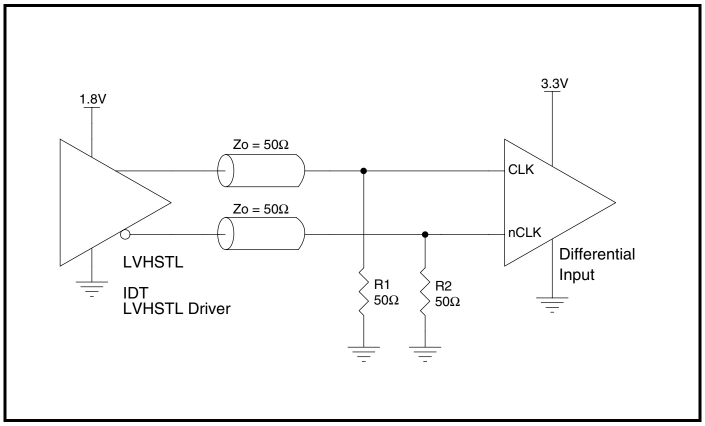


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

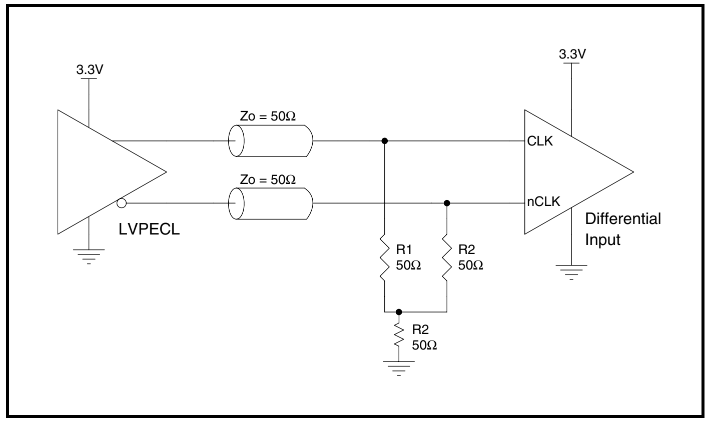


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

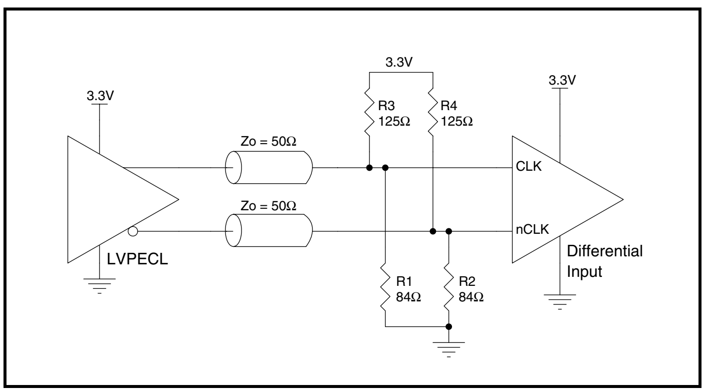


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

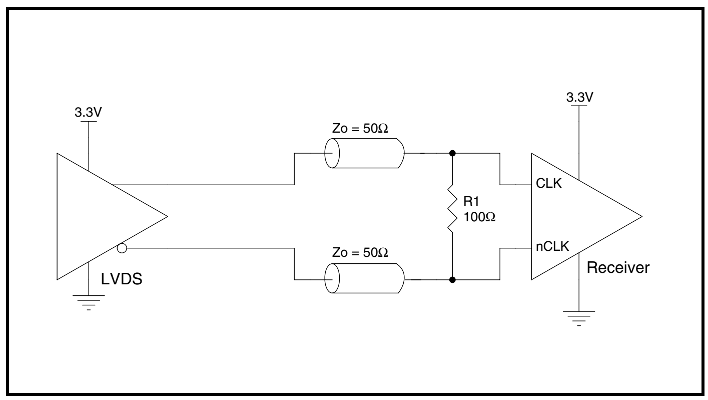


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

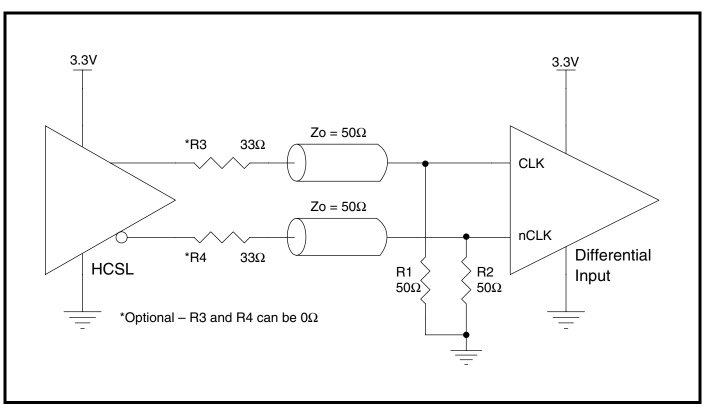


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

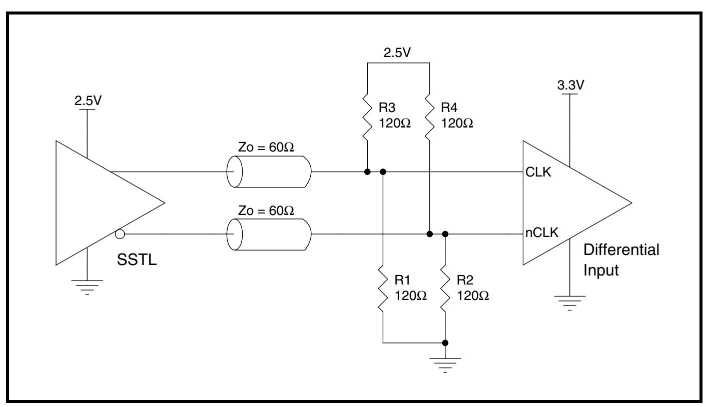


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

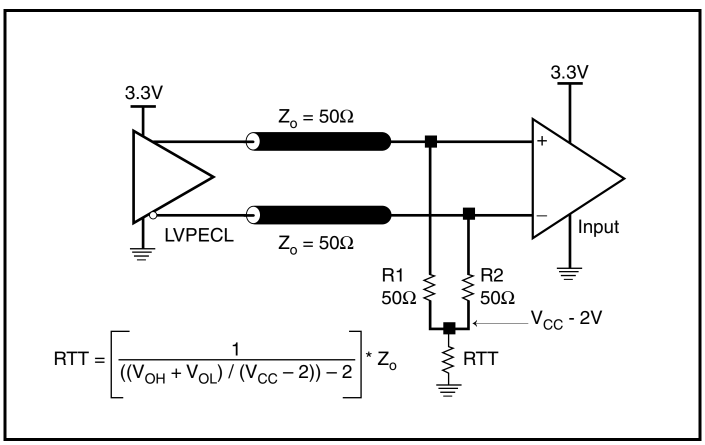


Figure 4A. 3.3V LVPECL Output Termination

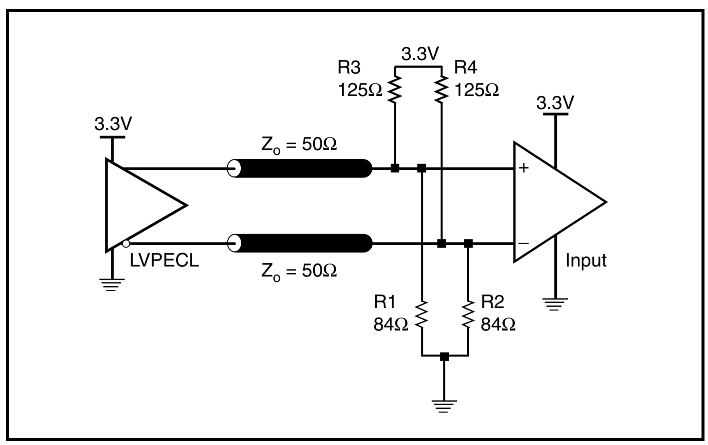
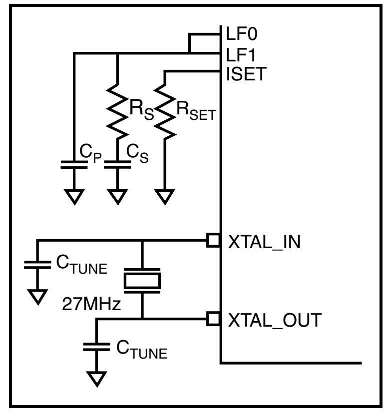


Figure 4B. 3.3V LVPECL Output Termination

Jitter Attenuator External Components

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the Jitter Attenuator. In choosing a crystal, special precaution must be taken with load capacitance (C_L), frequency accuracy and temperature range.

The crystal's C_L characteristic determines its resonating frequency and is closely related to the center tuning of the crystal. The total external capacitance seen by the crystal when installed on a PCB is the sum of the stray board capacitance, IC package lead capacitance, internal device capacitance and any installed tuning capacitors (CTUNE). The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve for a typical PCB. If the crystal C_L is greater than the total external capacitance, the crystal will oscillate at a higher frequency than the specification. If the crystal C_L is lower than the total external capacitance, the crystal will oscillate at a lower frequency than the specification. Tuning adjustments might be required depending on the PCB parasitics or if using a crystal with a higher C_L specification. In addition, the frequency accuracy specification in the crystal characteristics table are used to calculate the APR (Absolute Pull Range).



Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			27		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		0		+70	^{0}C
C_L	Load Capacitance			10		pF
C_O	Shunt Capacitance			4		pF
ESR	Equivalent Series Resistance				40	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C	First Year			±3	ppm

The VCXO-PLL Loop Bandwidth Selection Table shows RS, CS,CP and RSET values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. In addition, the digital VCXO gain (KVCXO) has been provided for additional loop filter requirements.

Jitter Attenuator Characteristics Table

Symbol	Parameter	Typical	Units
k_{VCXO}	VCXO Gain	2.79	kHz/V

Jitter Attenuator Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency	R_S (kΩ)	C_S (µF)	C_P (µF)	R_{SET} (kΩ)
9Hz (Low)	27MHz	110	10	0.01	2.21
44Hz (Mid)	27MHz	365	1	0.002	1.5
56Hz (High)	27MHz	470	1	0.0005	1.5

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

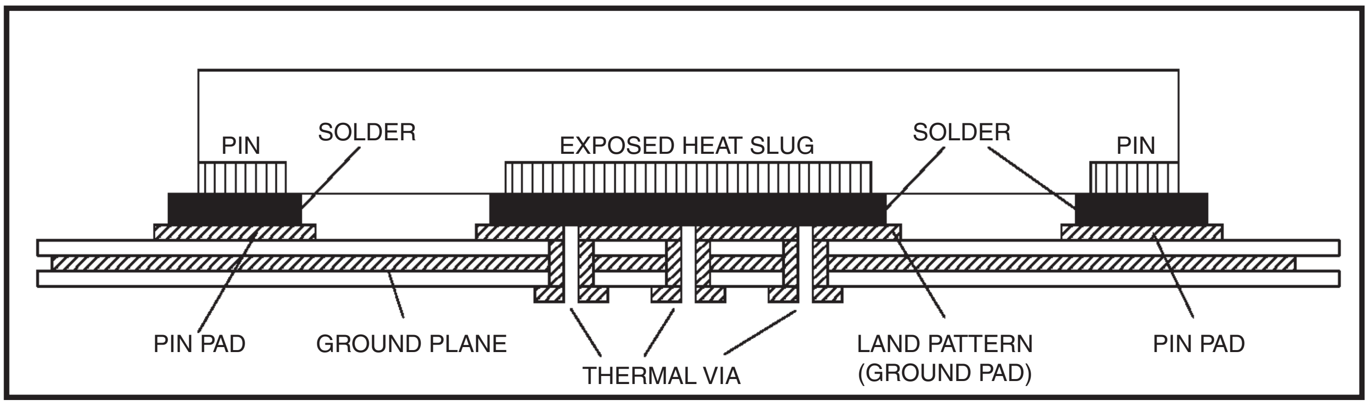


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)