

SRAM

128K x 8 SRAM

WITH SINGLE CHIP ENABLE

FEATURES

- High speed: 20, 25, 35, 45, 55 and 70ns
- Automatic Chip Enable power down
- All inputs and outputs are TTL compatible
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Fast Output Enable access time: 8ns
- Replaces industry standard 128K x 8 multichip SRAM module

OPTIONS

- Timing

20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*

*Electrical characteristics identical to those provided for the 45ns device.

MARKING

- Packages

Plastic DIP (400 mil)	None
Plastic DIP (600 mil)	W
Plastic SOJ (400 mil)	DJ

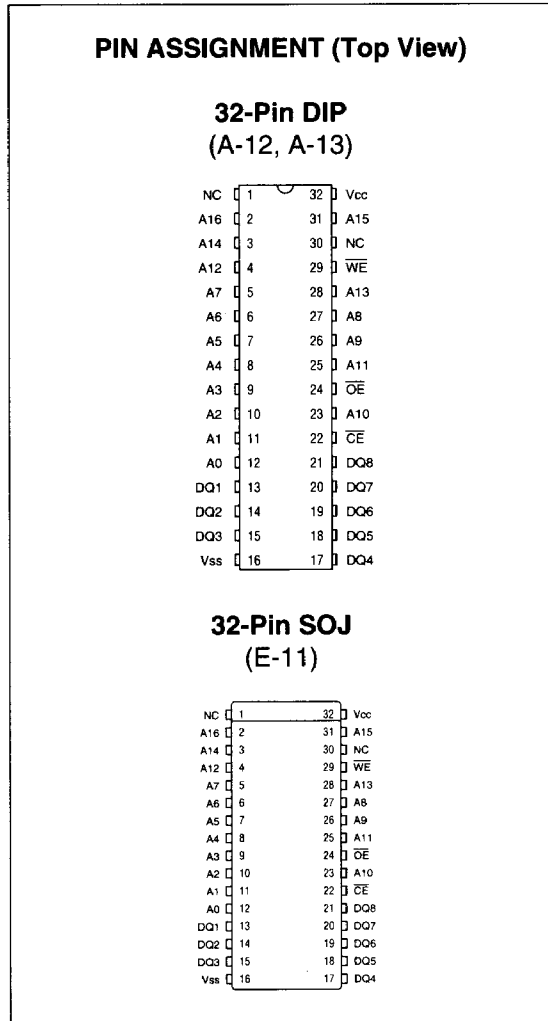
Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- 2V data retention L
- Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

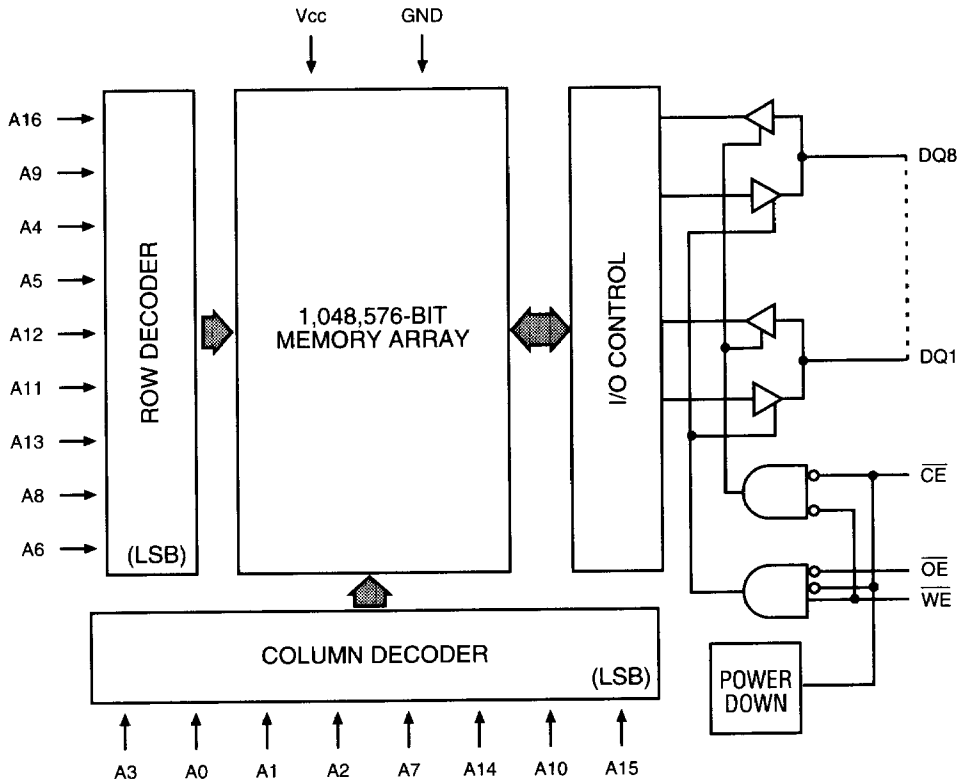
Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is



accomplished when \overline{WE} remains HIGH and \overline{CE} goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a gray code.

TRUTH TABLE

MODE	\overline{OE}	\overline{CE}	\overline{WE}	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-1V to +7V
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX				UNITS	NOTES
				-20	-25	-35	-45		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ f = MAX = 1/'RC Outputs Open	I _{CC}	95	140	125	115	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ f = MAX = 1/'RC Outputs Open	I _{SB1}	17	35	30	25	25	mA	14
	$\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V _{IL} ≤ V _{SS} +0.2V V _{IH} ≥ V _{CC} -0.2V; f = 0	I _{SB2}	0.4	5	5	5	5	mA	14
"L" version only	$\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V _{IL} ≤ V _{SS} +0.2V V _{IH} ≥ V _{CC} -0.2V; f = 0	I _{SB2}	0.3	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C, f = 1 MHz V _{CC} = 5V	C _I	8	pF	4
Output Capacitance		C _O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	SYM	-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	t ¹ RC	20		25		35		45		ns	
Address access time	t ¹ AA		20		25		35		45	ns	
Chip Enable access time	t ¹ ACE		20		25		35		45	ns	
Output hold from address change	t ¹ OH	5		5		5		5		ns	
Chip Enable to output in Low-Z	t ¹ LZCE	5		5		5		5		ns	
Chip disable to output in High-Z	t ¹ HZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	t ¹ PU	0		0		0		0		ns	
Chip disable to power-down time	t ¹ PD		20		25		35		45	ns	
Output Enable access time	t ¹ AOE		6		8		12		15	ns	
Output Enable to output in Low-Z	t ¹ LZOE	0		0		0		0		ns	
Output disable to output in High-Z	t ¹ HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	t ¹ WC	20		25		35		45		ns	
Chip Enable to end of write	t ¹ CW	12		15		20		25		ns	
Address valid to end of write	t ¹ AW	12		15		20		25		ns	
Address setup time	t ¹ AS	0		0		0		0		ns	
Address hold from end of write	t ¹ AH	0		0		0		0		ns	
WRITE pulse width	t ¹ WP1	12		15		20		25		ns	
WRITE pulse width	t ¹ WP2	15		15		20		25		ns	
Data setup time	t ¹ DS	8		10		15		20		ns	
Data hold time	t ¹ DH	0		0		0		0		ns	
Write disable to output in Low-Z	t ¹ LZWE	5		5		5		5		ns	
Write Enable to output in High-Z	t ¹ HZWE	0	8	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

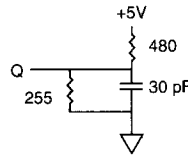


Fig. 1 OUTPUT LOAD EQUIVALENT

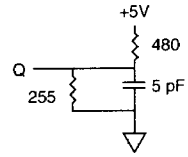


Fig. 2 OUTPUT LOAD EQUIVALENT

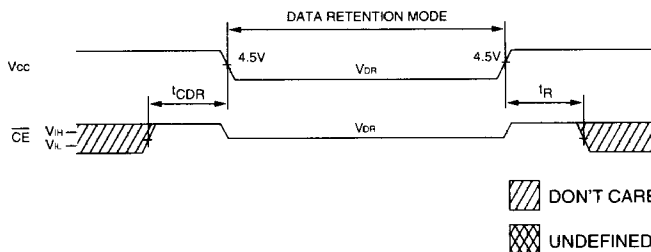
NOTES

- All voltages referenced to V_{ss} (GND).
- 3V for pulse width < 20ns.
- I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{t_{RC} (MIN)}$ Hz.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- ^tHZCE, ^tHZOE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
- \overline{WE} is HIGH for READ cycle.
- Device is continuously selected. Chip enable and output enables are held in their active state.
- Address valid prior to or coincident with latest occurring chip enable.
- ^tRC = Read Cycle Time.
- Chip enable (\overline{CE}) and write enable (\overline{WE}) can initiate and terminate a WRITE cycle.
- For automotive, industrial and extended temperature specifications, refer to page 1-177.
- Typical values are measured at 5V, 25°C and 25ns cycle time.

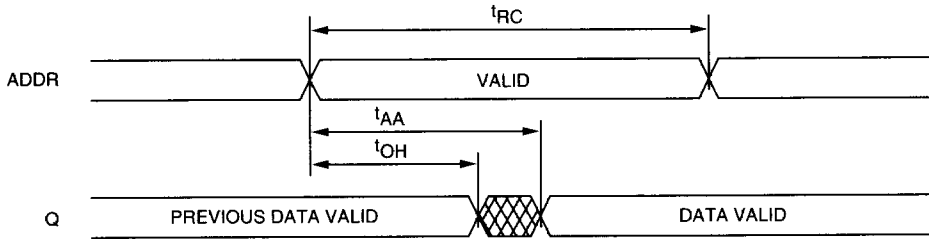
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} for Retention Data		V _{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$	V _{CC} = 2V		35	200	μA	
	$V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	V _{CC} = 3V		70	400	μA	
		V _{CC} = 5V		250	1,300	μA	
Chip Deselect to Data Retention Time		^t CDR	0		—	ns	4
Operation Recovery Time		^t R	^t RC			ns	4, 11

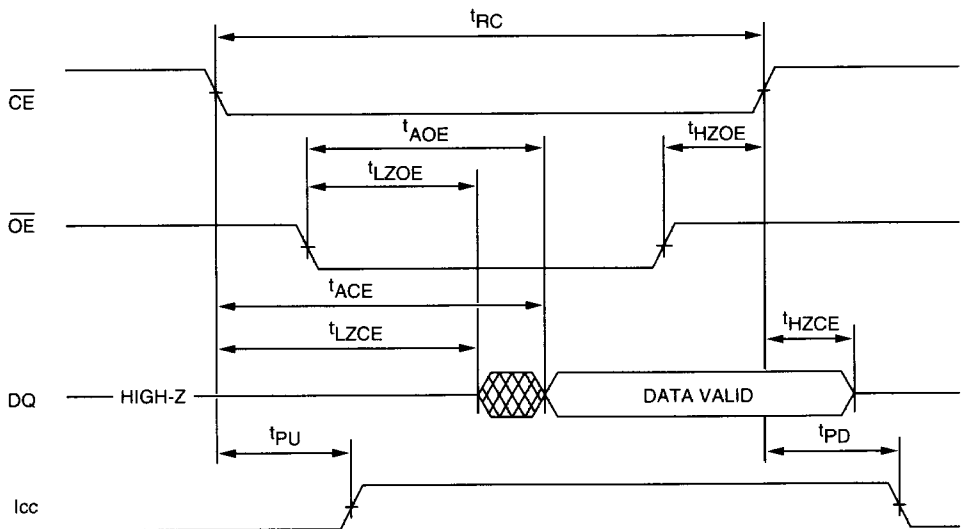
LOW V_{CC} DATA RETENTION WAVEFORM



READ CYCLE NO. 1 8, 9



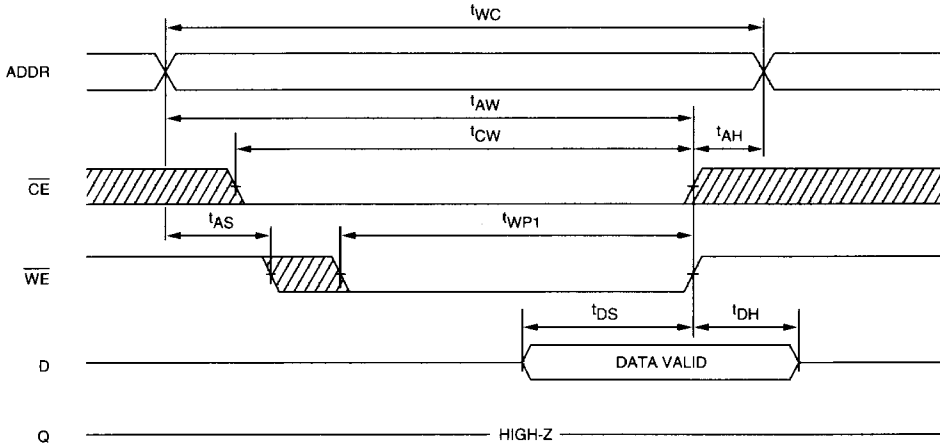
READ CYCLE NO. 2 7, 8, 10



 DON'T CARE

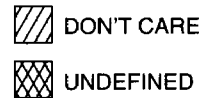
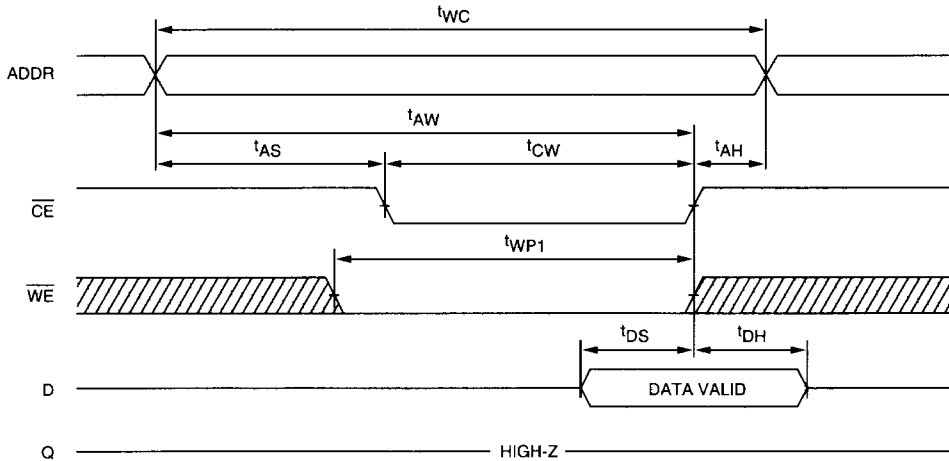
 UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) ¹²



NOTE: Output enable (\overline{OE}) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled)



WRITE CYCLE NO. 3 (Write Enable Controlled) 7, 12

