18Mb SYNCBURST™ SRAM

MT58L1MY18D, MT58V1MV18D,
MT58L512Y32D, MT58V512V32D,
MT58L512Y36D, MT58V512V36D

3.3V V_{DD}, 3.3V or 2.5V I/O; 2.5V V_{DD}, 2.5V I/O, Pipelined, Double-Cycle Deselect

FEATURES

- Fast clock and OE# access times
- Single +3.3V ±0.165V or 2.5V ±0.125V power supply (V_{DD})
- Separate +3.3V or 2.5V isolated output buffer supply ($V_{DD}Q$)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os, and control signals
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Automatic power-down
- Low capacitive bus loading
- x18, x32, and x36 versions available

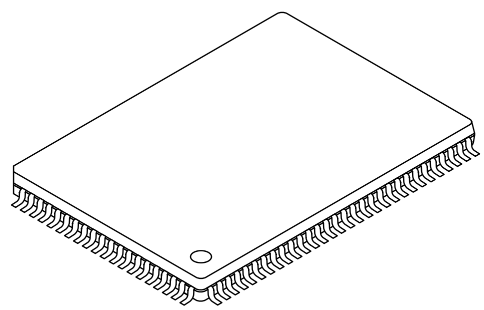
OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
2.5V V_{DD}, 2.5V I/O	
3.5ns/6ns/166 MHz	-6
4.0ns/7.5ns/133 MHz	-7.5
5.0ns/10ns/100 MHz	-10
3.3V V_{DD}, 3.3V or 2.5V I/O	
4.0ns/7.5ns/133 MHz	-7.5
5.0ns/10ns/100 MHz	-10
• Configurations	
3.3V V_{DD}, 3.3V or 2.5V I/O	
1 Meg x 18	MT58L1MY18D
512K x 32	MT58L512Y32D
512K x 36	MT58L512Y36D
2.5V V_{DD}, 2.5V I/O	
1 Meg x 18	MT58V1MV18D
512K x 32	MT58V512V32D
512K x 36	MT58V512V36D
• Packages	
100-pin TQFP (3-chip enable)	T
165-pin FBGA	F*
119-pin, 14mm x 22mm BGA	B
• Operating Temperature Range	
Commercial (0ºC to +70ºC)	None

Part Number Example:

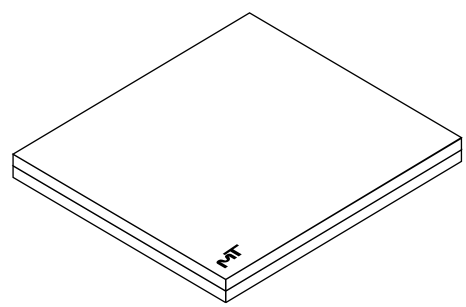
MT58L1MY18DT-7.5

* A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/support/index.html.

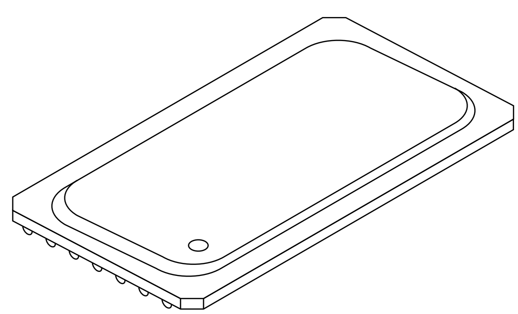
100-Pin TQFP[1]



165-Pin FBGA

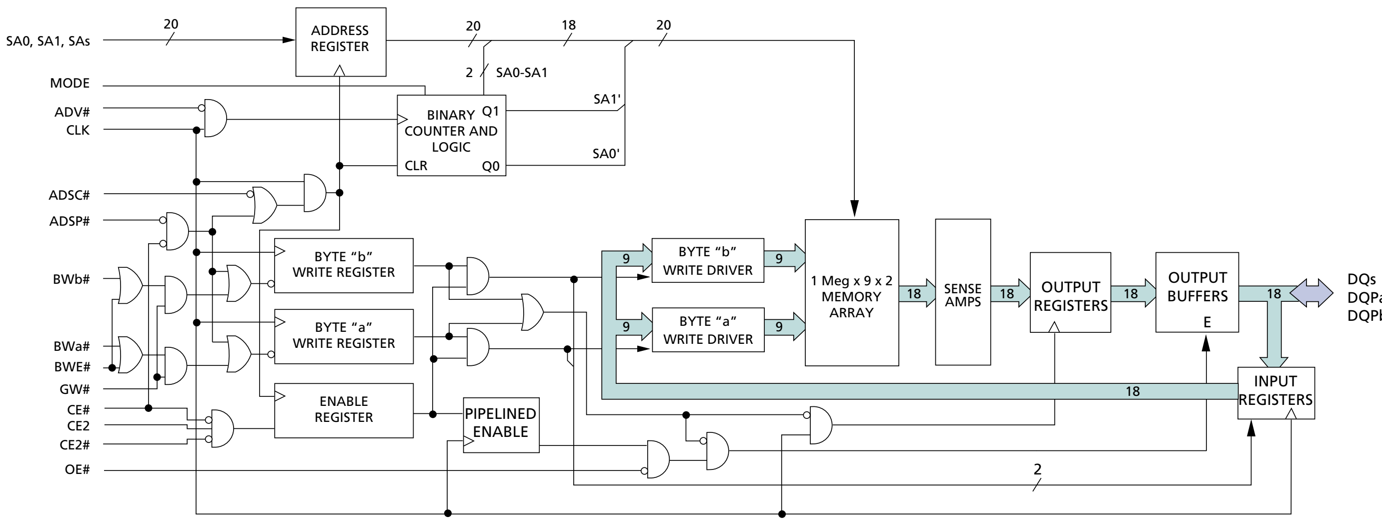


119-Pin BGA[2]

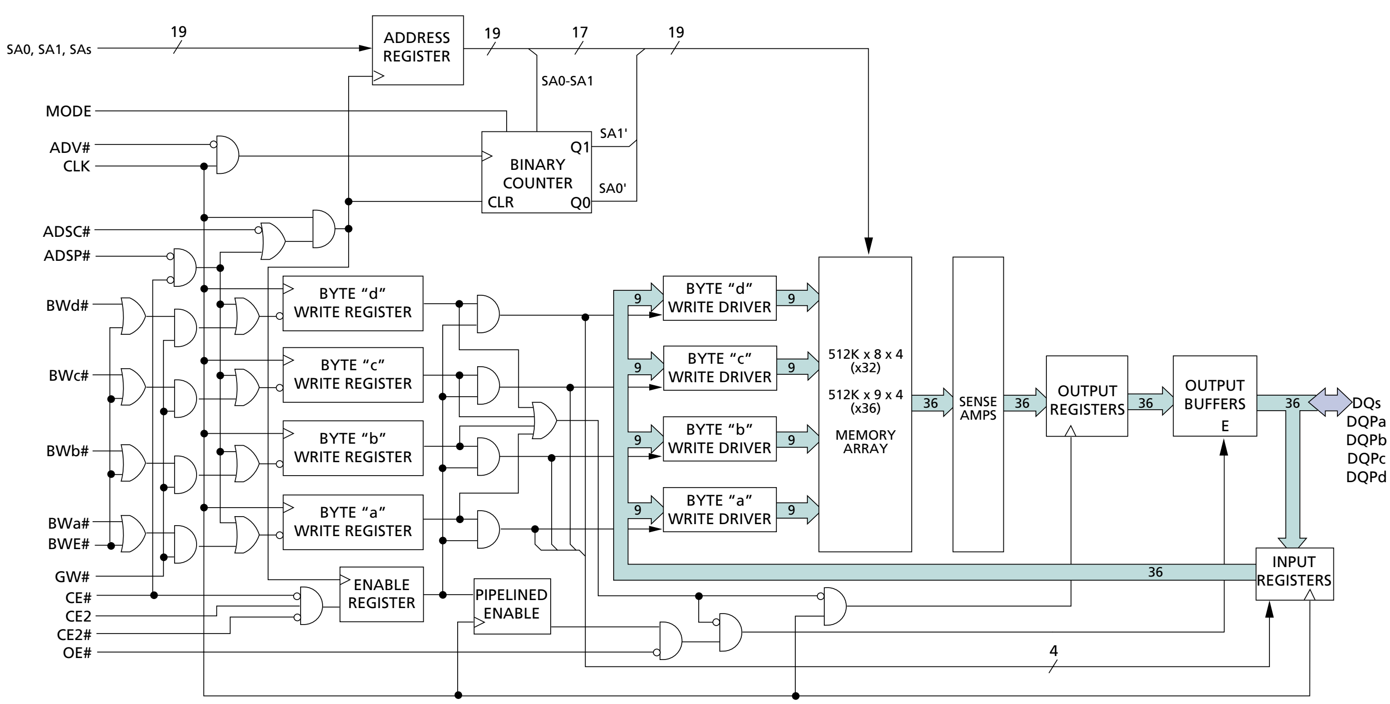


NOTE: 1. JEDEC-standard MS-026 BHA (LQFP).
2. JEDEC-standard MS-028 BHA (PBGA).

FUNCTIONAL BLOCK DIAGRAM
1 MEG x 18



FUNCTIONAL BLOCK DIAGRAM
512K x 32/36



NOTE: Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information.

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 18Mb SyncBurst SRAMs integrate a 1 Meg x 18, 512K x 32, or 512K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#), and global write (GW#). Note that CE2# is not available on the T Version.

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQbs and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates an additional pipelined enable register which delays turning off the output buffer an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

The device is ideally suited for Pentium® and PowerPC pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64-, and 72-bit-wide applications.

Please refer to Micron' Web site (www.micron.com/sram) for the latest data sheet.

DUAL VOLTAGE I/O

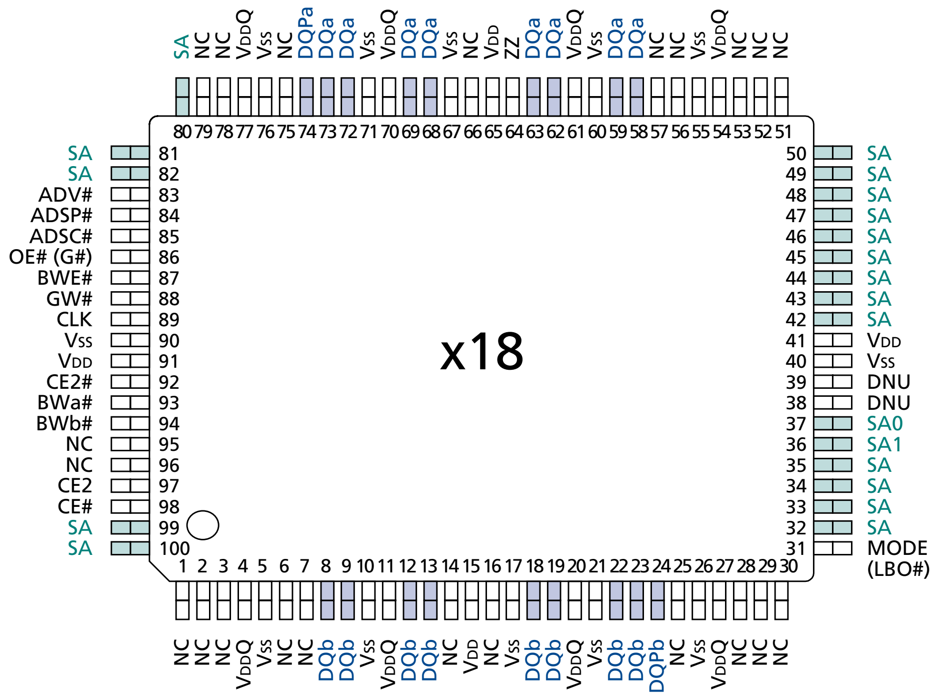
The 3.3V V_{DD} device is tested for 3.3V and 2.5V I/O function. The 2.5V V_{DD} device is tested for only 2.5V I/O function.

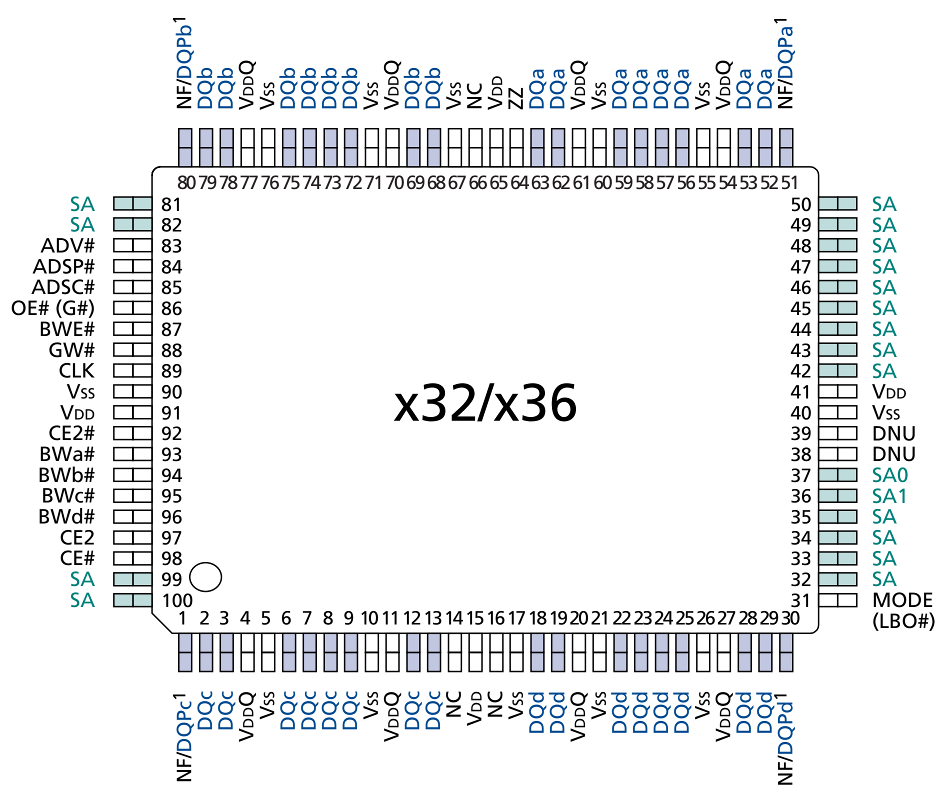
TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NF	DQPc[1]
2	NC	DQc	DQc
3	NC	DQc	DQc
4	$V_{DD}Q$		
5	V_{SS}		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	V_{SS}		
11	$V_{DD}Q$		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	NC		
15	V_{DD}		
16	NC		
17	V_{SS}		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	$V_{DD}Q$		
21	V_{SS}		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQPb	DQd	DQd
25	NC	DQd	DQd
26	V_{SS}		
27	$V_{DD}Q$		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NF	DQPd[1]
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	V_{SS}		
41	V_{DD}		
42	SA		
43	SA		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		
51	NC	NF	DQPa[1]
52	NC	DQa	DQa
53	NC	DQa	DQa
54	$V_{DD}Q$		
55	V_{SS}		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	V_{SS}		
61	$V_{DD}Q$		
62	DQa		
63	DQa		
64	ZZ		
65	V_{DD}		
66	NC		
67	V_{SS}		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	$V_{DD}Q$		
71	V_{SS}		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQPa	DQb	DQb
75	NC	DQb	DQb
76	V_{SS}		
77	$V_{DD}Q$		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NF	DQPb[1]
81	SA		
82	SA		
83	ADV#		
84	ADSP#		
85	ADSC#		
86	OE# (G#)		
87	BWE#		
88	GW#		
89	CLK		
90	V_{SS}		
91	V_{DD}		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

NOTE: 1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (TOP VIEW)
100-PIN TQFP





NOTE: 1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.

TQFP PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 42-50, 80-82, 99, 100	37 36 32-35, 42-50, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. For the x32 and x36 versions, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. Parity is only available on the x18 and x36 versions.
87	87	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
88	88	GW#	Input	Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This pin has an internal pull-down and can be floating.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
83	83	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

(continued on next page)

TQFP PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
84	84	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2, and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
85	85	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
(a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12, 13, 18, 19, 22, 23	(a) 52, 53, 56-59, 62, 63 (b) 68, 69 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins. For the x32 and x36 versions, Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
74 24 – –	51 80 1 30	NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Parity Data I/Os: On the x32 version, these pins are no function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd. No function pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.
15, 41, 65, 91	15, 41, 65, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.
38, 39	38, 39	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1-3, 6, 7, 14 16, 25, 28-30, 51-53, 56, 57, 66, 75, 78, 79, 95, 96	14, 16, 66	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

PIN LAYOUT (TOP VIEW)
165-PIN FBGA

x18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWb#	NC	CE2#	BWE#	ADSC#	ADV#	SA	SA
B	NC	SA	CE2	NC	BWa#	CLK	GW#	OE# (G#)	ADSP#	SA	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	VDD	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	SA	VSS	VSS	VDDQ	NC	NC
P	NC	NC	SA	SA	TD1	SA1	TD0	SA	SA	SA	SA
R	MODE (LBO#)	NC	SA	SA	TMS	SA0	TCK	SA	SA	SA	SA

TOP VIEW

x32/x36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWc#	BWb#	CE2#	BWE#	ADSC#	ADV#	SA	NC
B	NC	SA	CE2	BWd#	BWa#	CLK	GW#	OE# (G#)	ADSP#	SA	NC
C	NF/DQPc[1]	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	NF/DQPb[1]
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	VDD	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	NF/DQPd[1]	NC	VDDQ	VSS	NC	SA	VSS	VSS	VDDQ	NC	NF/DQPa[1]
P	NC	NC	SA	SA	TD1	SA1	TD0	SA	SA	SA	SA
R	MODE (LBO#)	NC	SA	SA	TMS	SA0	TCK	SA	SA	SA	SA

TOP VIEW

NOTE: 1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.

FBGA PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
6R 6P 2A, 2B, 3P, 3R, 4P, 4R, 6N, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11A, 11P, 11R	6R 6P 2A, 2B, 3P, 3R, 4P, 4R, 6N, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11P, 11R	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5B 4A – –	5B 5A 4A 4B	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. For the x32 and x36 versions, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. Parity is only available on the x18 and x36 versions.
7A	7A	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
7B	7B	GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
6B	6B	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3A	3A	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
6A	6A	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
11H	11H	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
3B	3B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
8B	8B	OE#(G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.

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FBGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
9A	9A	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on ADV# effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.
9B	9B	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2, and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
8A	8A	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
1R	1R	MODE (LB0#)	Input	Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
5R 5P 7R	5R 5P 7R	TMS TDI TCK	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These pins may be left not connected if the JTAG function is not used in the circuit.
(a) 10J, 10K, 10L, 10M, 11D, 11E, 11F, 11G (b) 1J, 1K, 1L, 1M, 2D, 2E, 2F, 2G	(a) 10J, 10K, 10L, 10M, 11J, 11K, 11L, 11M (b) 10D, 10E, 10F, 10G, 11D, 11E, 11F, 11G (c) 1D, 1E, 1F, 1G, 2D, 2E, 2F, 2G (d) 1J, 1K, 1L, 1M, 2J, 2K, 2L, 2M	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is associated DQa pins; Byte "b" is associated with DQb pins. For the x32 and x36 versions, Byte "a" is associated with DQa pins; Byte "b" is associated with DQbs; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
11C 1N – –	11N 11C 1C 1N	NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Parity Data I/Os: On the x32 version, these are no function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd. No function pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.

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FBGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
1H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	1H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
2H, 4C, 4N, 5C, 5D, 5E 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N	2H, 4C, 4N, 5C, 5D, 5E 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N	V_{SS}	Supply	Ground: GND.
7P	7P	TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
1A, 1B, 1C, 1D, 1E, 1F, 1G, 1P, 2C, 2J, 2K, 2L, 2M, 2N, 2P, 2R, 3H, 4B, 5A, 5N, 9H, 10C, 10D, 10E, 10F, 10G, 10H, 10N, 11B, 11J, 11K, 11L, 11M, 11N	1A, 1B, 1P, 2C, 2N, 2P, 2R, 3H, 5N, 9H, 10C, 10H, 10N, 11A, 11B	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

PIN LAYOUT (TOP VIEW)
119-PIN BGA

x18

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	ADSP#	SA	SA	VDDQ
B	NC	SA	SA	ADSC#	SA	SA	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	CE#	VSS	NC	DQa
F	VDDQ	NC	VSS	OE# (G#)	VSS	DQa	VDDQ
G	NC	DQb	BWb#	ADV#	VSS	NC	DQa
H	DQb	NC	VSS	GW#	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	BWa#	DQa	NC
M	VDDQ	DQb	VSS	BWE#	VSS	NC	VDDQ
N	DQb	NC	VSS	SA1	VSS	DQa	NC
P	NC	DQPb	VSS	SA0	VSS	NC	DQa
R	NC	SA	MODE (LBO#)	VDD	VDD	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

TOP VIEW

x32/x36

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	ADSP#	SA	SA	VDDQ
B	NC	SA	SA	ADSC#	SA	SA	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQc	NF/DQPc[1]	VSS	NC	VSS	NF/DQPb[1]	DQb
E	DQc	DQc	VSS	CE#	VSS	DQb	DQb
F	VDDQ	DQc	VSS	OE# (G#)	VSS	DQb	VDDQ
G	DQc	DQc	BWc#	ADV#	BWb#	DQb	DQb
H	DQc	DQc	VSS	GW#	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	BWd#	NC	BWa#	DQa	DQa
M	VDDQ	DQd	VSS	BWE#	VSS	DQa	VDDQ
N	DQd	DQd	VSS	SA1	VSS	DQa	DQa
P	DQd	NF/DQPd[1]	VSS	SA0	VSS	NF/DQPa[1]	DQa
R	NC	SA	MODE (LBO#)	VDD	VDD	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

TOP VIEW

NOTE: 1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.

BGA PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4P 4N 2A, 3A, 5A, 6A, 2B, 3B, 5B, 6B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	4P 4N 2A, 3A, 5A, 6A, 2B, 3B, 5B, 6B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5L 3G – –	5L 5G 3G 3L	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQ pins and DQPa; BWb# controls DQb pins and DQPb. For the x32 and x36 versions, BWa# controls DQ pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. Parity is only available on the x18 and x36 versions.
4M	4M	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
4H	4H	GW#	Input	Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
4K	4K	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	4E	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
7T	7T	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
NA	NA	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
4F	4F	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
4G	4G	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on ADV# effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

(continued on next page)

BGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4A	4A	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
4B	4B	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
3R	3R	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on MODE selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
2U 3U 4U	2U 3U 4U	TMS TDI TCK	Input	IEEE 1149.1 test inputs: JEDEC-standard 2.5V I/O levels. These pins may be left not connected if the JTAG function is not used in the circuit.
(a) 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M	(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins. For the x32 and x36 versions, Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
5U	5U	TDO	Output	IEEE 1149.1 test outputs: JEDEC-standard 2.5V I/O level.
6D 2P – –	6P 6D 2D 2P	NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Parity Data I/Os: On the x32 version, these are no function (NC). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd. No function pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.

(continued on next page)

BGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
3D, 3E, 3F, 3H, 3K, 3L, 3M, 3N, 3P, 5D, 5E, 5F, 5G, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Supply	Ground: GND.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)

FUNCTION	GW#	BWE#	BWa#	BWb#
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte “a”	H	L	L	H
WRITE Byte “b”	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)

FUNCTION	GW#	BWE#	BWa#	BWb#	BWc#	BWd#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte “a”	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

NOTE: Using BWE# and BWa# through BWd#, any one or more bytes may be written.

TRUTH TABLE

(Notes 1-8)

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
DESELECT Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:
1. X means "Don't Care." # means active LOW. H means logic HIGH. L means logic LOW.
2. For WRITE#, L means any one or more byte write enable signals (BWa#, BWb#, BWc#, or BWd#), and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
3. BWa# enables WRITEs to DQa and DQPa. BWb# enables WRITEs to DQb and DQPb. BWc# enables WRITEs to DQc and DQPc. BWd# enables WRITEs to DQd and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

3.3V V_{DD}, ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} .... -0.5V to +4.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS} .... -0.5V to +4.6V
V_{IN} (DQx) .... -0.5V to $V_{DD}Q$ + 0.5V
V_{IN} (inputs) .... -0.5V to V_{DD} + 0.5V
Storage Temperature (TQFP) .... -55ºC to +150ºC
Storage Temperature (FBGA) .... -55ºC to +125ºC
Junction Temperature** .... +150ºC
Short Circuit Output Current 100mA

2.5V V_{DD}, ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} .... -0.3V to +3.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS} .... -0.3V to +3.6V
V_{IN} (DQx) .... -0.3V to $V_{DD}Q$ + 0.3V
V_{IN} (inputs) .... -0.3V to V_{DD} + 0.3V
Storage Temperature (TQFP) .... -55ºC to +150ºC
Storage Temperature (FBGA) .... -55ºC to +125ºC
Junction Temperature** .... +150ºC
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V V_{DD}, 3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

($0°C \le T_A \le +110°C$; V_{DD} = +3.3V ±0.165V; $V_{DD}Q$ = +3.3V ±0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{DD}$	I_{LI}	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, $0V \le V_{IN} \le V_{DD}$	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4	–	V	1, 4
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}	–	0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	3.465	V	1, 5

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. For 3.3V V_{DD}:
   Overshoot: $V_{IH} \le +4.6V$ for $t \le {}^tKC/2$ for $I \le 20mA$
   Undershoot: $V_{IL} \ge -0.7V$ for $t \le {}^tKC/2$ for $I \le 20mA$
   Power-up: $V_{IH} \le +3.6V$ and $V_{DD} \le 3.135V$ for $t \le 200ms$
   For 2.5V V_{DD}:
   Overshoot: $V_{IH} \le +3.6V$ for $t \le {}^tKC/2$ for $I \le 20mA$
   Undershoot: $V_{IL} \ge -0.5V$ for $t \le {}^tKC/2$ for $I \le 20mA$
   Power-up: $V_{IH} \le +2.65V$ and $V_{DD} \le 2.375V$ for $t \le 200ms$
3. MODE has an internal pull-up, and input leakage = ±10µA.
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the stated DC values. AC I/O curves are available upon request.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be connected together.

3.3V V_{DD}, 2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

($0°C \leq T_A \leq +110°C$; V_{DD} = +3.3V ±0.165V; $V_{DD}Q$ = +2.5V ±0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{DD}$	I_{LI}	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, $0V \leq V_{IN} \leq V_{DD}Q$ (DQx)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1, 4
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1, 4
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1, 4
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.625	V	1

2.5V V_{DD}, 2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

($0°C \leq T_A \leq +110°C$; V_{DD} = +2.5V ±0.125V; $V_{DD}Q$ = +2.5V ±0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{DD}$	I_{LI}	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, $0V \leq V_{IN} \leq V_{DD}Q$ (DQx)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1, 4
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1, 4
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1, 4
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1, 4
Supply Voltage		V_{DD}	2.375	2.625	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.625	V	1

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. For 3.3V V_{DD}:
   Overshoot: $V_{IH} \leq +4.6V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.7V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +3.6V$ and $V_{DD} \leq 3.135V$ for $t \leq 200ms$
   For 2.5V V_{DD}:
   Overshoot: $V_{IH} \leq +3.6V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.5V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +2.65V$ and $V_{DD} \leq 2.375V$ for $t \leq 200ms$
3. MODE has an internal pull-up, and input leakage = ±10µA.
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 4 for 2.5V I/O. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. This parameter is sampled.

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	46	°C/W	1
Thermal Resistance (Junction to Top of Case)		θ_{JC}	2.8	°C/W	1

BGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	1
Junction to Case (Top)		θ_{JC}	9	°C/W	1
Junction to Pins (Bottom)		θ_{JB}	17	°C/W	1

FBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	1
Junction to Case (Top)		θ_{JC}	9	°C/W	1
Junction to Pins (Bottom)		θ_{JB}	17	°C/W	1

NOTE: 1. This parameter is sampled.

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz; V_{DD} = 3.3V	C_I	4.8	6.0	pF	1
Input/Output Capacitance (DQ)		C_O	3.8	4.5	pF	1
Address Capacitance		C_A	4.7	5.5	pF	1
Clock Capacitance		C_{CK}	4.5	5.0	pF	1

BGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	4	7	pF	1
Input/Output Capacitance (DQ)		C_O	4.5	5.5	pF	1
Address Capacitance		C_A	4	7	pF	1
Clock Capacitance		C_{CK}	4.5	5.5	pF	1

FBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	2.5	3.5	pF	1
Output Capacitance (Q)		C_O	4	5	pF	1
Clock Capacitance		C_{CK}	2.5	3.5	pF	1

NOTE: 1. This parameter is sampled.

3.3V V_{DD}, I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS (512K x 32/36)

(Note 1, unless otherwise noted)(0°C ≤ T_A ≤ +110°C)

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -7.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	TBD	675	525	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	TBD	225	175	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	TBD	30	30	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	TBD	100	100	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	TBD	225	175	mA	3, 4

NOTE:
1. $V_{DD}Q$ = +3.3V or +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 3.3V, 25°C, and 10ns cycle time.

2.5V V_{DD}, I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS (512K x 32/36)

(Note 1, unless otherwise noted)(0°C ≤ T_A ≤ +110°C)

				MAX				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	TBD	625	515	400	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	TBD	210	175	135	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	TBD	25	25	25	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	TBD	80	80	80	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	TBD	210	175	135	mA	3, 4

NOTE:
1. $V_{DD}Q$ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

3.3V V_{DD}, I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS (1 MEG x 18)

(Note 1, unless otherwise noted)(0°C ≤ T_A ≤ +110°C)

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -7.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	TBD	510	400	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	TBD	170	140	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	TBD	25	25	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	TBD	75	75	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	TBD	170	140	mA	3, 4

NOTE:
1. $V_{DD}Q$ = +3.3V or +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 3.3V, 25°C, and 10ns cycle time.

2.5V V_{DD}, I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS (1 MEG x 18)

(Note 1, unless otherwise noted)(0°C ≤ T_A ≤ +110°C)

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -6	MAX -7.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	TBD	470	390	305	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	TBD	160	130	110	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	TBD	20	20	20	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	TBD	60	60	60	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	TBD	160	130	110	mA	3, 4

NOTE:
1. $V_{DD}Q$ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Notes 1, 2 unless otherwise noted) (0°C ≤ T_A ≤ +110°C)

DESCRIPTION	SYMBOL	-6[3]		-7.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time	^tKC	6.0		7.5		10		ns	
Clock frequency	^fKF		166		133		100	MHz	
Clock HIGH time	^tKH	2.3		2.5		3.0		ns	4
Clock LOW time	^tKL	2.3		2.5		3.0		ns	4
Output Times									
Clock to output valid	^tKQ		3.5		4.0		5.0	ns	
Clock to output invalid	^tKQX	1.5		1.5		1.5		ns	5
Clock to output in Low-Z	^tKQLZ	0		0		0		ns	5, 6, 7, 8
Clock to output in High-Z	^tKQHZ		3.5		4.2		5.0	ns	5, 6, 7, 8
OE# to output valid	^tOEQ		3.5		4.2		5.0	ns	9
OE# to output in Low-Z	^tOELZ	0		0		0		ns	5, 6, 7, 8
OE# to output in High-Z	^tOEHZ		3.5		4.2		4.5	ns	5, 6, 7, 8
Setup Times									
Address	^tAS	1.5		1.5		2.0		ns	10, 11
Address status (ADSC#, ADSP#)	^tADSS	1.5		1.5		2.0		ns	10, 11
Address advance (ADV#)	^tAAS	1.5		1.5		2.0		ns	10, 11
Write signals (BWa#-BWd#, BWE#, GW#)	^tWS	1.5		1.5		2.0		ns	10, 11
Data-in	^tDS	1.5		1.5		2.0		ns	10, 11
Chip enables (CE#, CE2#, CE2)	^tCES	1.5		1.5		2.0		ns	10, 11
Hold Times									
Address	^tAH	0.5		0.5		0.5		ns	10, 11
Address status (ADSC#, ADSP#)	^tADSH	0.5		0.5		0.5		ns	10, 11
Address advance (ADV#)	^tAAH	0.5		0.5		0.5		ns	10, 11
Write signals (BWa#-BWd#, BWE#, GW#)	^tWH	0.5		0.5		0.5		ns	10, 11
Data-in	^tDH	0.5		0.5		0.5		ns	10, 11
Chip enables (CE#, CE2#, CE2)	^tCEH	0.5		0.5		0.5		ns	10, 11

NOTE:
1. Test conditions as specified with the output loading shown in Figure 1 for +3.3V I/O ($V_{DD}Q$ = +3.3V ±0.165V) and Figure 3 for 2.5V I/O ($V_{DD}Q$ = +2.5V ±0.125V) unless otherwise noted.
2. If V_{DD} = +3.3V, then $V_{DD}Q$ = +3.3V or +2.5V. If V_{DD} = +2.5V, then $V_{DD}Q$ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and $V_{DD}Q$.
3. The -6 speed grade is available in 2.5V V_{DD} with 2.5V $V_{DD}Q$ only.
4. Measured as HIGH above V_{IH} and LOW below V_{IL}.
5. This parameter is measured with the output loading shown in Figure 2.
6. This parameter is sampled.
7. Transition is measured ±500mV from steady state voltage.
8. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
9. OE# is a "Don't Care" when a byte write enable is sampled LOW.
10. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ADSC# or ADV# LOW or ADSP# LOW for the required setup and hold times.
11. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.

3.3V V_{DD}, 3.3V I/O AC TEST CONDITIONS

Input pulse levels	$V_{IH} = (V_{DD}/2.2) + 1.5V$
	$V_{IL} = (V_{DD}/2.2) - 1.5V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2.2$
Output reference levels	$V_{DD}Q/2.2$
Output load	See Figures 1 and 2

3.3V V_{DD}, 2.5V I/O AC TEST CONDITIONS

Input pulse levels	$V_{IH} = (V_{DD}/2.64) + 1.25V$
	$V_{IL} = (V_{DD}/2.64) - 1.25V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2.64$
Output reference levels	$V_{DD}Q/2$
Output load	See Figures 3 and 4

2.5V V_{DD}, 2.5V I/O AC TEST CONDITIONS

Input pulse levels	$V_{IH} = (V_{DD}/2) + 1.25V$
	$V_{IL} = (V_{DD}/2) - 1.25V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2$
Output reference levels	$V_{DD}Q/2$
Output load	See Figures 3 and 4

LOAD DERATING CURVES

Micron 1 Meg x 18, 512K x 32 and 512K x 36 SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

3.3V I/O Output Load Equivalents

Figure 1

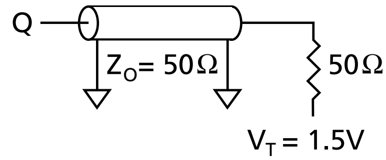
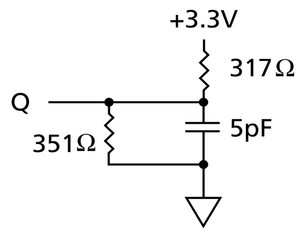


Figure 2



2.5V I/O Output Load Equivalents

Figure 3

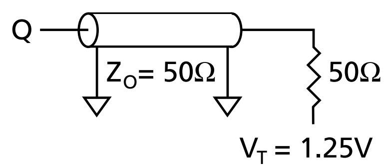
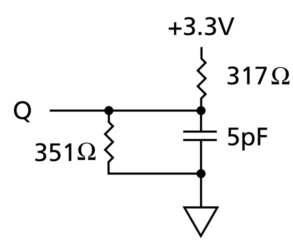


Figure 4



SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

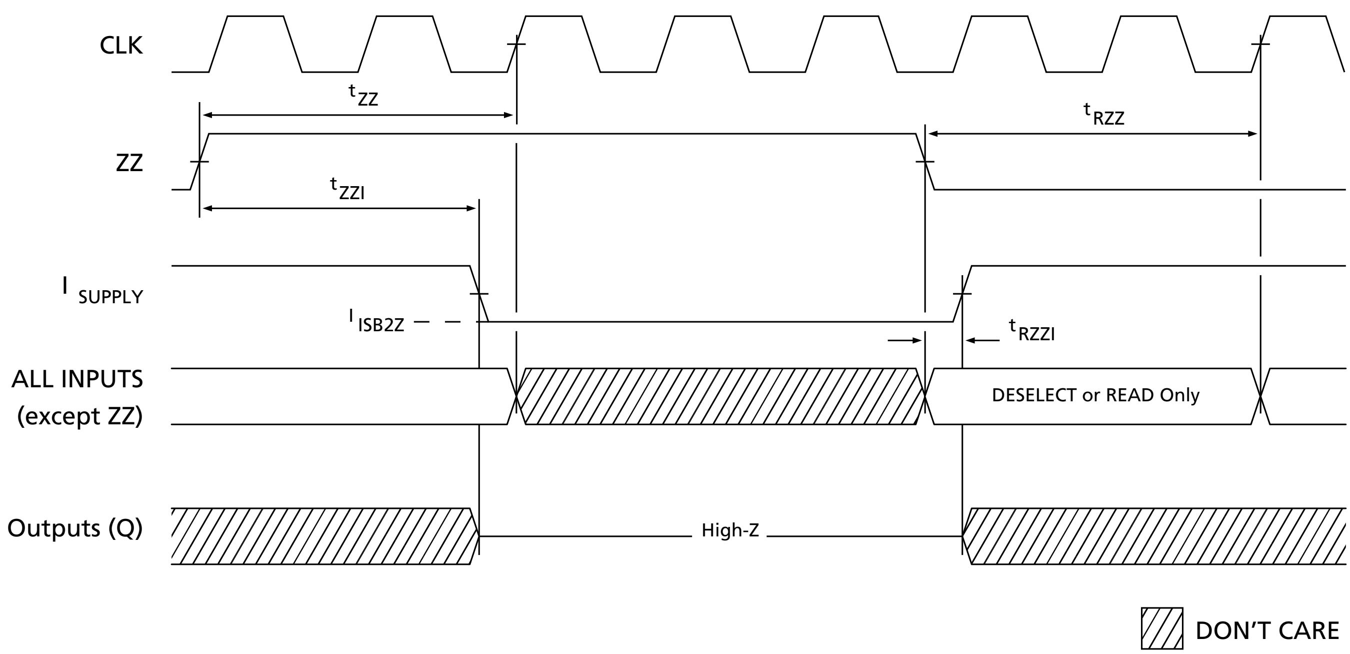
ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time ^tZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

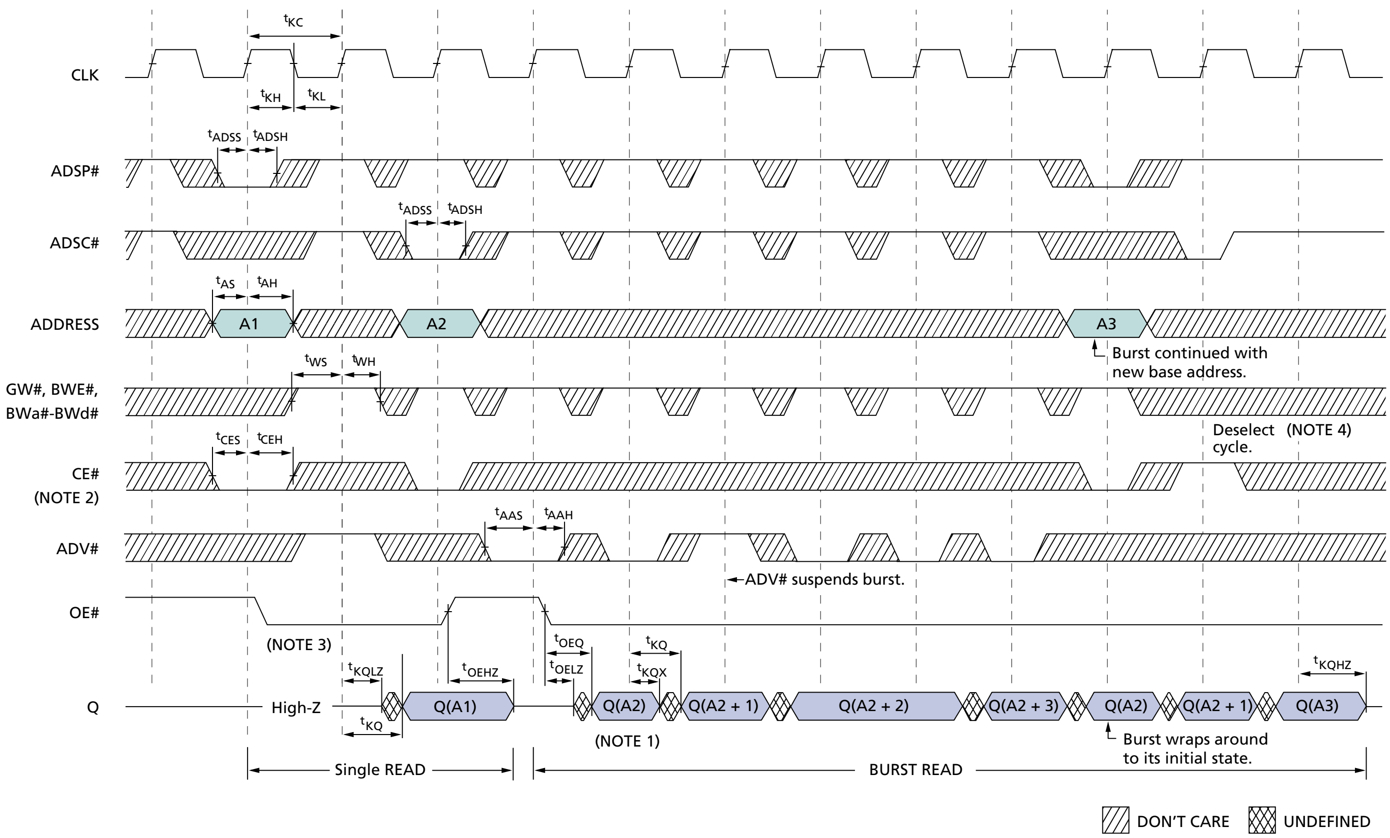
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		10	mA	
ZZ active to input ignored		^tZZ		$2(^tKC)$	ns	1
ZZ inactive to input sampled		^tRZZ	$2(^tKC)$		ns	1
ZZ active to snooze current		^tZZI		$2(^tKC)$	ns	1
ZZ inactive to exit snooze current		^tRZZI	0		ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



READ TIMING[3]



READ TIMING PARAMETERS

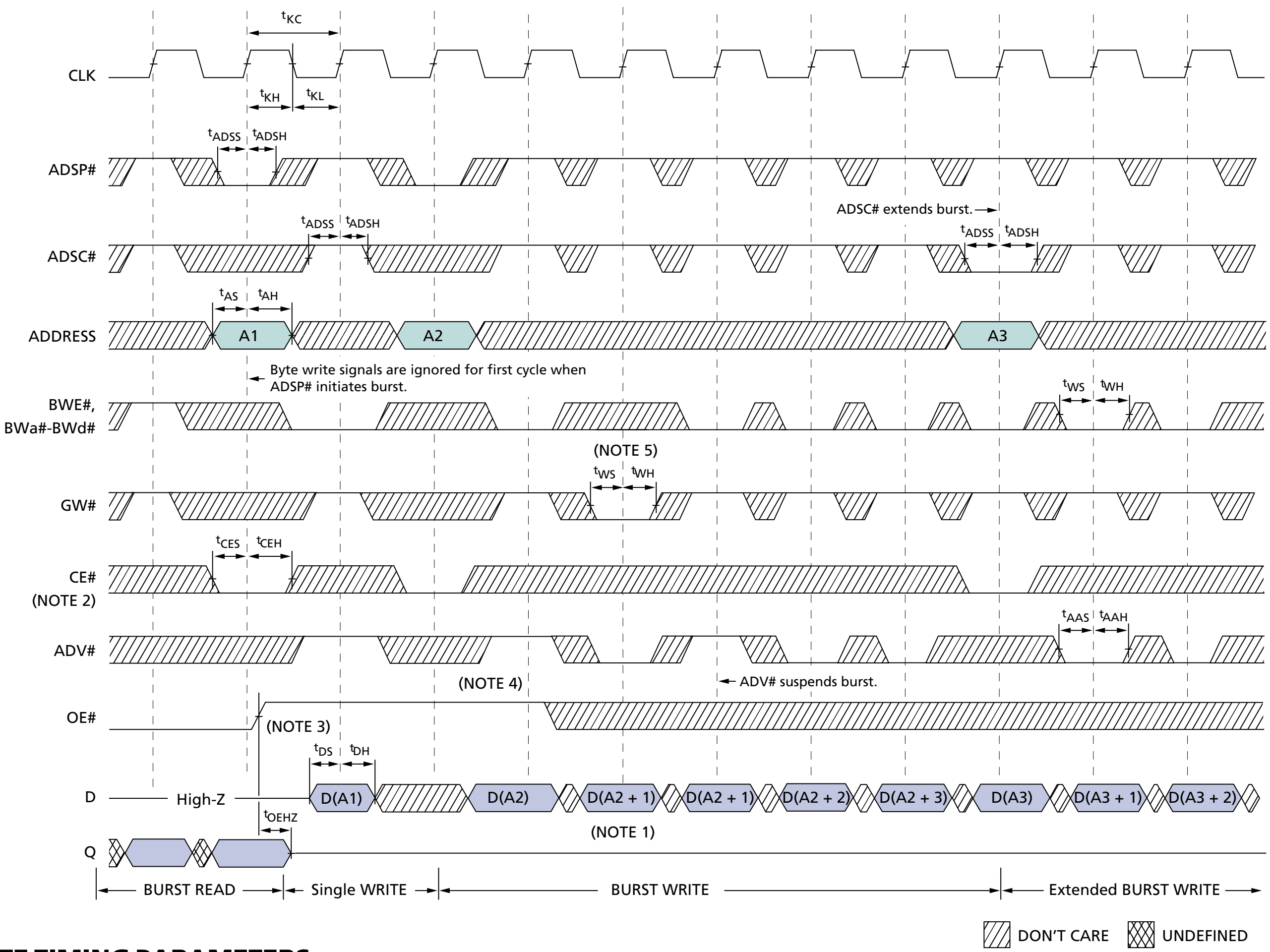
SYMBOL	-6* MIN	-6* MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKC	6.0		7.5		10		ns
tKF		166		133		100	MHz
tKH	2.3		2.5		3.0		ns
tKL	2.3		2.5		3.0		ns
tKQ		3.5		4.0		5.0	ns
tKQX	1.5		1.5		1.5		ns
tKQLZ	0		0		1.0		ns
tKQHZ		3.5		4.2		5.0	ns
tOEQ		3.5		4.2		5.0	ns
tOELZ	0		0		0		ns
tOEHZ		3.5		4.2		4.5	ns

SYMBOL	-6* MIN	-6* MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tAS	1.5		1.5		2.0		ns
tADSS	1.5		1.5		2.0		ns
tAAS	1.5		1.5		2.0		ns
tWS	1.5		1.5		2.0		ns
tCES	1.5		1.5		2.0		ns
tAH	0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		ns
tAAH	0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		ns

*The -6 speed grade available in 2.5V V_{DD} and I/O only.

NOTE:
1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
4. Outputs are disabled within two clock cycles after deselect.

WRITE TIMING



WRITE TIMING PARAMETERS

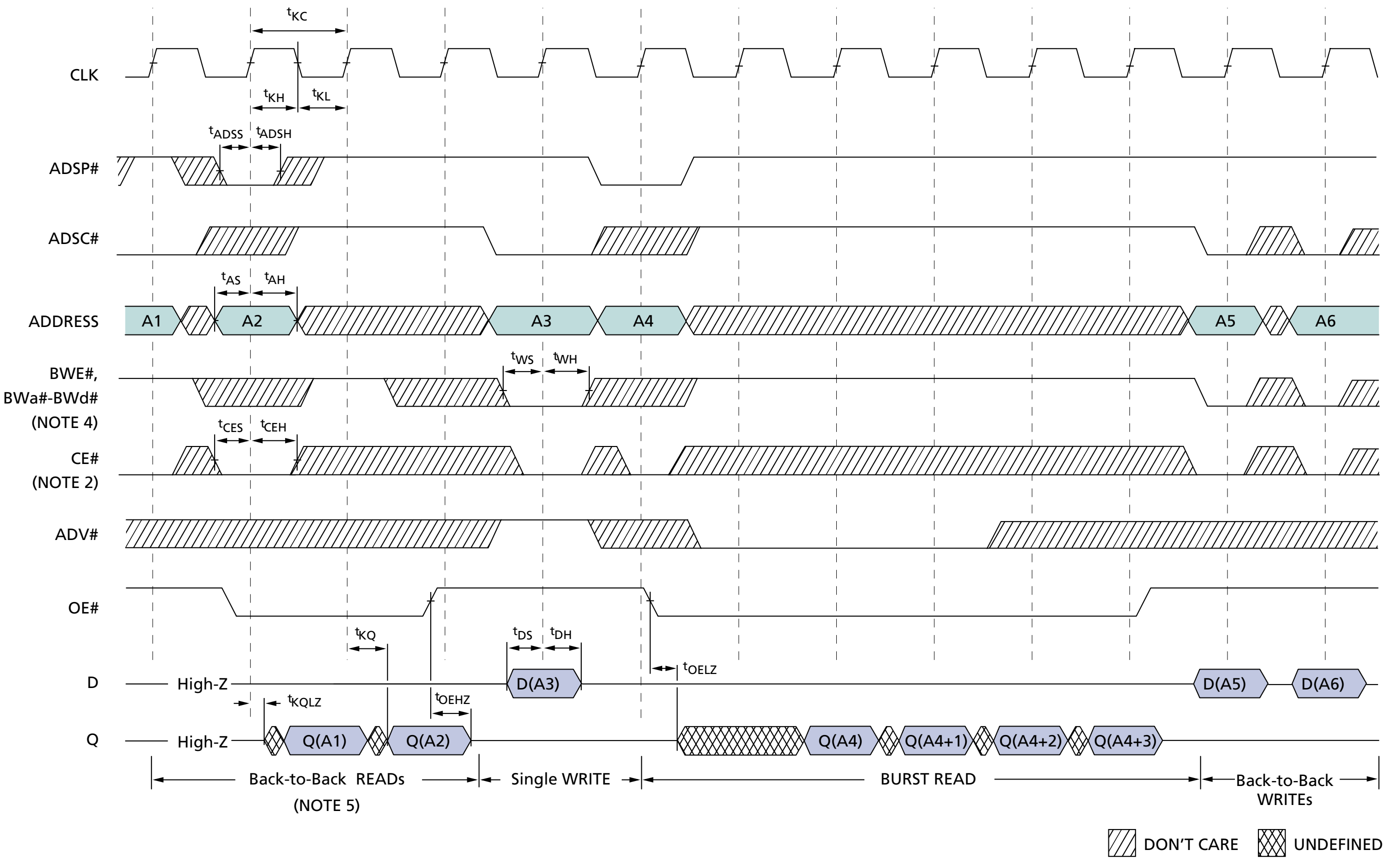
SYMBOL	-6* MIN	-6* MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKC	6.0		7.5		10		ns
fKF		166		133		100	MHz
tKH	2.3		2.5		3.0		ns
tKL	2.3		2.5		3.0		ns
tOEHZ	3.5		4.2		4.5	ns	
tAS	1.5		1.5		2.0		ns
tADSS	1.5		1.5		2.0		ns
tAAS	1.5		1.5		2.0		ns
tWS	1.5		1.5		2.0		ns

SYMBOL	-6* MIN	-6* MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tDS	1.5		1.5		2.0		ns
tCES	1.5		1.5		2.0		ns
tAH	0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		ns
tAAH	0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		ns
tDH	0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		ns

*The -6 speed grade available only in 2.5V VDD with 2.5V VDDQ.

NOTE:
1. D(A2) refers to input for address A2. D(A2 + 1) refers to input for the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV# must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW# LOW; or by GW# HIGH, BWE# LOW and BWa#-BWb# LOW for x18 device; or GW# HIGH, BWE# LOW and BWa#-BWd# LOW for x32 and x36 devices.

READ/WRITE TIMING3



READ/WRITE TIMING PARAMETERS

SYMBOL	-6* MIN	-6* MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKC	6.0		7.5		10		ns
tKF		166		133		100	MHz
tKH	2.3		2.5		3.0		ns
tKL	2.3		2.5		3.0		ns
tKQ		3.5		4.0		5.0	ns
tKQLZ	0		0		1.0		ns
tOELZ	0		0		0		ns
tOEHZ		3.5		4.2		4.5	ns
tAS	1.5		1.5		2.0		ns

SYMBOL	-6* MIN	-6* MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tADSS	1.5		1.5		2.0		ns
tWS	1.5		1.5		2.0		ns
tDS	1.5		1.5		2.0		ns
tCES	1.5		1.5		2.0		ns
tAH	0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		ns
tDH	0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		ns

*The -6 speed grade available only in 2.5V V_{DD} with 2.5V $V_{DD}Q$.

NOTE:
1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC#, or ADV# cycle is performed.
4. GW# is HIGH.
5. Back-to-back READs may be controlled by either ADSP# or ADSC#.

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

These pins can be left floating (unconnected), if the JTAG function is not to be implemented. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

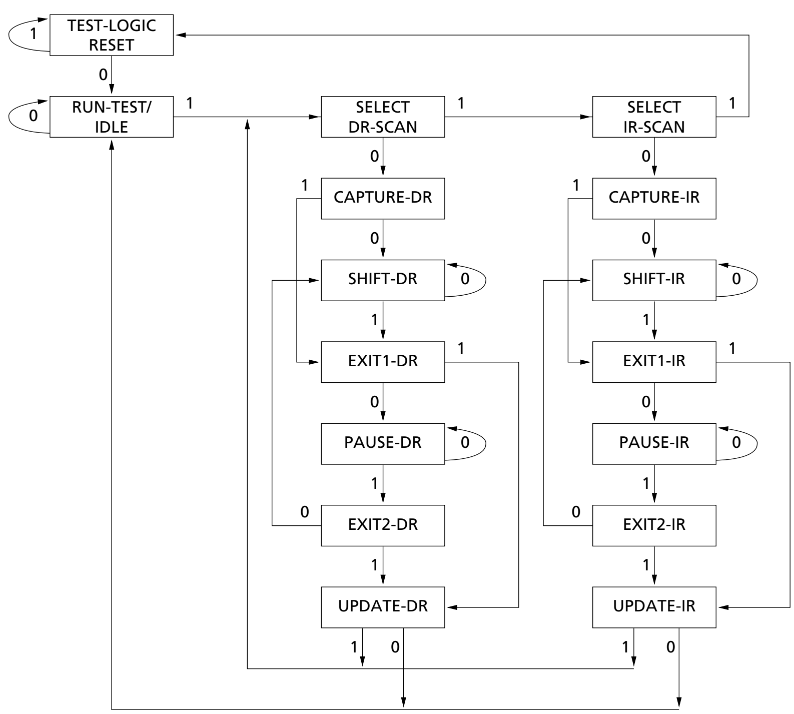
TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 5. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 6.)

Figure 5
TAP Controller State Diagram



NOTE: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TEST DATA-OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 5.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 6.)

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 5. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

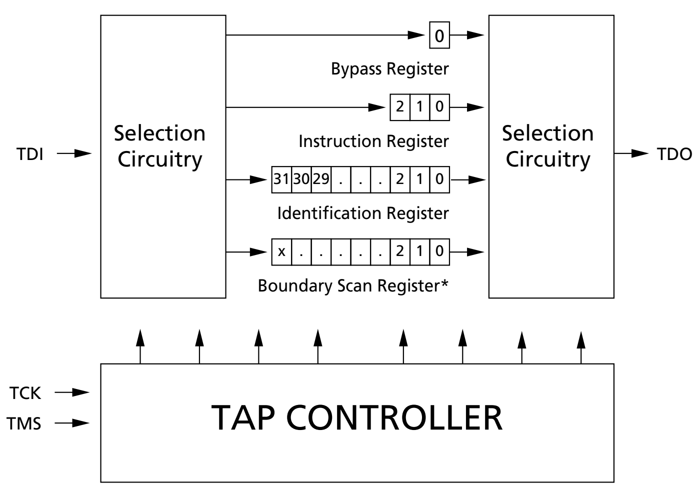
BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for 8Mb and 18Mb Claymore SRAMs. The x36 configuration has a 71-bit-long register, the x32 configuration has a 67-bit-long register, and the x18 configuration has a 52-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the

Figure 6
TAP Controller Block Diagram



*x = 52 for the x18 configuration, x = 67 for the x32 configuration, x = 71 for the x36 configuration.

register is connected to TDI, and the LSB is connected to TDO.

IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

OVERVIEW

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^tCS plus ^tCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

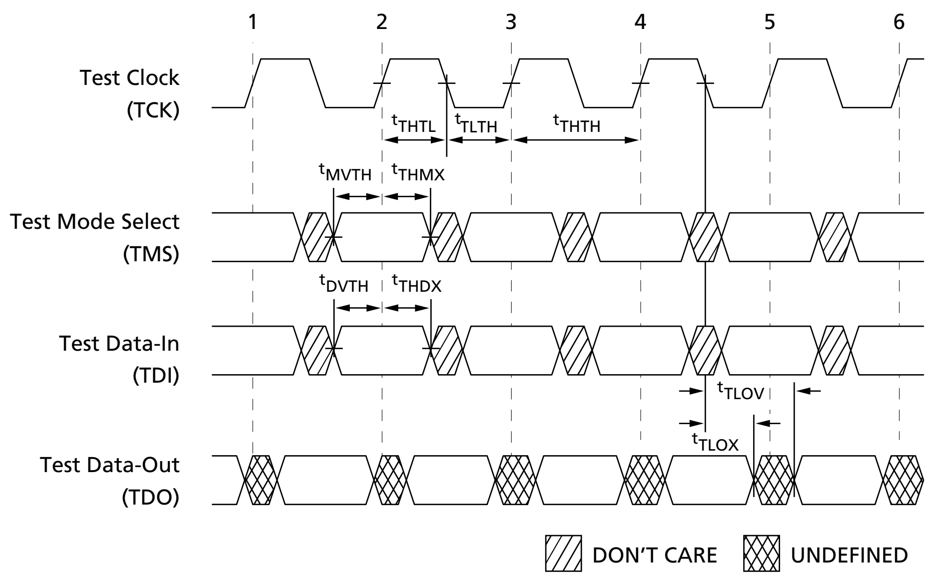
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instruction are not implemented but are reserved for future use. Do not use these instructions.

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) (+20°C ≤ T_J ≤ +100°C; +2.4V ≤ V_{DD} ≤ +2.6V)

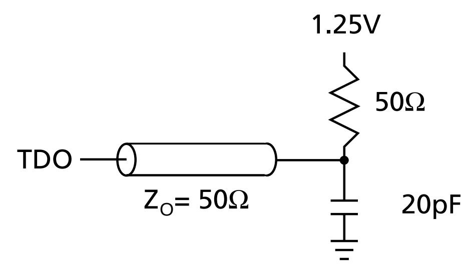
DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 7.

TAP AC TEST CONDITIONS

Input pulse levels	V_{SS} to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V

Figure 7
TAP AC Output Load Equivalent



3.3V V_{DD}, TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +3.135V ≤ V_{DD} ≤ +3.465V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	IL_O	-5.0	5.0	µA	
Output Low Voltage	I_{OLC} = 100µA	V_{OL1}		0.7	V	1
Output Low Voltage	I_{OLT} = 2mA	V_{OL2}		0.8	V	1
Output High Voltage	I_{OHC} = -100µA	V_{OH1}	2.9		V	1
Output High Voltage	I_{OHT} = -2mA	V_{OH2}	2.0		V	1

2.5V V_{DD}, TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	IL_O	-5.0	5.0	µA	
Output Low Voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output Low Voltage	I_{OLT} = 2mA	V_{OL2}		0.7	V	1
Output High Voltage	I_{OHC} = -100µA	V_{OH1}	2.1		V	1
Output High Voltage	I_{OHT} = -2mA	V_{OH2}	1.7		V	1

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} (AC) ≤ V_{DD} + 1.5V for t ≤ $^tKHKH/2$
   Undershoot: V_{IL} (AC) ≥ -0.5V for t ≤ $^tKHKH/2$
   Power-up: V_{IH} ≤ +2.6V and V_{DD} ≤ 2.4V and $V_{DD}Q$ ≤ 1.4V for t ≤ 200ms
   During normal operation, $V_{DD}Q$ must not exceed V_{DD}. Control input signals (such as LD#, R/W#, etc.) may not have pulse widths less than ^tKHKL (MIN) or operate at frequencies exceeding ^fKF (MAX).

IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	512K x 18	DESCRIPTION
REVISION NUMBER (31:28)	xxxx	Reserved for version number.
DEVICE DEPTH (27:23)	00111	Defines depth of 512K or 1Mb words.
DEVICE WIDTH (22:18)	00011	Defines width of x18, x32, or x36 bits.
MICRON DEVICE ID (17:12)	xxxxxx	Reserved for future use.
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE		
Instruction	3		
Bypass	1		
ID	32		
Boundary Scan	x18: 52	x32: 67	x36: 71

INSTRUCTION CODES

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

165-PIN FBGA BOUNDARY SCAN ORDER (x18)

FBGA BIT#	SIGNAL NAME	PIN ID
1	SA	6N
2	SA	11P
3	SA	8P
4	SA	9R
5	SA	9P
6	SA	10R
7	SA	10P
8	SA	11R
9	SA	8R
10	DQa	10M
11	DQa	10L
12	DQa	10K
13	DQa	10J
14	ZZ	11H
15	DQa	11G
16	DQa	11F
17	DQa	11E
18	DQa	11D
19	DQPa	11C
20	SA	11A
21	SA	10B
22	SA	10A
23	ADV#	9A
24	ADSP#	9B
25	ADSC#	8A
26	OE# (G#)	8B
27	BWE#	7A

FBGA BIT#	SIGNAL NAME	PIN ID
28	GWE#	7B
29	CLK	6B
30	CE2#	6A
31	BWa#	5B
32	BWb#	4A
33	CE2	3B
34	CE#	3A
35	SA	2A
36	SA	2B
37	DQb	2D
38	DQb	2E
39	DQb	2F
40	DQb	2G
41	V_{DD}	1H
42	DQb	1J
43	DQb	1K
44	DQb	1L
45	DQb	1M
46	DQPb	1N
47	MODE (LBO#)	1R
48	SA	3P
49	SA	3R
50	SA	4P
51	SA	4R
52	SA1	6P
53	SA0	6R

165-PIN FBGA BOUNDARY SCAN ORDER (x32)

FBGA BIT#	SIGNAL NAME	PIN ID
1	SA	6N
2	SA	11P
3	SA	8P
4	SA	9R
5	SA	9P
6	SA	10R
7	SA	10P
8	SA	11R
9	SA	8R
10	DQa	11M
11	DQa	11L
12	DQa	11K
13	DQa	11J
14	DQa	10M
15	DQa	10L
16	DQa	10K
17	DQa	10J
18	ZZ	11H
19	DQb	11G
20	DQb	11F
21	DQb	11E
22	DQb	11D
23	DQb	10G
24	DQb	10F
25	DQb	10E
26	DQb	10D
27	SA	10B
28	SA	10A
29	ADV#	9A
30	ADSP#	9B
31	ADSC#	8A
32	OE# (G#)	8B
33	BWE#	7A
34	GW#	7B

FBGA BIT#	SIGNAL NAME	PIN ID
35	CLK	6B
36	CE2#	6A
37	BWa#	5B
38	BWb#	5A
39	BWc#	4A
40	BWd#	4B
41	CE2	3B
42	CE2#	3A
43	SA	2A
44	SA	2B
45	DQc	1D
46	DQc	1E
47	DQc	1F
48	DQc	1G
49	DQc	2D
50	DQc	2E
51	DQc	2F
52	DQc	2G
53	V_{DD}	1H
54	DQd	1J
55	DQd	1K
56	DQd	1L
57	DQd	1M
58	DQd	2J
59	DQd	2K
60	DQd	2L
61	DQd	2M
62	MODR (LBO#)	1R
63	SA	3P
64	SA	3R
65	SA	4P
66	SA	4R
67	SA1	6P
68	SA0	6R

165-PIN FBGA BOUNDARY SCAN ORDER (x36)

FBGA BIT#	SIGNAL NAME	PIN ID
1	SA	6N
2	SA	11P
3	SA	8P
4	SA	9R
5	SA	9P
6	SA	10R
7	SA	10P
8	SA	11R
9	SA	8R
10	NF/DQPa	11N
11	DQa	11M
12	DQa	11L
13	DQa	11K
14	DQa	11J
15	DQa	10M
16	DQa	10L
17	DQa	10K
18	DQa	10J
19	ZZ	11H
20	DQb	11G
21	DQb	11F
22	DQb	11E
23	DQb	11D
24	DQb	10G
25	DQb	10F
26	DQb	10E
27	DQb	10D
28	NF/DQPb	11C
29	SA	10B
30	SA	10A
31	ADV#	9A
32	ADSP#	9B
33	ADSC#	8A
34	OE# (G#)	8B
35	BWE#	7A
36	GW#	7B

FBGA BIT#	SIGNAL NAME	PIN ID
37	CLK	6B
38	CE2#	6A
39	BWa#	5B
40	BWb#	5A
41	BWc#	4A
42	BWd#	4B
43	CE2	3B
44	CE2#	3A
45	SA	2A
46	SA	2B
47	NF/DQPc	1C
48	DQc	1D
49	DQc	1E
50	DQc	1F
51	DQc	1G
52	DQc	2D
53	DQc	2E
54	DQc	2F
55	DQc	2G
56	V_{DD}	1H
57	DQd	1J
58	DQd	1K
59	DQd	1L
60	DQd	1M
61	DQd	2J
62	DQd	2K
63	DQd	2L
64	DQd	2M
65	NF/DQPd	1N
66	MODR (LBO#)	1R
67	SA	3P
68	SA	3R
69	SA	4P
70	SA	4R
71	SA1	6P
72	SA0	6R

119-PIN PBGA BOUNDARY SCAN ORDER (x18)

BGA BIT#	SIGNAL NAME	PIN ID
1	SA	2T
2	SA	6R
3	SA	5T
4	SA	3B
5	SA	5B
6	SA	5C
7	SA	6C
8	DQa	7P
9	DQa	6N
10	DQa	6L
11	DQa	7K
12	ZZ	7T
13	DQa	6H
14	DQa	7G
15	DQa	6F
16	DQa	7E
17	DQPa	6D
18	SA	6T
19	SA	6A
20	SA	5A
21	ADV#	4G
22	ADSP	4A
23	ADSC#	4B
24	OE# (G#)	4F
25	BWE#	4M
26	GW#	4H
27	CLK	4K
28	SA	6B
29	BWa#	5L
30	BWb#	3G
31	SA	2B
32	CE#	4E
33	SA	3A
34	SA	2A
35	DQb	1D
36	DQb	2E
37	DQb	2G
38	DQb	1H
39	V_{DD}	5R
40	DQb	2K
41	DQb	1L
42	DQb	2M
43	DQb	1N
44	DQPb	2P
45	MODE (LBO#)	3R
46	SA	2C
47	SA	3C
48	SA	2R
49	SA	3T
50	SA1	4N
51	SA0	4P

119-PIN PBGA BOUNDARY SCAN ORDER (x32)

BGA BIT#	SIGNAL NAME	PIN ID
1	SA	4T
2	SA	6R
3	SA	5T
4	SA	3B
5	SA	5B
6	SA	5C
7	SA	6C
8	DQa	7N
9	DQa	6M
10	DQa	7L
11	DQa	6K
12	DQa	7P
13	DQa	6N
14	DQa	6L
15	DQa	7K
16	ZZ	7T
17	DQb	6H
18	DQb	7G
19	DQb	6F
20	DQb	7E
21	DQb	6E
22	DQb	7H
23	DQb	7D
24	DQb	6G
25	SA	6A
26	SA	5A
27	ADV#	4G
28	ADSP#	4A
29	ADSC#	4B
30	OE# (G#)	4F
31	BWE#	4M
32	GW#	4H
33	CLK	4K

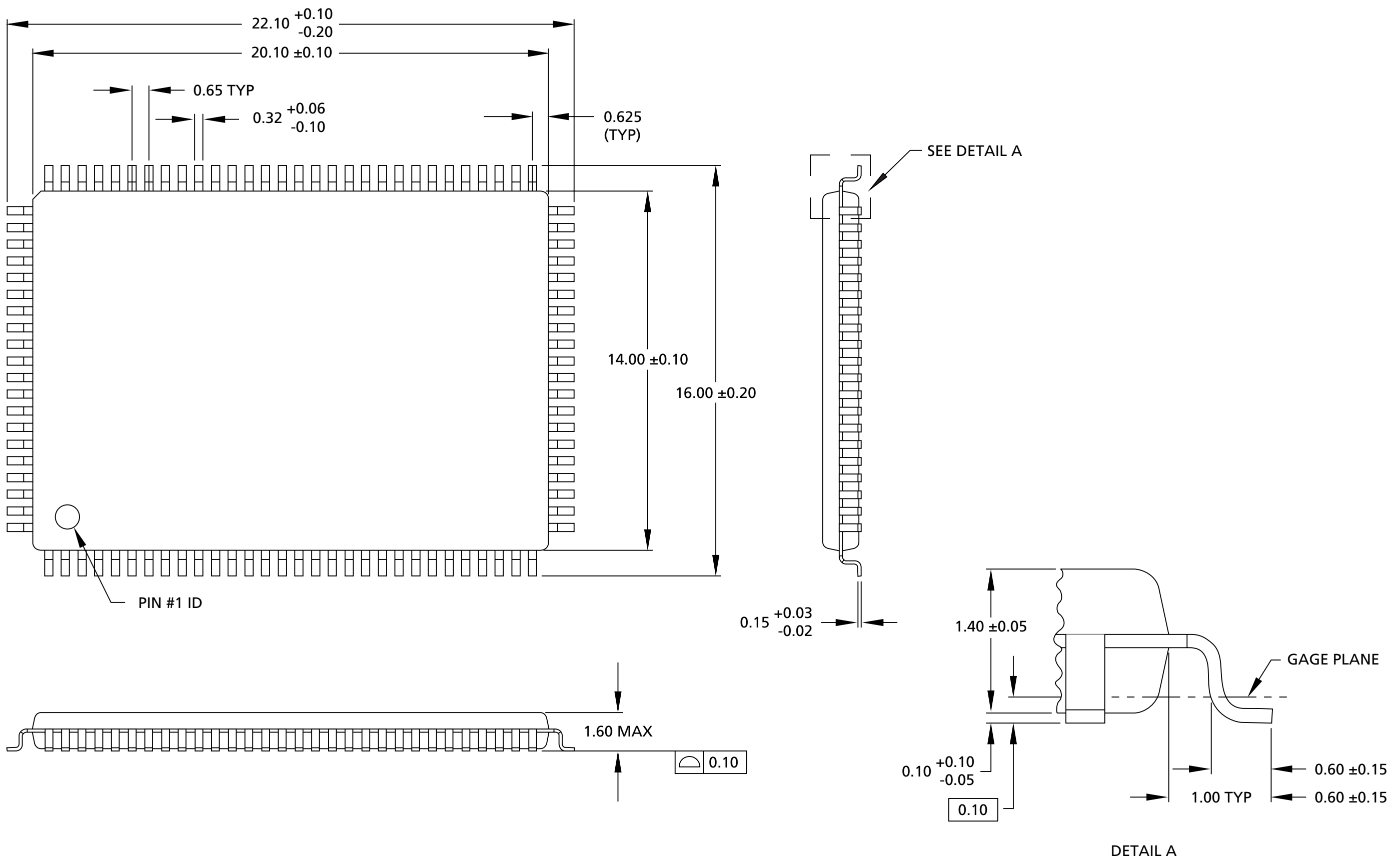
BGA BIT#	SIGNAL NAME	PIN ID
34	SA	6B
35	BWa#	5L
36	BWb#	5G
37	BWc#	3G
38	BWd#	3L
39	SA	2B
40	CE#	4E
41	SA	3A
42	SA	2A
43	DQc	1E
44	DQc	2F
45	DQc	1G
46	DQc	2H
47	DQc	1D
48	DQc	2E
49	DQc	2G
50	DQc	1H
51	V_{DD}	5R
52	DQd	2K
53	DQd	1L
54	DQd	2M
55	DQd	1N
56	DQd	1P
57	DQd	1K
58	DQd	2L
59	DQd	2N
60	MODE (LBO#)	3R
61	SA	2C
62	SA	3C
63	SA	2R
64	SA	3T
65	SA1	4N
66	SA0	4P

119-PIN PBGA BOUNDARY SCAN ORDER (x36)

BGA BIT#	SIGNAL NAME	PIN ID
1	SA	4T
2	SA	6R
3	SA	5T
4	SA	3B
5	SA	5B
6	SA	5C
7	SA	6C
8	NF/DQPa	6P
9	DQa	7N
10	DQa	6M
11	DQa	7L
12	DQa	6K
13	DQa	7P
14	DQa	6N
15	DQa	6L
16	DQa	7K
17	ZZ	7T
18	DQb	6H
19	DQb	7G
20	DQb	6F
21	DQb	7E
22	DQb	6E
23	DQb	7H
24	DQb	7D
25	DQb	6G
26	NF/DQPb	6D
27	SA	6A
28	SA	5A
29	ADV#	4G
30	ADSP#	4A
31	ADSC#	4B
32	OE# (G#)	4F
33	BWE#	4M
34	GW#	4H
35	CLK	4K

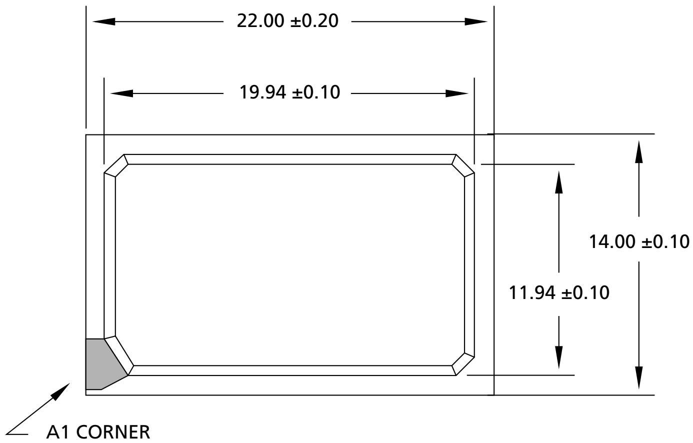
BGA BIT#	SIGNAL NAME	PIN ID
36	SA	6B
37	BWa#	5L
38	BWb#	5G
39	BWc#	3G
40	BWd#	3L
41	SA	2B
42	CE#	4E
43	SA	3A
44	SA	2A
45	NF/DQPc	2D
46	DQc	1E
47	DQc	2F
48	DQc	1G
49	DQc	2H
50	DQc	1D
51	DQc	2E
52	DQc	2G
53	DQc	1H
54	V_{DD}	5R
55	DQd	2K
56	DQd	1L
57	DQd	2M
58	DQd	1N
59	DQd	1P
60	DQd	1K
61	DQd	2L
62	DQd	2N
63	NF/DQPd	2P
64	MODE (LBO#)	3R
65	SA	2C
66	SA	3C
67	SA	2R
68	SA	3T
69	SA1	4N
70	SA0	4P

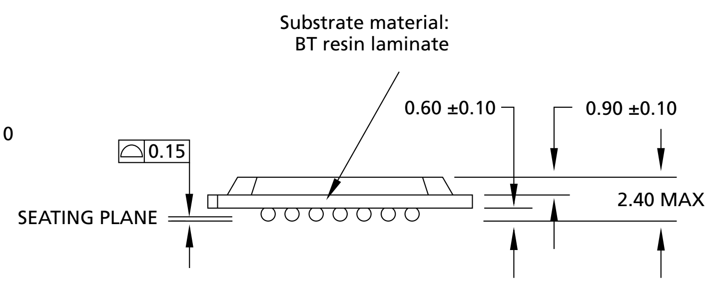
100-PIN PLASTIC TQFP
(JEDEC LQFP)

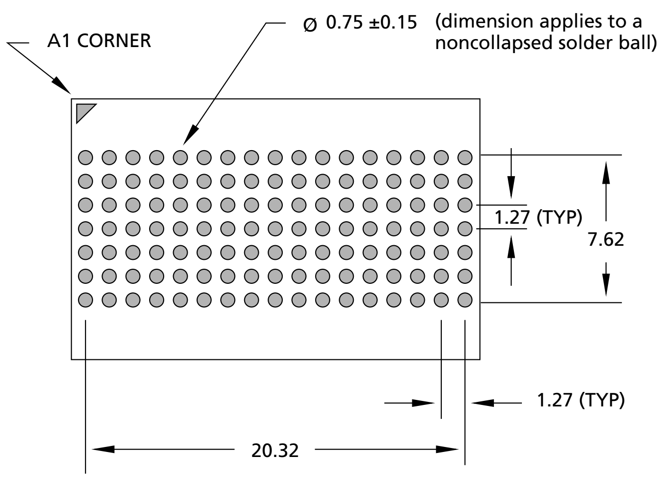


NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

119-PIN BGA

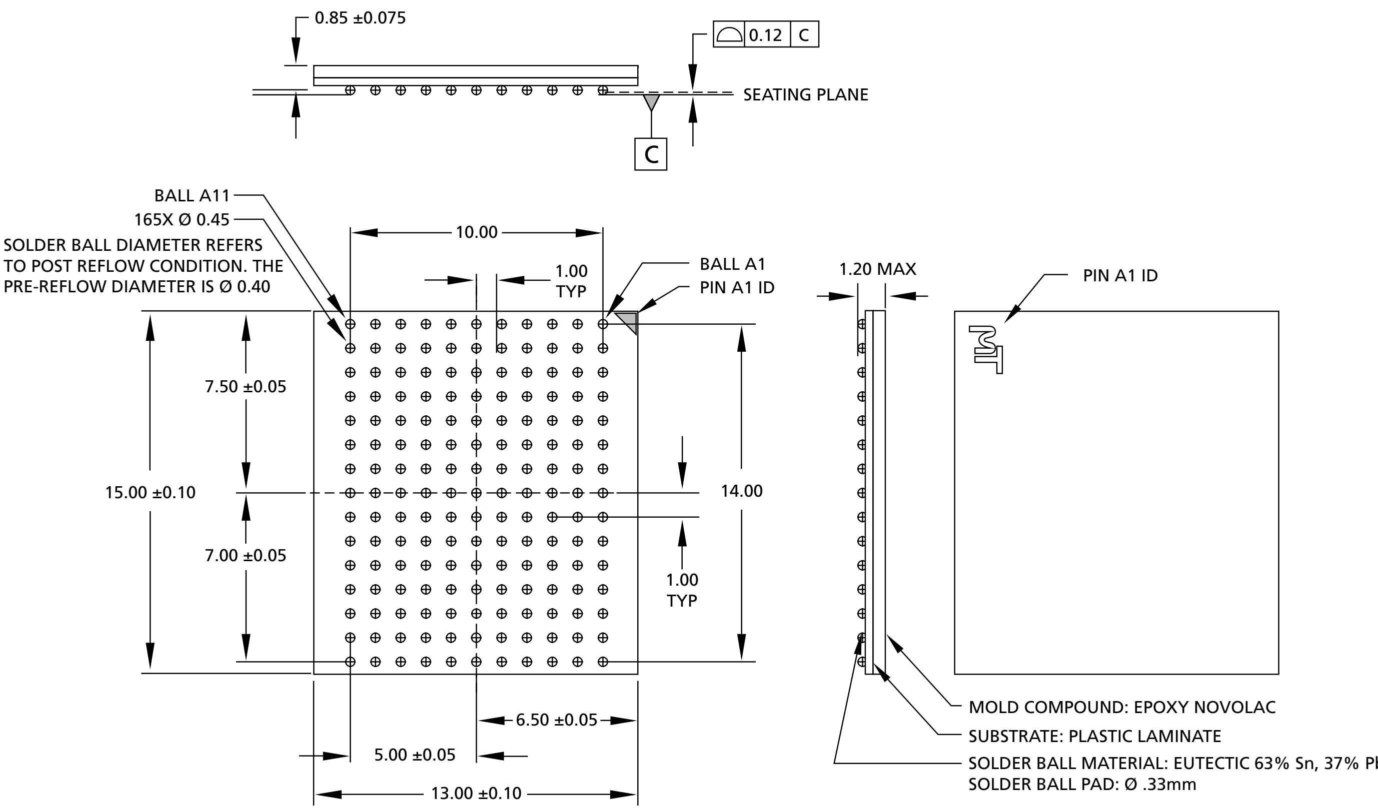






NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Solder ball land pad is 0.6mm.

165-PIN FBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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REVISION HISTORY

Rev. E, Pub. 1/02, ADVANCE Jan/02
- Changed MAX temperature from +70ºC to +110ºC

Rev. D, Pub. 9/01, ADVANCE Sept/01
- Fixed typographical error

Rev. C, Pub. 9/01, ADVANCE Sept/01
- Removed Industrial Temperature references
- Removed -5 speed grade
- Changed I_{DD} tables by splitting x18 and x32/36 configuration
- Changed NC references to NF
- Removed note “Not Recommended for New Design” from 119-pin FBGA
- Changed boundary scan order, 165-pin FBGA, x18 and x32/36
  8P (SA) moved to bit #9 from bit #3
- Increased I_{DD} table values

Rev. 2/01, ADVANCE Feb/24/01
- Added Industrial Temperature note and references
- Changed 16Mb references to 18Mb
- Added -5 speed grade

Rev. 1/01, ADVANCE Jan/10/01
- Added 165-Pin FBGA JTAG Boundary Scan Order
- Added 119-Pin PBGA and references

Rev. 8/00, ADVANCE Aug/22/00
- Removed FBGA Part Marking Guide

Rev. 7/00, ADVANCE Aug/8/00
- Changed FBGA capacitance values
- C_I; TYP 2.5 pF from 4 pF; MAX 3.5 pF from 5 pF
- C_O; TYP 4 pF from 6 pF; MAX 5 pF from 7 pF
- C_{CK}; TYP 2.5 pF from 5 pF; MAX 3.5 pF from 6 pF

Rev. 7/00, ADVANCE July/24/00
- Removed Industrial Temperature references

Rev. 7/00, ADVANCE Jun/28/00
- Added 165-pin FBGA package
- Added FBGA part marking references
- Removed 119-pin PBGA and references
- Added Note: “IT available for -8.5 and -10 speed grades”

Rev. 4/00, ADVANCE Apr/13/00
- Change Pin 14 to NC from V_{DD}
- Added note: ZZ has internal pull-down

Rev. 3/00, ADVANCE Apr/6/00
- Updated Boundary Scan Order

Rev. 1/00, ADVANCE Jan/18/00
- Added ADVANCE status

Rev. 11/99, ADVANCE Nov/11/99
- MT58L1MY18D, Rev. 11/99
- Added BGA JTAG functionality