DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC2762T, μPC2763T

3V-BIAS, MEDIUM-POWER HIGH-FREQUENCY SiMMIC AMPLIFIER FOR MOBILE COMMUNICATIONS

DESCRIPTION

μPC2762T and μPC2763T are silicon monolithic integrated circuits designed for the transmission (TX) stage buffers of mobile communications. The high frequency medium power output is suitable for RF-TX of cellular and cordless telephones. The RF characteristics are specified with wideband operation, but the improved characteristics in narrow band can be also available due to adjustment of external inductor (inductance, Q, etc.). 3 V supply operation is suitable for low voltage systems. Due to the 50 Ω cascadable and mini-mold package, these ICs are suitable for high-density surface mounting.

These ICs are manufactured using NEC's 20 GHz f_T NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this series have excellent performance, uniformity and reliability.

FEATURES

- Supply voltage : V_{CC} = 3.0 V ± 0.3 V
- Medium output power : $P_{O(1dB)}$ = +8.0 dBm TYP. @ 0.9 GHz – μPC2762T
  (with external inductor to gain wideband)
  $P_{O(1dB)}$ = +9.5 dBm TYP. @ 0.9 GHz – μPC2763T
  (with external inductor to gain wideband)
- Wide band operation : μPC2762T – G_P = 13 dB TYP., f_u = 2.9 GHz TYP., μPC2763T – G_P = 20 dB TYP., f_u = 2.4 GHz TYP..
- 50 Ω cascadable : 50 Ω input/output impedance
- High-density surface mounting : 6 pin mini mold package
- Adjacent channel interference : –60 dBc (reference) @ f = 900 MHz, Δf = ±50 kHz, P_O = 4 dBm

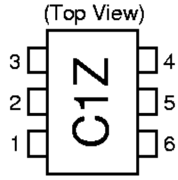
ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKINGS	SUPPLYING FORM	POWER GAIN @ f = 0.9 GHz
μPC2762T-E3	6pin mini mold	C1Z	Embossed tape 8mm wide. Pin 1, 2, 3 face to perforation side of the tape. QTY 3 kp/reel.	13 dB TYP.
μPC2763T-E3		C2A		20 dB TYP.

Note To order evaluation samples, please contact your local NEC sales office. (Part number: μPC2762T, μPC2763T)

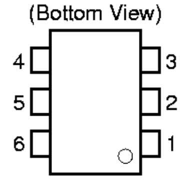
PIN CONNECTION

(Top View)



Marking is an example for μPC2762T

(Bottom View)



Pin No.	Pin name
1	Input
2	GND
3	GND
4	Output
5	GND
6	V_{CC}

Caution: Electro-static sensitive devices

Document No. P11439EJ2V0DS00 (2nd edition)
(Previous No. ID-3587)
Date Published August 1996 P
Printed in Japan

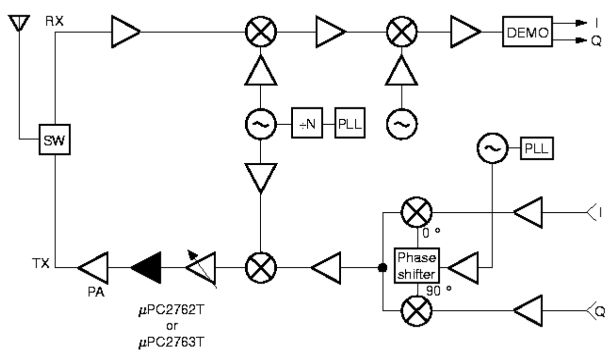
SELECTOR GUIDE (T_A = +25 °C, V_{CC} = V_{out} = 3.0 V, Z_L = Z_S = 50 Ω)

TYPE		PART NUMBER	V_{CC} (V)	I_{CC} (mA)	G_P (dB)	f_u (GHz)	$P_{O(sat)}$ (dBm)	$P_{O(1dB)}$ (dBm)
5 V, 15 dB gain		μPC2708T	5	26	15	2.9	+10	+8.5
5 V, 23 dB gain		μPC2709T	5	26	23	2.3	+11.5	+9
3 V, 20 dB gain		μPC2762T	3	26.5	13	2.9	+9	+8
3 V, 13 dB gain	+9.5 dBm output	μPC2763T	3	27	20	2.4	+11	+9.5
	+11.5 dBm output	μPC2771T	3	36	21	2.1	+12.5	+11.5

Notice Typical performance with TEST CIRCUIT. Please refer to ELECTRICAL CHARACTERISTICS in detail. To know the associated product listed above, please refer to each latest data sheet.

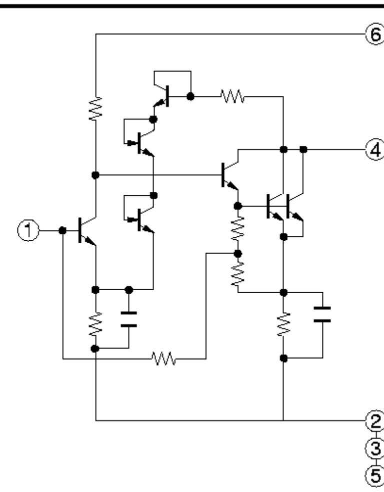
SYSTEM APPLICATION EXAMPLE

Digital cellular telephone



Note The insertion point is different due to the specifications of conjunct devices.
For conjunction with your devices, refer to the data sheets to confirm their conbination.

PIN FUNCTIONS

PIN	SYMBOL	APPLIED VOLTAGE (V)	DESCRIPTION	EQUIVALENT CIRCUIT
1	INPUT	—	High-frequency signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. A multi-feedback circuit is designed to cancel the deviations of h_{FE} and resistance.	
2 3 5	GND	0	Ground pin. Form a ground pattern as wide as possible to minimize ground impedance.	
4	OUTPUT	2.7 - 3.3	High-frequency signal output pin. Connect an inductor between this pin and V_{CC} to supply current to the internal output transistors.	
6	V_{CC}		Power supply pin, which biases the internal input transistor. Excellent RF characteristics are obtained by employing a two-stage amplifier.	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	CONDITIONS
Supply Voltage	V_{CC}	3.6	V	T_A = +25 °C, pins 4 and 6.
Circuit Current	I_{CC}	70	mA	T_A = +25 °C
Power Dissipation	P_D	280	mW	Mounted on 50 × 50 × 1.6 mm double side copper clad epoxy glass PWB T_A = +85 °C
Operating Temperature	$T_{A(opt)}$	–40 to +85	°C	
Storage Temperature	$T_{A(stg)}$	–55 to +150	°C	
Input Power	P_{in}	+10	dBm	T_A = +25 °C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	Notices
Supply Voltage	V_{CC}	2.7	3.0	3.3	V	The same voltage must be applied to pin 4 and 6.
Operating Temperature	$T_{A(opt)}$	–40	+25	+85	°C	

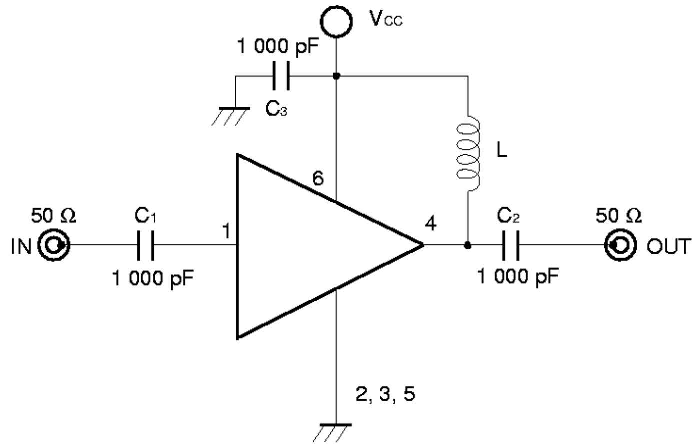
ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = V_{out} = 3.0 V, Z_L = Z_S = 50 Ω)

PARAMETER	SYMBOL	μPC2762T			μPC2763T			UNIT	CONDITION
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Circuit Current	I_{CC}	—	26.5	35	—	27	35	mA	No input signals
Power Gain	G_P	11 11.5	13 14.5	16 17.5	18 16.5	20 19.5	23 22.5	dB	f = 0.9 GHz f = 1.9 GHz
Noise Figure	NF	— —	6.5 7.0	8.0 8.5	— —	5.5 5.5	7.0 7.0	dB	f = 0.9 GHz f = 1.9 GHz
Upper Limit Operating Frequency	f_u	2.7	2.9	—	2.0	2.4	—	GHz	3 dB less than the gain at 0.1 GHz
Isolation	ISL	22 20	27 25	— —	25 24	30 29	— —	dB	f = 0.9 GHz f = 1.9 GHz
Input Return Loss	PL_{in}	6.0 5.5	9.0 8.5	— —	8.0 9.0	11.0 12.0	— —	dB	f = 0.9 GHz f = 1.9 GHz
Output Return Loss	RL_{out}	8.0 9.0	11.0 12.0	— —	5.0 6.0	8.0 9.0	— —	dB	f = 0.9 GHz f = 1.9 GHz
1dB Compression Output	$P_{O(1dB)}$	+5.5 +4.5	+8.0 +7.0	— —	+7.0 +4.0	+9.5 +6.5	— —	dBm	f = 0.9 GHz f = 1.9 GHz

STANDARD CHARACTERISTICS FOR REFERENCE (T_A = +25 °C, V_{CC} = V_{out} = 3.0 V, Z_L = Z_S = 50 Ω)

PARAMETER	SYMBOL	μPC2762T			μPC2763T			UNIT	CONDITION	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Saturated Output Power	$P_{O(sat)}$	— —	+9.0 +8.5	— —	— —	+11 +8.0	— —	dBm	f = 0.9 GHz f = 1.9 GHz	
Adjacent Channel Interference	P_{adj}	—	–64	—	—	–61	—	dBc	f = 900 MHz π / 4QPSK P_O = +4 dBm	Δf = ±50 kHz
		—	–64	—	—	–62	—			Δf = ±100 kHz
3rd Order Intermodulation Distortion	IM_3	—	–16	—	—	–27	—	dBc	2 sine wave input. Output of each tone P_O = +4 dBm	f_1 = 900 MHz f_2 = 902 MHz
		—	–10	—	—	–14	—	dBc		f_1 = 1.9 GHz f_2 = 1.902 GHz

TEST CIRCUIT



Components of test circuit for measuring electrical characteristics

	TYPE	VALUE
C_3	Capacitor	1 000 pF
L	Bias Tee	1 000 nH
C_1 to C_2	Bias Tee	1 000 pF

Example of actual application components

	TYPE	VALUE	OPERATING FREQUENCY
C_1 to C_3	Chip capacitor	1 000 pF	100 MHz or higher
L	Chip inductor	50 nH	900 MHz band
		10 nH	2.5 GHz band

INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 20 mA, to output medium power. To supply current for output transistor, connect an inductor between the Vcc pin (pin 6) and output pin (pin 4). Select large value inductance, as listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port-impedance higher to get enough gain. In this case, large inductance and Q is suitable.

For above reason, select an inductance of 100 Ω or over impedance in the operating frequency. The gain is a peak in the operating frequency band, and suppressed at lower frequencies.

The recommendable inductance can be chosen from example of actual application components list as shown above.

CAPACITORS FOR THE V_{CC}, INPUT, AND OUTPUT PINS

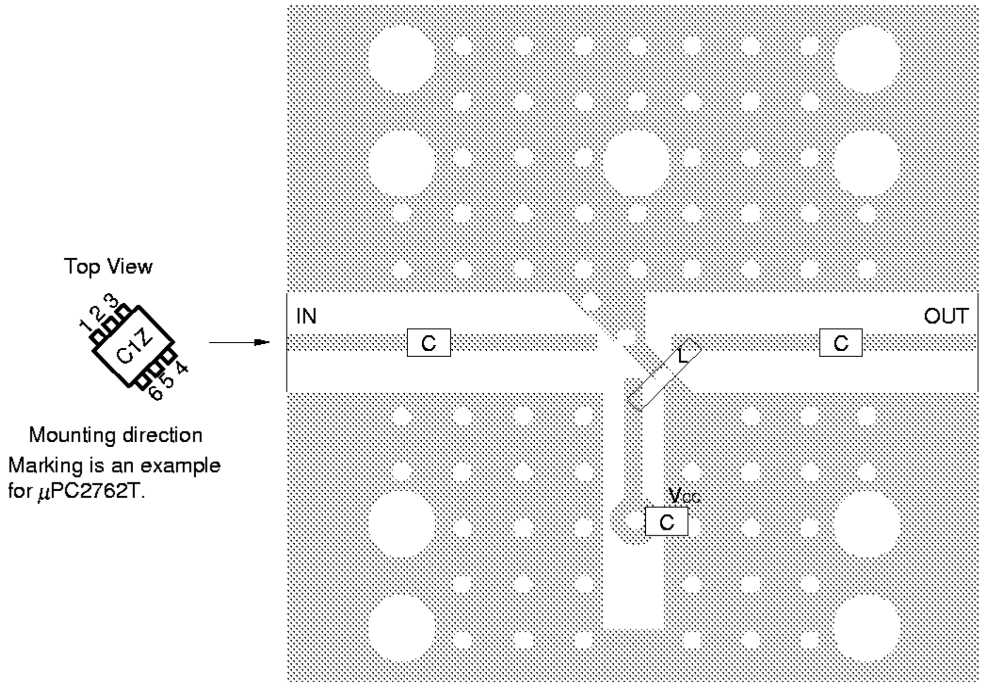
Capacitors of 1 000 pF are recommendable as the bypass capacitor for the V_{CC} pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the V_{CC} pin is used to minimize ground impedance of V_{CC} pin. So, stable bias can be supplied against V_{CC} fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation, $C = 1/(2\pi Rfc)$.

ILLUSTRATION OF TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



Component list for Application Example

SYMBOL	Value
C	1 000 pF
L	10 nH etc.

Note for Evaluation board

(1) Double sided copper clad 30 × 30 × 0.4 mm polyimide board

(2) Solder plated pattern

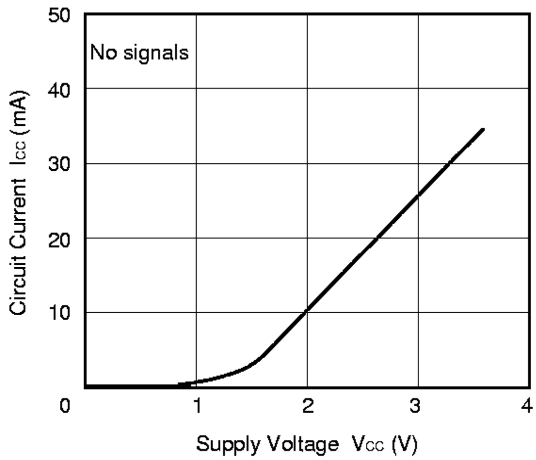
(3) ◯ : Through holes

(4) Back side: GND pattern

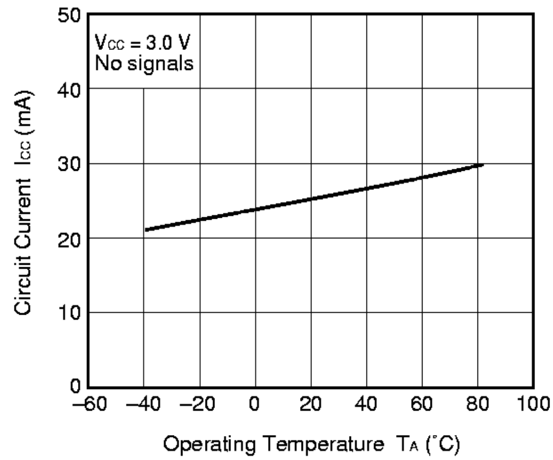
TYPICAL CHARACTERISTICS (T_A = +25 °C)

—μPC2762T—

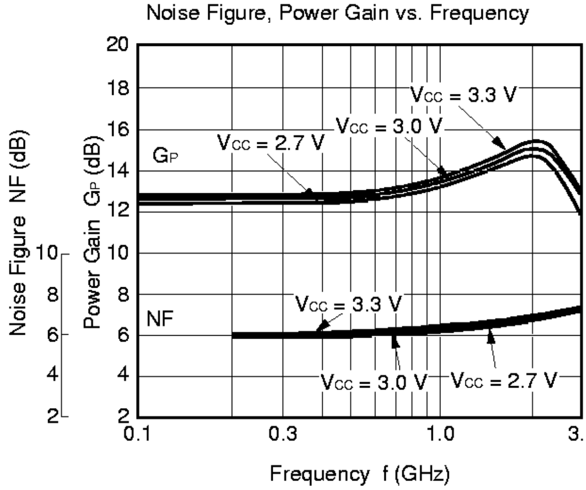
Circuit Current vs. Supply Voltage



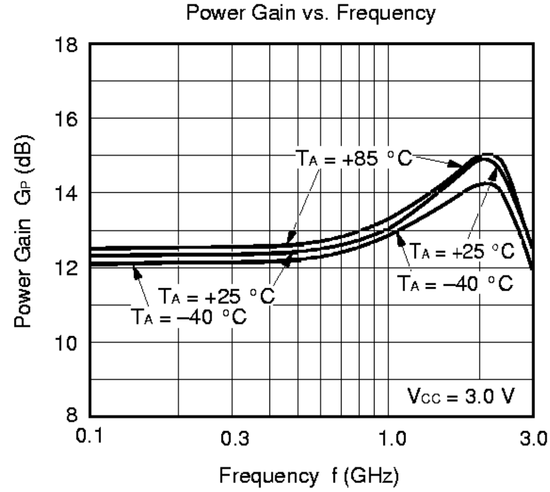
Circuit Current vs. Operating Temperature



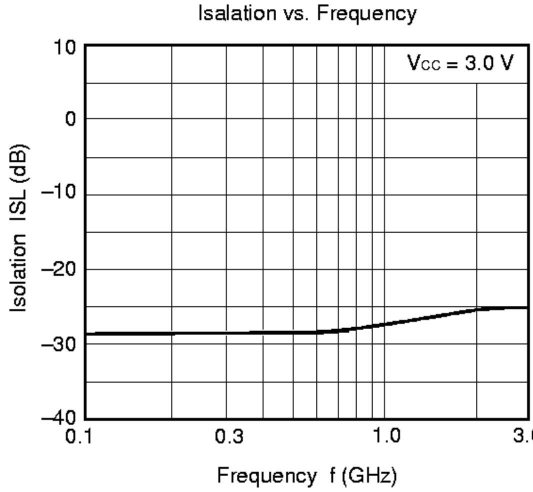
Noise Figure, Power Gain vs. Frequency



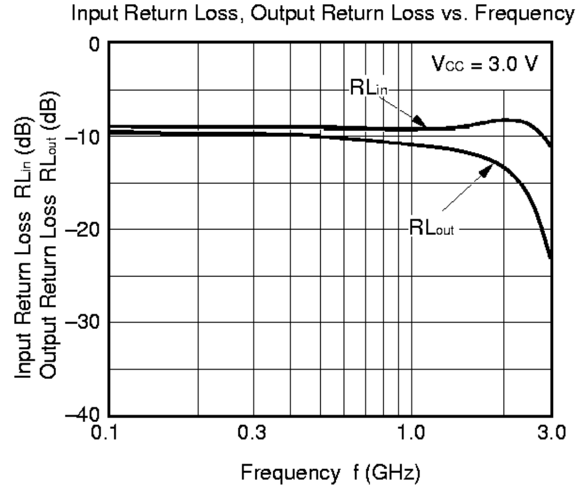
Power Gain vs. Frequency



Isalation vs. Frequency



Input Return Loss, Output Return Loss vs. Frequency



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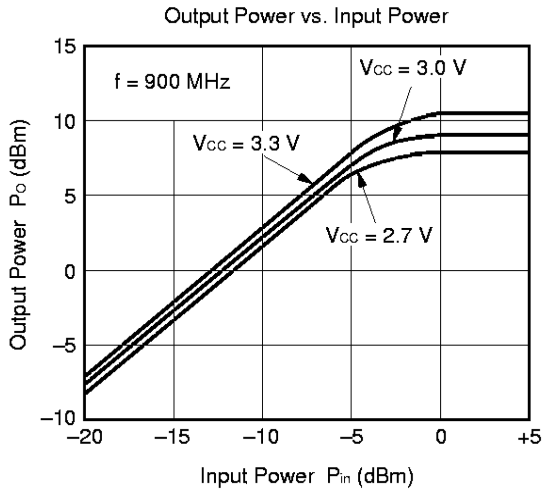
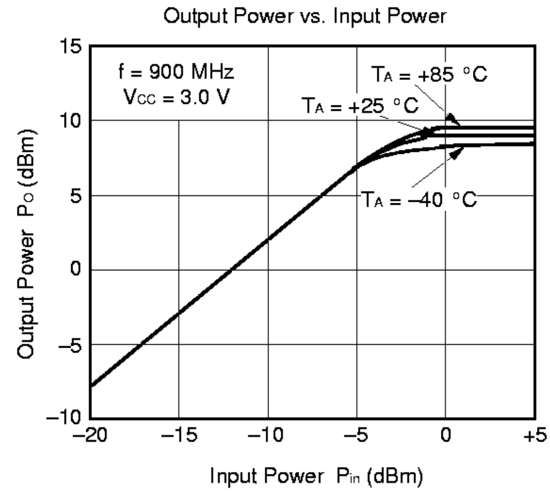
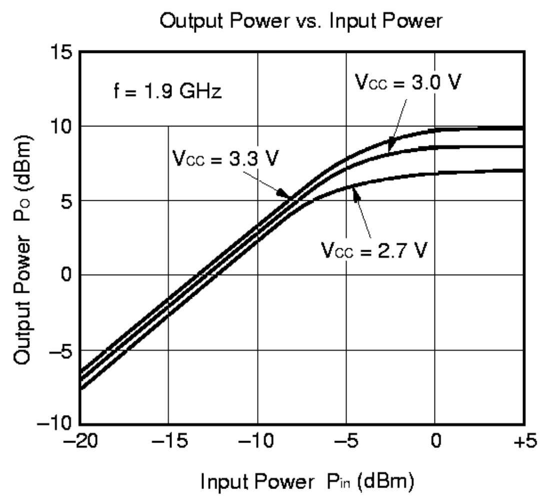
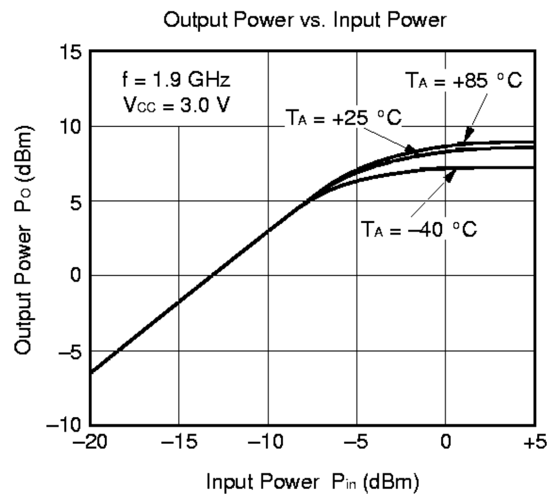
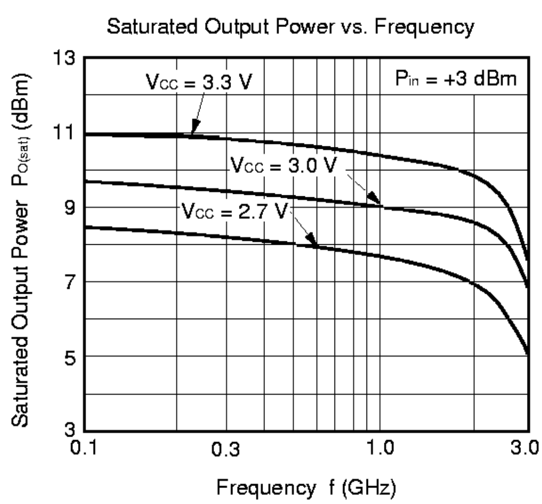
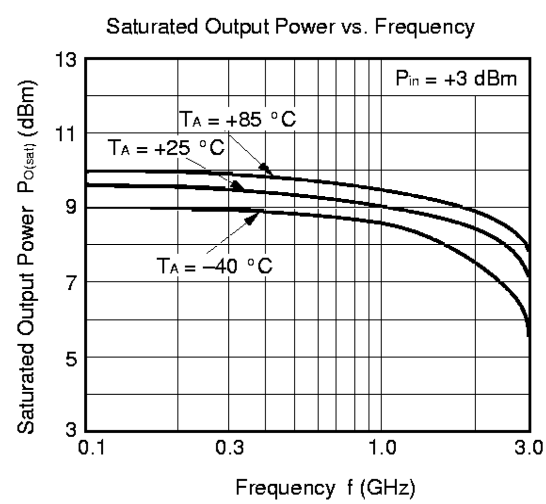

Output Power vs. Input Power
f = 900 MHz
VCC = 3.0 V
VCC = 3.3 V
VCC = 2.7 V
Output Power PO (dBm)
Input Power Pin (dBm)
15
10
5
0
−5
−10
−20
−15
−10
−5
0
+5


Output Power vs. Input Power
f = 900 MHz
VCC = 3.0 V
TA = +85 °C
TA = +25 °C
TA = −40 °C
Output Power PO (dBm)
Input Power Pin (dBm)
15
10
5
0
−5
−10
−20
−15
−10
−5
0
+5


Output Power vs. Input Power
f = 1.9 GHz
VCC = 3.0 V
VCC = 3.3 V
VCC = 2.7 V
Output Power PO (dBm)
Input Power Pin (dBm)
15
10
5
0
−5
−10
−20
−15
−10
−5
0
+5

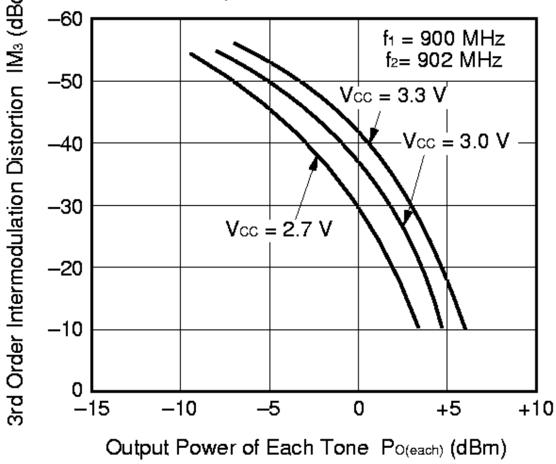

Output Power vs. Input Power
f = 1.9 GHz
VCC = 3.0 V
TA = +85 °C
TA = +25 °C
TA = −40 °C
Output Power PO (dBm)
Input Power Pin (dBm)
15
10
5
0
−5
−10
−20
−15
−10
−5
0
+5


Saturated Output Power vs. Frequency
VCC = 3.3 V
Pin = +3 dBm
VCC = 3.0 V
VCC = 2.7 V
Saturated Output Power PO(sat) (dBm)
Frequency f (GHz)
13
11
9
7
5
3
0.1
0.3
1.0
3.0

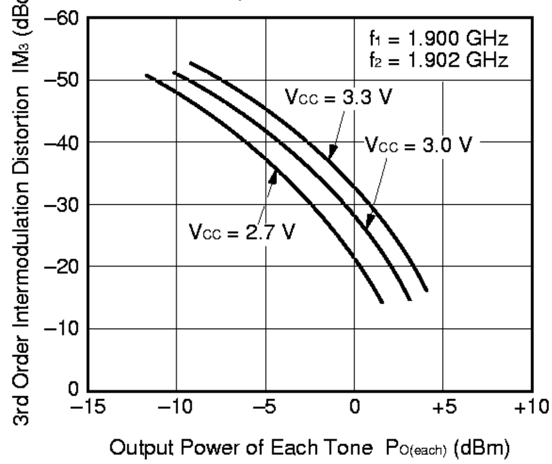

Saturated Output Power vs. Frequency
Pin = +3 dBm
TA = +85 °C
TA = +25 °C
TA = −40 °C
Saturated Output Power PO(sat) (dBm)
Frequency f (GHz)
13
11
9
7
5
3
0.1
0.3
1.0
3.0

—μPC2762T—

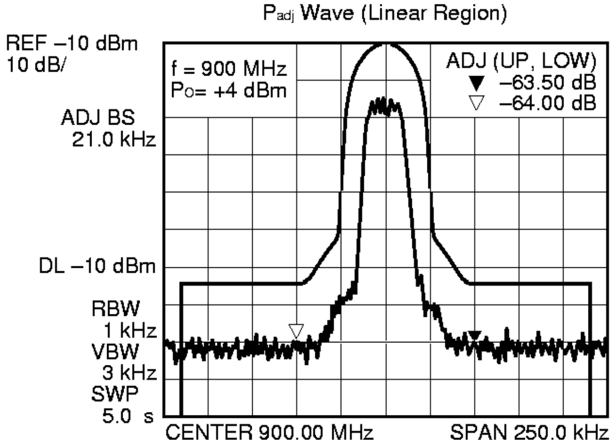
IM3 vs. Output Power of Each Tone



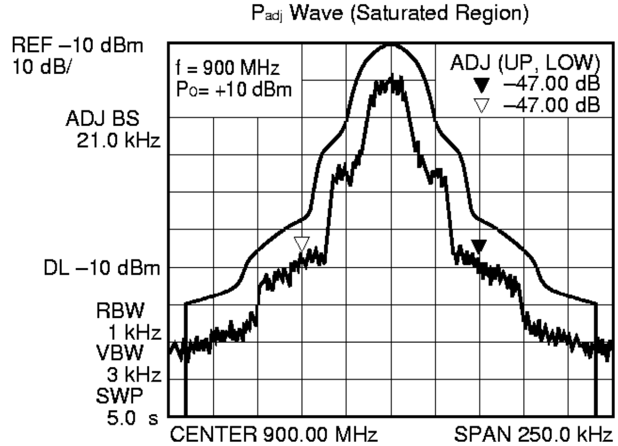
IM3 vs. Output Power of Each Tone



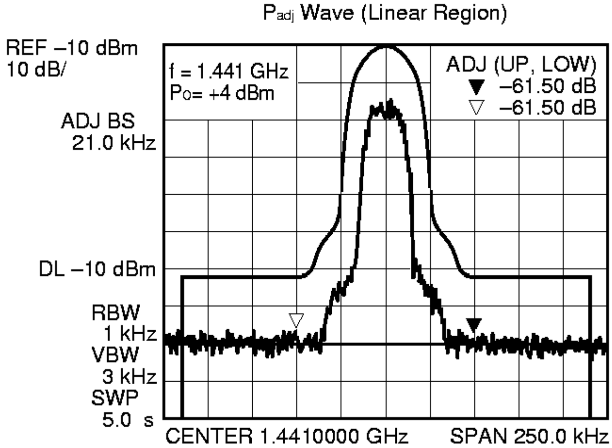
Padj Wave (Linear Region)



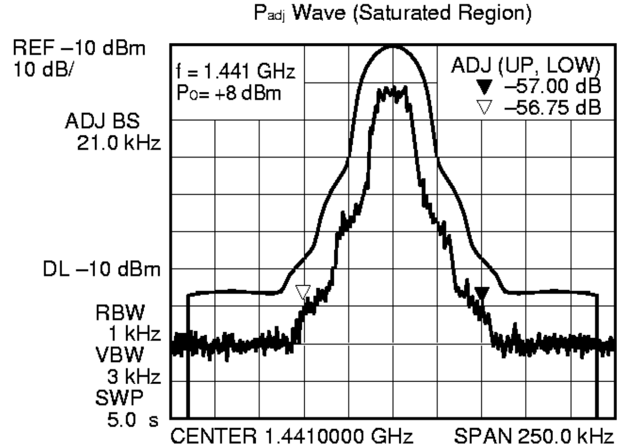
Padj Wave (Saturated Region)



Padj Wave (Linear Region)

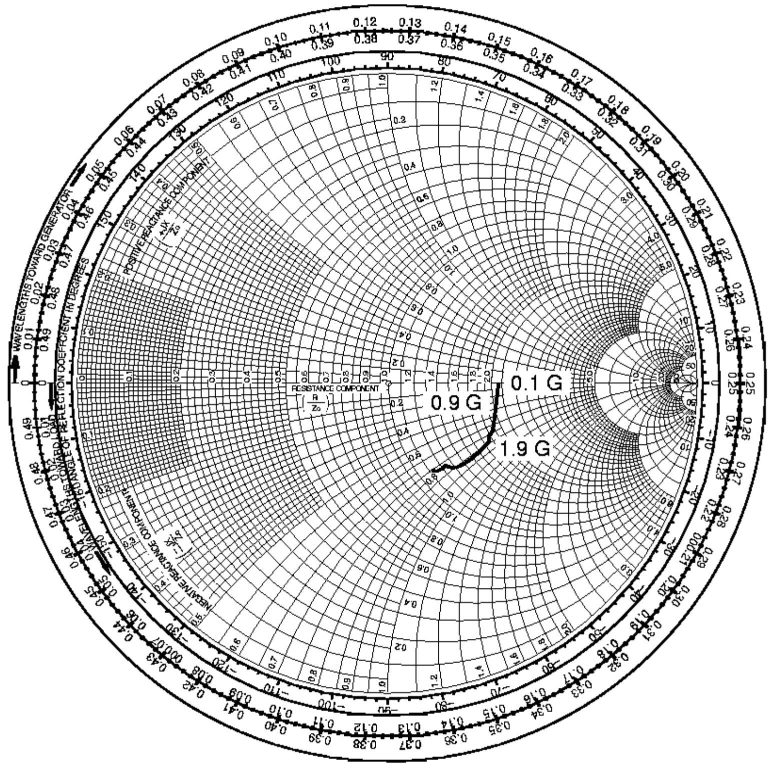


Padj Wave (Saturated Region)

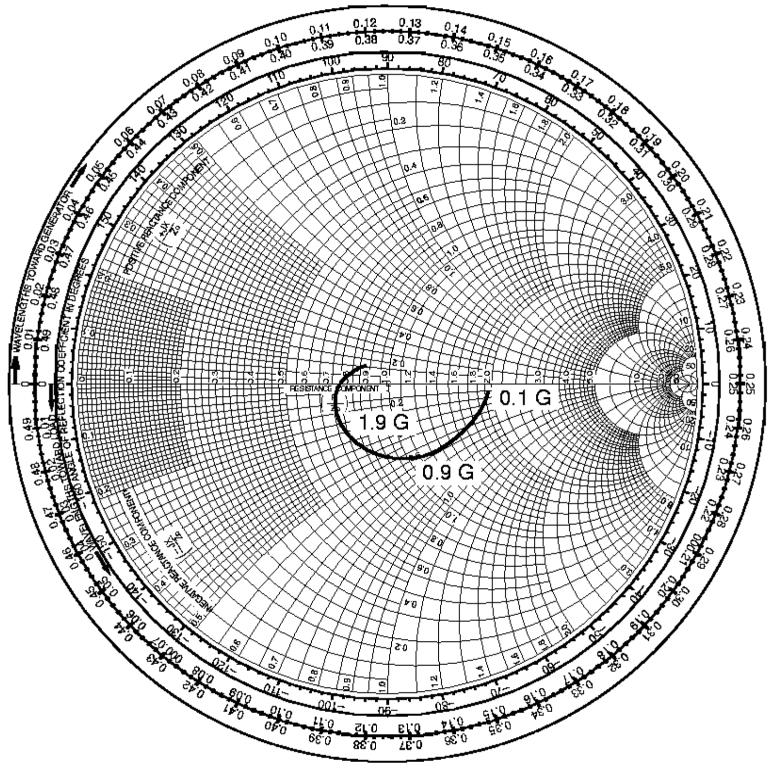


S Parameter —μPC2762T—

S_{11} – FREQUENCY (V_{CC} = 3.0 V)

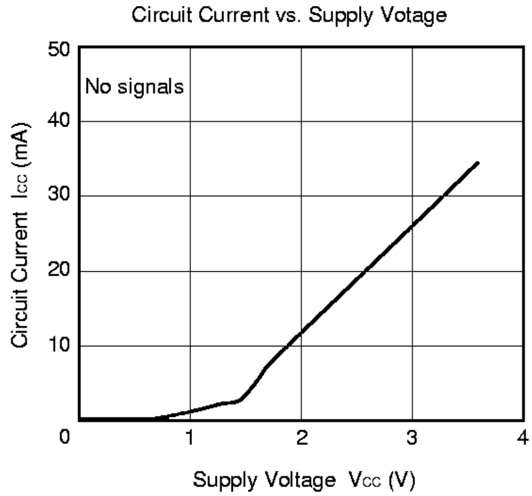


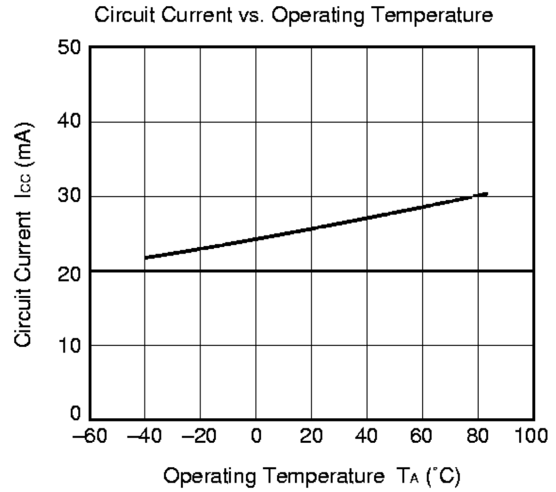
S_{22} – FREQUENCY (V_{CC} = 3.0 V)

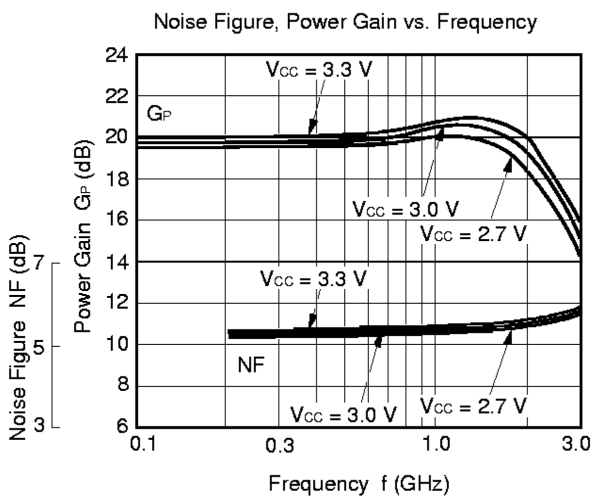


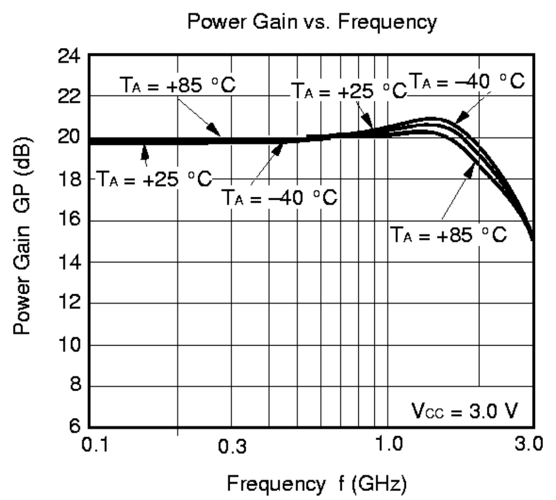
TYPICAL CHARACTERISTICS (T_A = +25 °C)

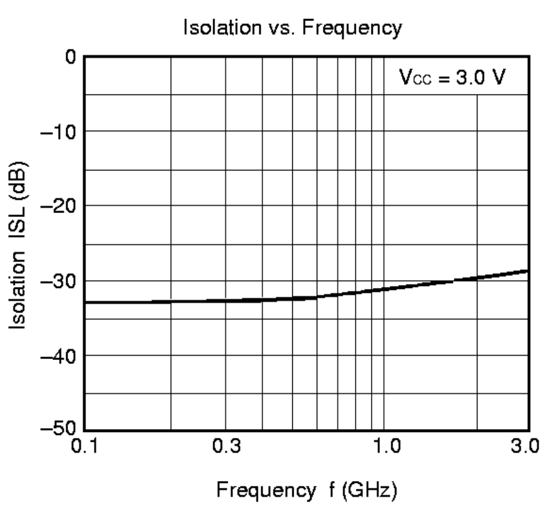
—μPC2763T—

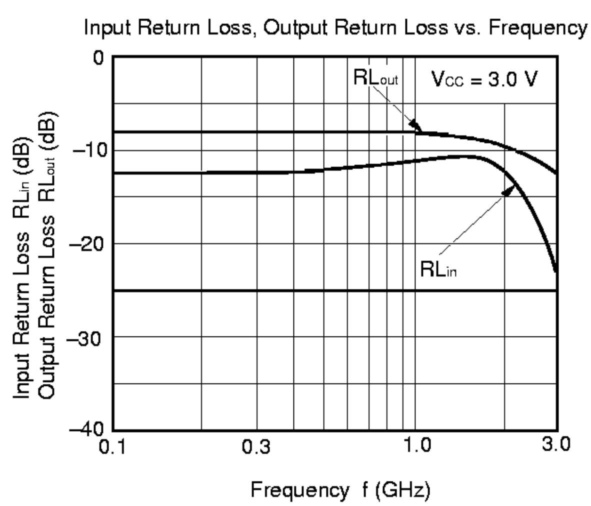






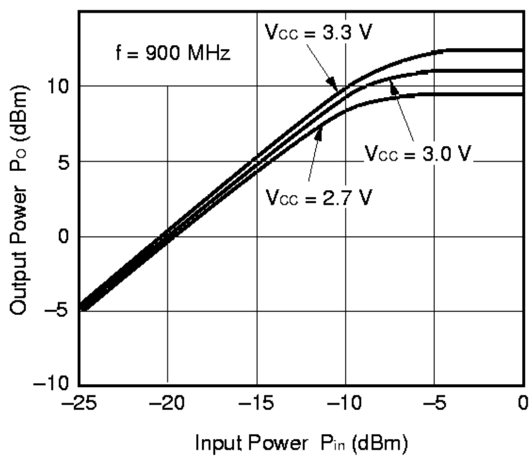




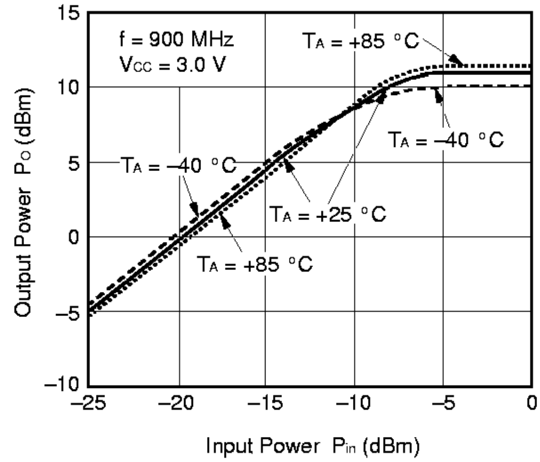


—μPC2763T—

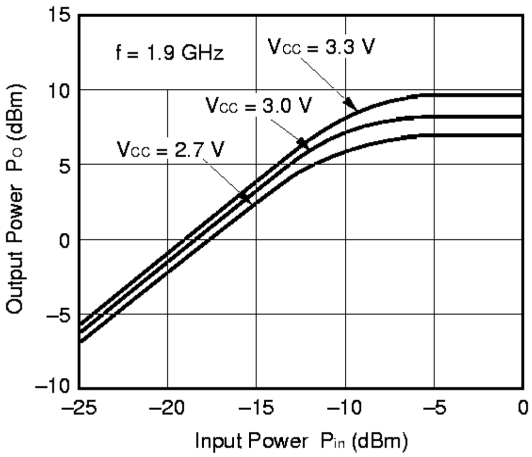
Output Power vs. Input Power



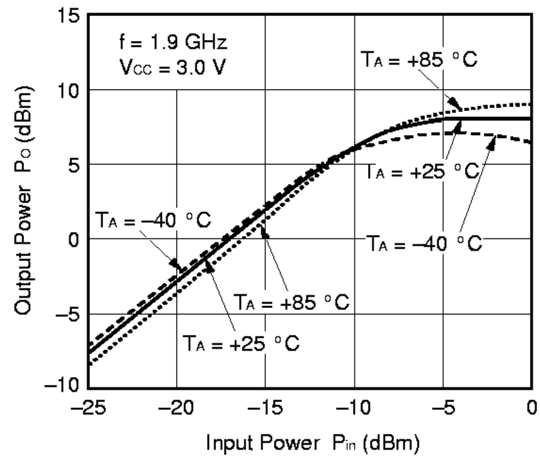
Output Power vs. Input Power



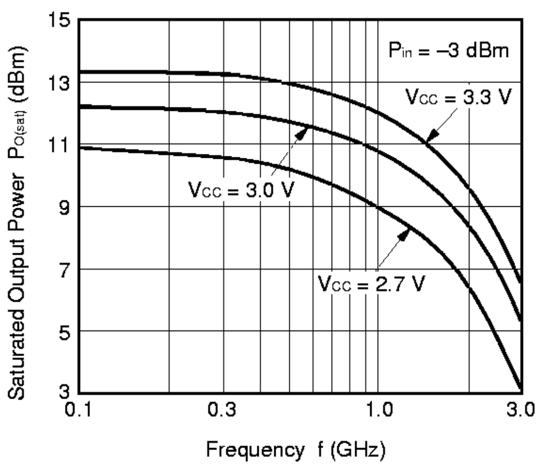
Output Power vs. Input Power



Output Power vs. Input Power



Saturated Output Power vs. Frequency



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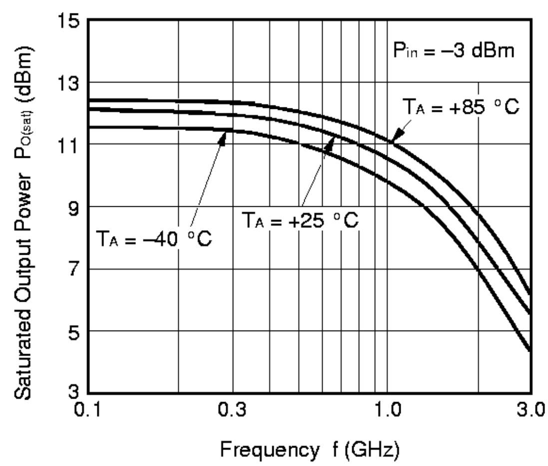
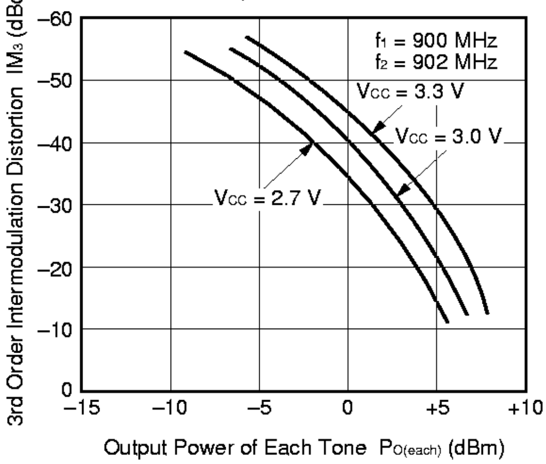
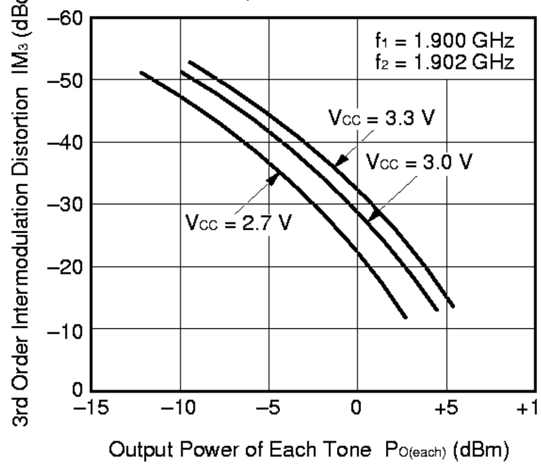


—μPC2763T—

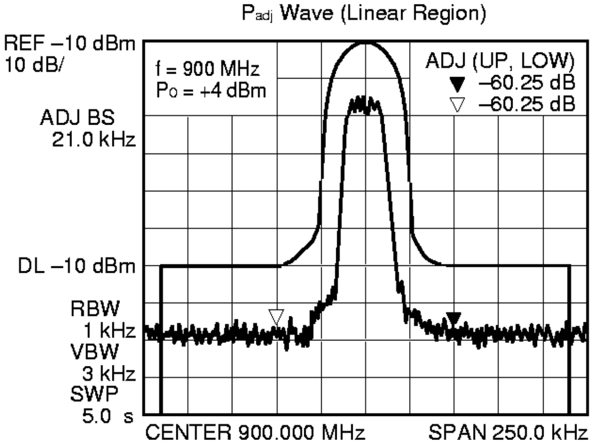
IM3 vs. Output Power of Each Tone



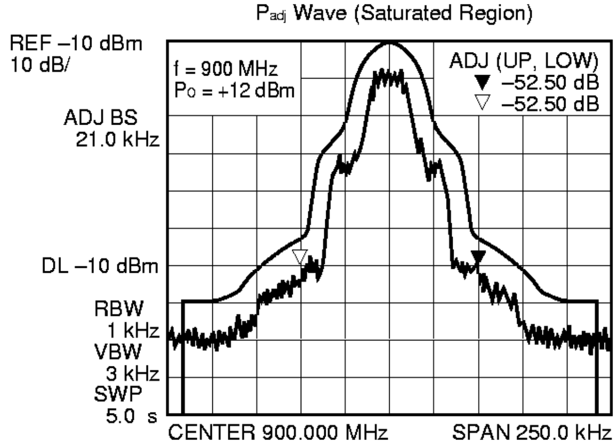
IM3 vs. Output Power of Each Tone



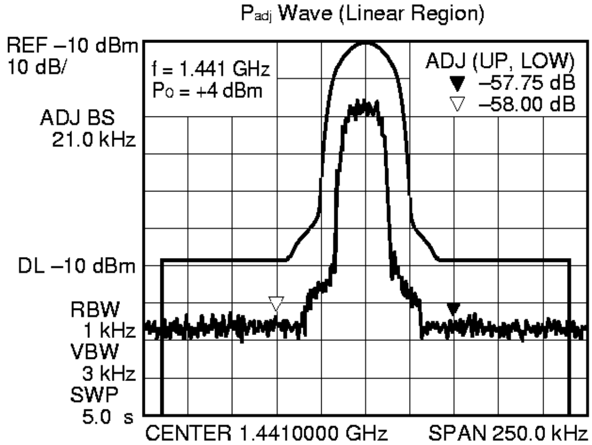
Padj Wave (Linear Region)



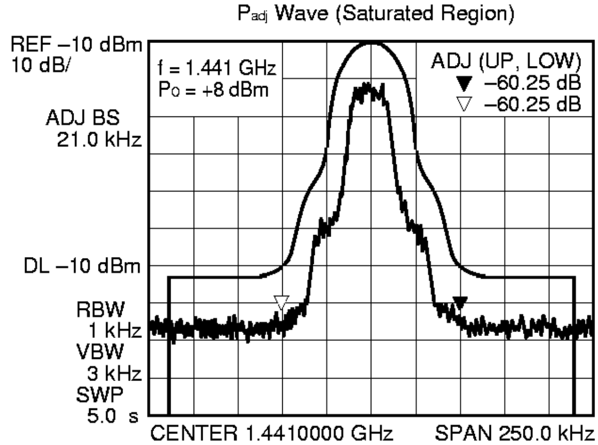
Padj Wave (Saturated Region)



Padj Wave (Linear Region)

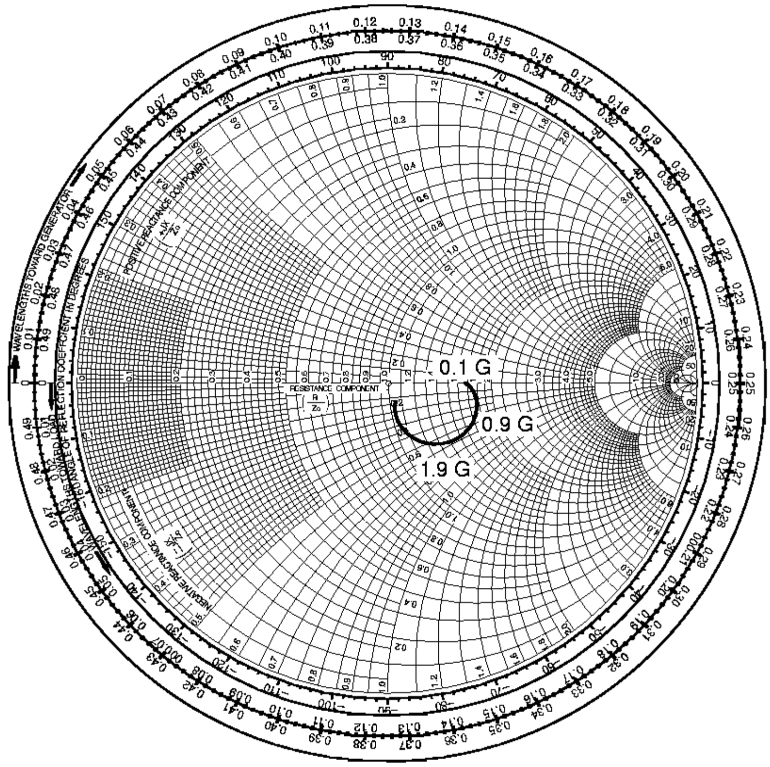


Padj Wave (Saturated Region)

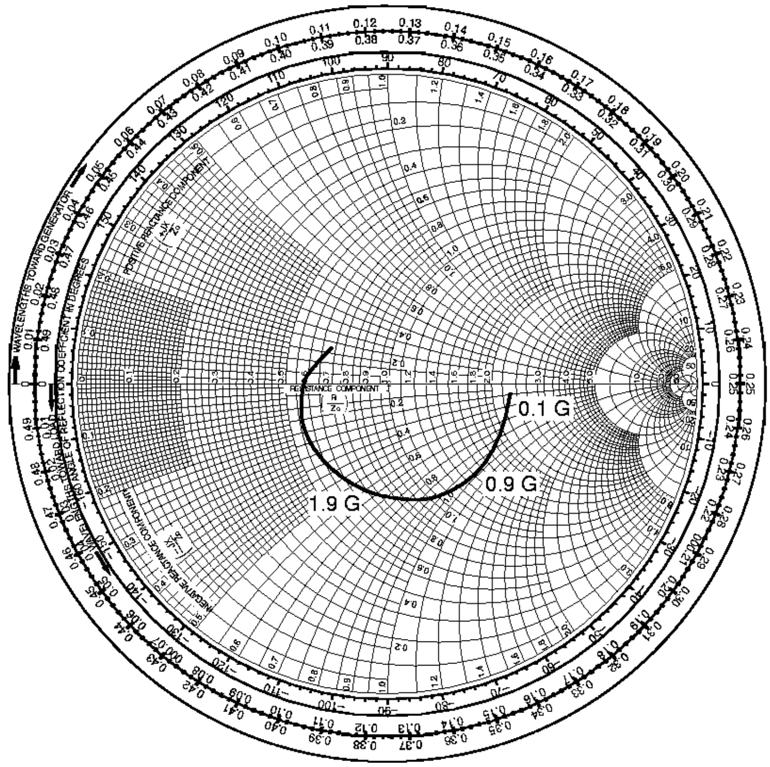


S Parameter —μPC2763T—

S_{11} – FREQUENCY (V_{CC} = 3.0 V)



S_{22} – FREQUENCY (V_{CC} = 3.0 V)



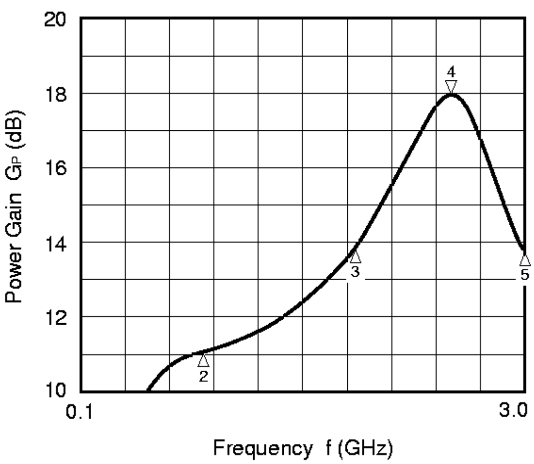
—CHARACTERISTIC CURVES WITH ACTUAL APPLICATION COMPONENTS EXAMPLE—

Specifications of sample chip inductor

Manufacturer	Product name	Inductance: nH	Q TYP.	DC resistance	Self-resonance frequency	Allowable current
Murata Mfg. Co, Ltd.	LQN2A10NM	10	60	0.25 ≤ 0	1 000 MHz	770 mA

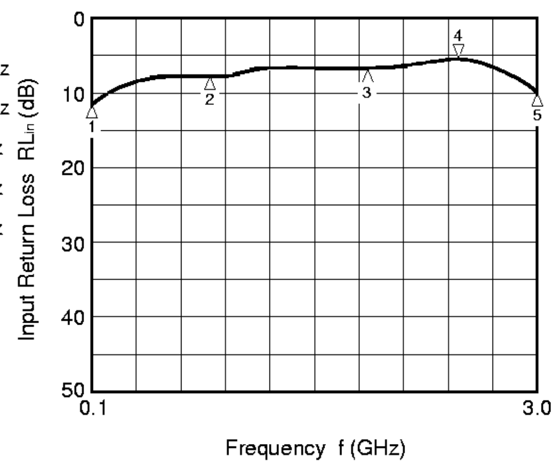
—μPC2762T—

POWER GAIN vs. FREQUENCY

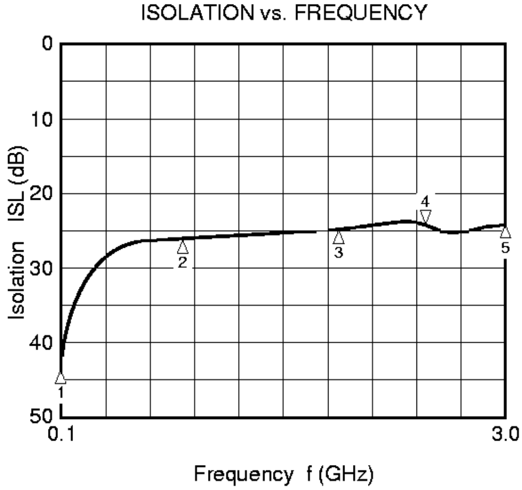


1: 100 MHz
2: 900 MHz
3: 1.9 GHz
4: 2.5 GHz
5: 3.0 GHz

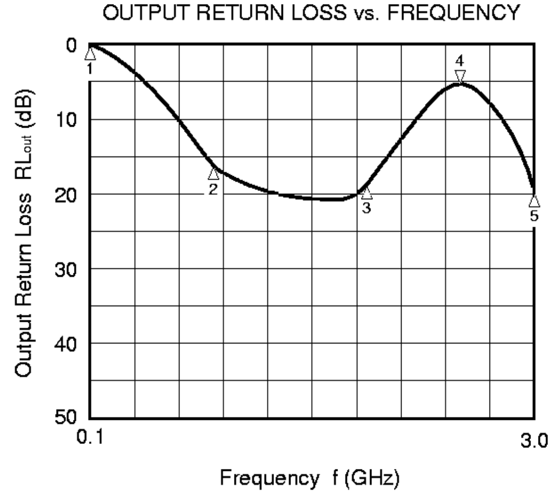
INPUT RETURN LOSS vs. FREQUENCY



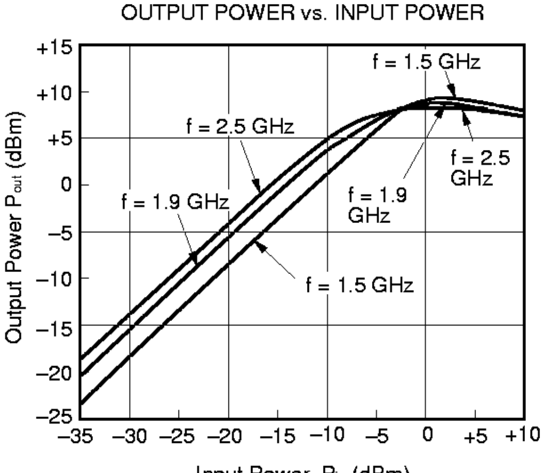
ISOLATION vs. FREQUENCY



OUTPUT RETURN LOSS vs. FREQUENCY

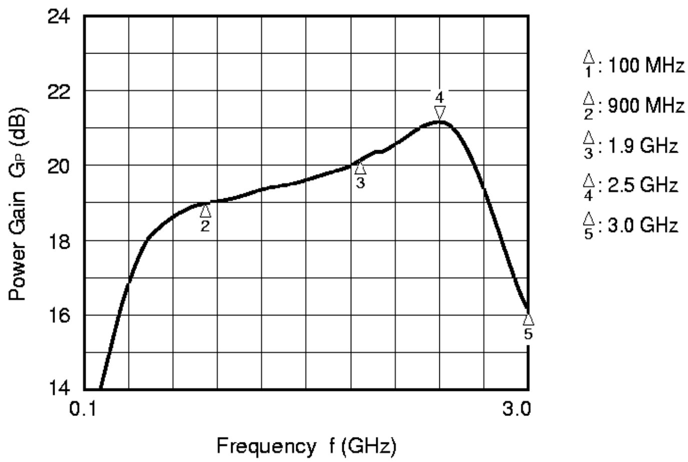


OUTPUT POWER vs. INPUT POWER

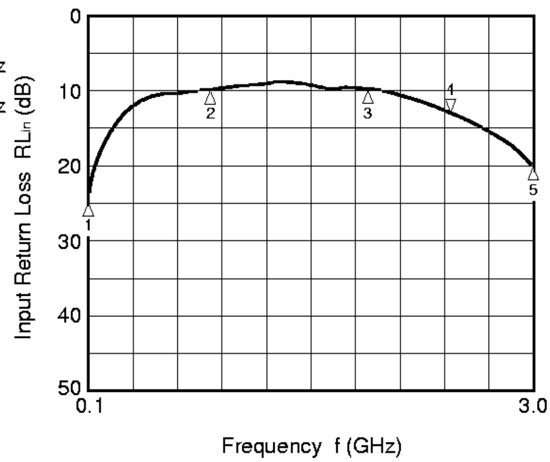


—μPC2763T—

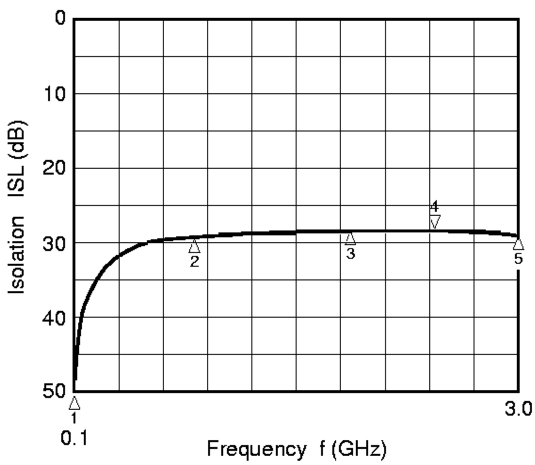
POWER GAIN vs. FREQUENCY



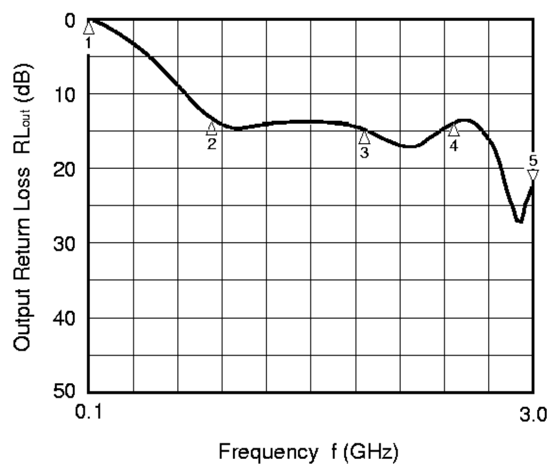
INPUT RETURN LOSS vs. FREQUENCY



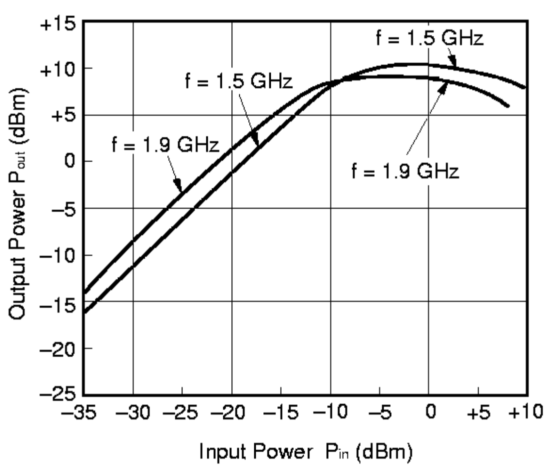
ISOLATION vs. FREQUENCY



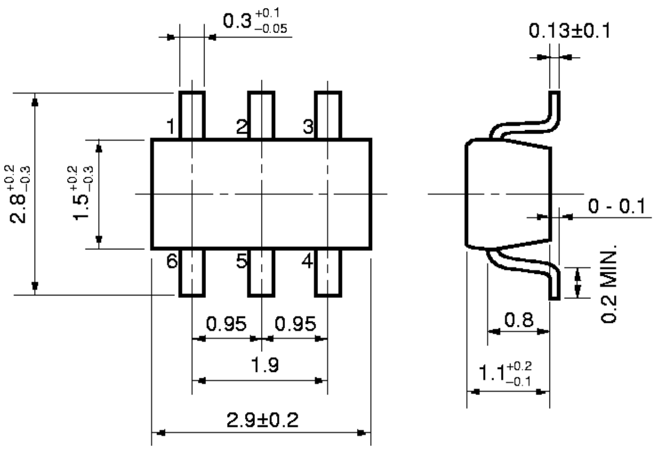
OUTPUT RETURN LOSS vs. FREQUENCY



OUTPUT POWER vs. INPUT POWER



DIMENSIONS OF 6-PIN MINI-MOLD PACKAGE (Units: mm)



NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
(3) The bypass capacitor should be attached to the Vcc pin.
(4) The inductor must be attached between Vcc and output pin. The indactance value should be determined in accordance with desired frequency.
(5) The DC cut capacitor must be each attached to the input and output pins.

RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be satisfied when soldering this product.

Consult your NEC sales offices when using any other soldering process, or when soldering is done under different conditions.

μPC2762T, μPC2763T

SOLDERING PROCESS	SOLDERING CONDITIONS	SYMBOL
Infrared ray reflow	Peak package surface temperature : 235 °C Reflow time : 30 seconds MAX. (at 210 °C or more) Number of reflow processes : 3 Exposure limit[Note] : None	IR35-00-3
VPS	Peak package surface temperature : 215 °C Reflow time : 40 seconds MAX. (at 200 °C or more) Number of reflow processes : 3 Exposure limit[Note] : None	VP15-00-3
Wave soldering	Solder temperature : 260 °C Flow time : 10 seconds MAX. Number of flow processes : 1 Exposure limit[Note] : None	WS60-00-1
Partial heating method	Solder temperature : 300 °C or less Flow time : 3 seconds MAX./pin Exposure limit[Note] : None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity of 65 %

Caution Do not apply more than a single process at once, except for "Partial heating method".

For details of the recommended soldering conditions, refer to the "SMD Surface Mount Technology Manual" (C10535EJ7V0IF00).

ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

- Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.
Anti-radioactive design is not implemented in this product.

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