



# 1.5V DDR2 SDRAM

**MT47J256M4 – 32 Meg x 4 x 8 Banks**
**MT47J128M8 – 16 Meg x 8 x 8 Banks**
**MT47J64M16 – 8 Meg x 16 x 8 Banks**

## Features

- $V_{DD} = V_{DDQ} = +1.5V - 0.075V, +0.125V$
- Pseudo 1.8V I/O
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 t<sub>CK</sub>
- Selectable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Supports JEDEC clock jitter specification
- RoHS compliant
- 95°C T<sub>CASE</sub> support
- Very low power DDR2 operation

## Options

- Configuration
  - 256 Meg x 4 (32 Meg x 4 x 8 banks) 256M4
  - 128 Meg x 8 (16 Meg x 8 x 8 banks) 128M8
  - 64 Meg x 16 (8 Meg x 16 x 8 banks) 64M16
- FBGA package
  - 60-ball FBGA (8mm x 11.5mm) Rev. E HQ
  - 84-ball FBGA (8mm x 12.5mm) Rev. E HR
- Timing – cycle time
  - 5.0ns @ CL = 3 (DDR2-400) -5E
  - 3.75ns @ CL = 4 (DDR2-533) -37E
  - 3.0ns @ CL = 5 (DDR2-667) -3
  - 3.0ns @ CL = 4 (DDR2-667) -3E
  - 2.5ns @ CL = 6 (DDR2-800) -25
  - 2.5ns @ CL = 5 (DDR2-800) -25E
  - 1.875ns @ CL = 7 (DDR2-1066) -187E
- Operating temperature
  - Commercial<sup>1</sup> (0°C ≤ T<sub>C</sub> ≤ 95°C) None
- Revision :E

## Marking

Notes: 1. All speed grades are not necessarily available in all configurations.

**Table 1: Key Timing Parameters**

Speed Grade	Data Rate (MT/s)					t <sub>RC</sub> (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	CL = 7	
-5E	400	400	n/a	n/a	n/a	55
-37E	400	533	n/a	n/a	n/a	55
-3	400	533	667	n/a	n/a	55
-3E	n/a	667	667	n/a	n/a	54
-25	n/a	533	667	800	n/a	55
-25E	n/a	533	800	n/a	n/a	55
-187E	n/a	n/a	667	800	1066	54

**Table 2: Configuration Addressing**

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 Banks	16 Meg x 8 x 8 Banks	8 Meg x 16 x 8 Banks
Refresh count	8K	8K	8K
Row address	A0–A13 (16K)	A0–A13 (16K)	A0–A12 (8K)
Bank address	BA0–BA2 (8)	BA0–BA2 (8)	BA0–BA2 (8)
Column address	A0–A9, A11 (2K)	A0–A9 (1K)	A0–A9 (1K)



## Table of Contents

Features . . . . .	1
Functional Description . . . . .	9
General Notes . . . . .	10
Ball Assignments and Descriptions . . . . .	11
Functional Block Diagrams . . . . .	16
State Diagram . . . . .	18
Initialization . . . . .	19
Mode Register (MR) . . . . .	22
Burst Length . . . . .	22
Burst Type . . . . .	23
Operating Mode . . . . .	24
DLL RESET . . . . .	24
Write Recovery . . . . .	24
Power-Down Mode . . . . .	25
CAS Latency (CL) . . . . .	25
Extended Mode Register (EMR) . . . . .	26
DLL Enable/Disable . . . . .	27
Output Drive Strength . . . . .	28
DQS# Enable/Disable . . . . .	28
RDQS Enable/Disable . . . . .	28
Output Enable/Disable . . . . .	28
On-Die Termination (ODT) . . . . .	28
Off-Chip Driver (OCD) Impedance Calibration . . . . .	29
Posted CAS Additive Latency (AL) . . . . .	29
Extended Mode Register 2 . . . . .	30
Extended Mode Register 3 . . . . .	31
Command Truth Tables . . . . .	32
DESELECT, NOP, and LM Commands . . . . .	37
DESELECT . . . . .	37
NO OPERATION (NOP) . . . . .	37
LOAD MODE (LM) . . . . .	37
Bank/Row Activation . . . . .	37
ACTIVE Command . . . . .	37
ACTIVE Operation . . . . .	37
READ Command . . . . .	38
READ Operation . . . . .	39
WRITE Command . . . . .	50
WRITE Operation . . . . .	50
PRECHARGE Command . . . . .	61
PRECHARGE Operation . . . . .	61
SELF REFRESH Command . . . . .	61
REFRESH Command . . . . .	63
Power-Down Mode . . . . .	64
Precharge Power-Down Clock Frequency Change . . . . .	71
RESET Function . . . . .	72
(CKE LOW Anytime) . . . . .	72
ODT Timing . . . . .	74
MRS Command to ODT Update Delay . . . . .	75
Absolute Maximum Ratings . . . . .	79
Temperature and Thermal Impedance . . . . .	79
AC and DC Operating Conditions . . . . .	81



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Table of Contents

Input Electrical Characteristics and Operating Conditions . . . . .	82
Input Slew Rate Derating . . . . .	85
Power and Ground Clamp Characteristics . . . . .	97
AC Overshoot/Undershoot Specification . . . . .	98
Output Electrical Characteristics and Operating Conditions . . . . .	99
Full Strength Pull-Down Driver Characteristics . . . . .	101
Full Strength Pull-Up Driver Characteristics . . . . .	102
Reduced Strength Pull-Down Driver Characteristics . . . . .	103
Reduced Strength Pull-Up Driver Characteristics . . . . .	104
FBGA Package Capacitance . . . . .	105
IDD7 Conditions . . . . .	108
AC Operating Specifications . . . . .	109
Notes . . . . .	116
Package Dimensions . . . . .	120

**List of Figures**

Figure 1: 1Gb 1.5V DDR2 Part Numbers . . . . . 8

Figure 2: 60-Ball FBGA – x4, x8 Pin Assignments (Top View) . . . . . 11

Figure 4: 64 Meg x 16 Functional Block Diagram . . . . . 16

Figure 5: 128 Meg x 8 Functional Block Diagram . . . . . 17

Figure 6: 256 Meg x 4 Functional Block Diagram . . . . . 17

Figure 7: Simplified State Diagram . . . . . 18

Figure 8: 1.5V DDR2 Power-Up and Initialization . . . . . 19

Figure 9: Mode Register (MR) Definition . . . . . 23

Figure 10: CAS Latency (CL) . . . . . 26

Figure 11: Extended Mode Register Definition . . . . . 27

Figure 12: READ Latency . . . . . 29

Figure 13: WRITE Latency . . . . . 30

Figure 14: Extended Mode Register 2 (EMR2) Definition . . . . . 30

Figure 15: Extended Mode Register 3 (EMR3) Definition . . . . . 31

Figure 16: Example: Meeting <sup>t</sup>RRD (MIN) and <sup>t</sup>RCD (MIN) . . . . . 38

Figure 17: Multibank Activate Restriction . . . . . 38

Figure 18: READ Latency . . . . . 40

Figure 19: Consecutive READ Bursts . . . . . 41

Figure 20: Nonconsecutive READ Bursts . . . . . 42

Figure 21: READ Interrupted by READ . . . . . 42

Figure 22: READ-to-PRECHARGE – BL = 4 . . . . . 44

Figure 23: READ-to-PRECHARGE – BL = 8 . . . . . 44

Figure 24: READ-to-WRITE . . . . . 44

Figure 25: Bank Read – Without Auto Precharge . . . . . 45

Figure 26: Bank Read – with Auto Precharge . . . . . 46

Figure 27: x4, x8 Data Output Timing – <sup>t</sup>DQSQ, <sup>t</sup>QH, and Data Valid Window . . . . . 47

Figure 29: Data Output Timing – <sup>t</sup>AC and <sup>t</sup>DQCK. . . . . 49

Figure 30: WRITE Burst. . . . . 52

Figure 31: Consecutive WRITE-to-WRITE . . . . . 53

Figure 32: Nonconsecutive WRITE-to-WRITE. . . . . 53

Figure 33: Random WRITE Cycles . . . . . 54

Figure 34: WRITE Interrupted by WRITE . . . . . 54

Figure 35: WRITE-to-READ . . . . . 55

Figure 36: WRITE-to-PRECHARGE . . . . . 56

Figure 37: Bank Write – Without Auto Precharge . . . . . 57

Figure 38: Bank Write – with Auto Precharge. . . . . 58

Figure 39: WRITE – DM Operation. . . . . 59

Figure 42: Refresh Mode. . . . . 63

Figure 43: Power-Down . . . . . 65

Figure 44: READ to Power-Down or Self Refresh Entry . . . . . 67

Figure 45: READ with Auto Precharge to Power-Down or Self Refresh Entry. . . . . 67

Figure 47: WRITE with Auto Precharge to Power-Down or Self Refresh Entry. . . . . 68

Figure 48: REFRESH Command to Power-Down Entry. . . . . 69

Figure 49: ACTIVE Command to Power-Down Entry . . . . . 69

Figure 50: PRECHARGE Command to Power-Down Entry . . . . . 70

Figure 51: LOAD MODE Command to Power-Down Entry . . . . . 70

Figure 52: Input Clock Frequency Change During Precharge Power-Down Mode. . . . . 71

Figure 53: RESET Function . . . . . 73

Figure 54: ODT Timing for Entering and Exiting Power-Down Mode . . . . . 75

Figure 55: Timing for MRS Command to ODT Update Delay . . . . . 75

Figure 56: ODT Timing for Active or Fast-Exit Power-Down Mode . . . . . 76

Figure 57: ODT Timing for Slow-Exit or Precharge Power-Down Modes . . . . . 76

Figure 58: ODT Turn-Off Timings When Entering Power-Down Mode . . . . . 77

Figure 59: ODT Turn-On Timing When Entering Power-Down Mode . . . . . 77

Figure 60: ODT Turn-Off Timing When Exiting Power-Down Mode . . . . . 78

Figure 61: ODT Turn-On Timing When Exiting Power-Down Mode . . . . . 78

Figure 62:	Example Temperature Test Point Location . . . . .	.80
Figure 63:	Single-Ended Input Signal Levels . . . . .	.82
Figure 64:	Differential Input Signal Levels . . . . .	.83
Figure 65:	Nominal Slew Rate for $t_{IS}$ . . . . .	.87
Figure 66:	Tangent Line for $t_{IS}$ . . . . .	.87
Figure 67:	Nominal Slew Rate for $t_{IH}$ . . . . .	.88
Figure 68:	Tangent Line for $t_{IH}$ . . . . .	.88
Figure 69:	Nominal Slew Rate for $t_{DS}$ . . . . .	.93
Figure 70:	Tangent Line for $t_{DS}$ . . . . .	.93
Figure 71:	Nominal Slew Rate for $t_{DH}$ . . . . .	.94
Figure 72:	Tangent Line for $t_{DH}$ . . . . .	.94
Figure 73:	AC Input Test Signal Waveform Command/Address Balls . . . . .	.95
Figure 74:	AC Input Test Signal Waveform for Data with DQS, DQS# (Differential). . . . .	.95
Figure 75:	AC Input Test Signal Waveform for Data with DQS (Single-Ended) . . . . .	.96
Figure 76:	AC Input Test Signal Waveform (Differential) . . . . .	.96
Figure 77:	Input Clamp Characteristics . . . . .	.97
Figure 78:	Overshoot . . . . .	.98
Figure 79:	Undershoot . . . . .	.98
Figure 80:	Differential Output Signal Levels . . . . .	.99
Figure 81:	Output Slew Rate Load . . . . .	100
Figure 82:	Full Strength Pull-Down Characteristics . . . . .	101
Figure 83:	Full Strength Pull-Up Characteristics . . . . .	102
Figure 84:	Reduced Strength Pull-Down Characteristics . . . . .	103
Figure 85:	Reduced Strength Pull-Up Characteristics . . . . .	104
Figure 86:	60-Ball FBGA Package – x4, x8 . . . . .	120
Figure 87:	84-Ball FBGA Package – x16 . . . . .	121

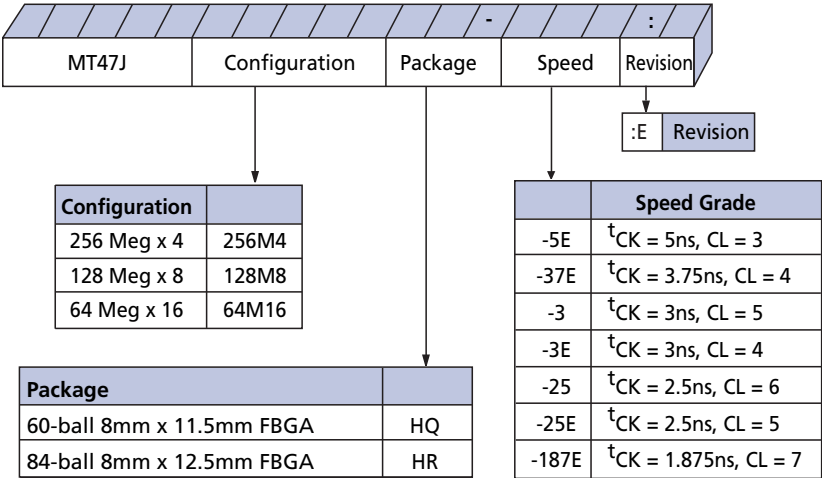
**List of Tables**

Table 1:	Key Timing Parameters . . . . .	1
Table 2:	Configuration Addressing . . . . .	2
Table 3:	FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions . . . . .	13
Table 4:	Burst Definition . . . . .	24
Table 5:	Truth Table – 1.5V DDR2 Commands . . . . .	32
Table 6:	Truth Table – Current State Bank <i>n</i> – Command to Bank <i>n</i> . . . . .	33
Table 7:	Truth Table – Current State Bank <i>n</i> – Command to Bank <i>m</i> . . . . .	35
Table 8:	Minimum Delay with Auto Precharge Enabled . . . . .	36
Table 9:	READ Using Concurrent Auto Precharge . . . . .	43
Table 10:	WRITE Using Concurrent Auto Precharge . . . . .	51
Table 11:	CKE Truth Table . . . . .	66
Table 12:	Absolute Maximum DC Ratings . . . . .	79
Table 13:	Temperature Limits . . . . .	80
Table 14:	Thermal Impedance . . . . .	80
Table 15:	Recommended DC Operating Conditions (SSTL_18) . . . . .	81
Table 16:	ODT DC Electrical Characteristics . . . . .	81
Table 17:	Input DC Logic Levels . . . . .	82
Table 18:	Input AC Logic Levels . . . . .	82
Table 19:	Differential Input Logic Levels . . . . .	83
Table 20:	AC Input Test Conditions . . . . .	84
Table 21:	1.5V DDR2-400/533 Setup and Hold Time Derating Values ( <sup>t</sup> IS and <sup>t</sup> IH) . . . . .	86
Table 22:	1.5V DDR2-667/800/1066 Setup and Hold Time Derating Values ( <sup>t</sup> IS and <sup>t</sup> IH) . . . . .	86
Table 23:	1.5V DDR2-400/DDR2-533 <sup>t</sup> DS, <sup>t</sup> DH Derating Values with Differential Strobe . . . . .	89
Table 24:	1.5V DDR2-667/DDR2-800/DDR2-1066 <sup>t</sup> DS, <sup>t</sup> DH Derating Values with Differential Strobe . . . . .	90
Table 25:	Single-Ended DQS Slew Rate Derating Values Using <sup>t</sup> DS <sub>b</sub> and <sup>t</sup> DH <sub>b</sub> . . . . .	91
Table 26:	Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at 1.5V DDR2-667 . . . . .	91
Table 27:	Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at 1.5V DDR2-533 . . . . .	92
Table 28:	Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at 1.5V DDR2-400 . . . . .	92
Table 29:	Input Clamp Characteristics . . . . .	97
Table 30:	Address and Control Balls . . . . .	98
Table 31:	Clock, Data, Strobe, and Mask Balls . . . . .	98
Table 32:	Differential AC Output Parameters . . . . .	99
Table 33:	Output DC Current Drive . . . . .	100
Table 34:	Output Characteristics . . . . .	100
Table 35:	Full Strength Pull-Down Current (mA) . . . . .	101
Table 36:	Full Strength Pull-Up Current (mA) . . . . .	102
Table 37:	Reduced Strength Pull-Down Current (mA) . . . . .	103
Table 38:	Reduced Strength Pull-Up Current (mA) . . . . .	104
Table 39:	Input Capacitance . . . . .	105
Table 40:	Input Capacitance . . . . .	105
Table 41:	1.5V DDR2 IDD Specifications and Conditions (Die Revision E) . . . . .	106
Table 42:	General IDD Parameters . . . . .	108
Table 43:	IDD7 Timing Patterns (8-Bank Interleave READ Operation) . . . . .	108
Table 44:	AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds . . . . .	109



1Gb: x4, x8, x16 1.5V DDR2 SDRAM

Figure 1: 1Gb 1.5V DDR2 Part Numbers



Notes: 1. Not all speeds and configurations may be available in each package.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron’s Web site: [www.micron.com](http://www.micron.com).





## Functional Description

The 1.5V DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multibank DRAM. The functional block diagrams of all device configurations are shown starting on page 16. Ball assignments and signal descriptions are shown in “Ball Assignments and Descriptions” on page 11.

The 1.5V DDR2 SDRAM provides essentially the same functional and operational performance as the JEDEC-standard, 1.8V DDR2 SDRAM, but offers a reduction in operating power in the range of 30 percent. Unless specifically noted, the 1.5V DDR2 SDRAM specifications meet the 1.8V DDR2 SDRAM timing specifications.

The 1.5V DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $4n$ -prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 1.5V DDR2 SDRAM effectively consists of a single  $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the 1.5V DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 1.5V DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the 1.5V DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The 1.5V DDR2 SDRAM provides for programmable READ or WRITE burst lengths of four or eight locations. 1.5V DDR2 SDRAM supports interrupting a burst READ of eight with another READ or a burst WRITE of eight with another WRITE. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of 1.5V DDR2 SDRAMs enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Inputs are generally compatible with the JEDEC standard for SSTL\_18. All full drive-strength outputs are generally SSTL\_18-compatible.



## General Notes

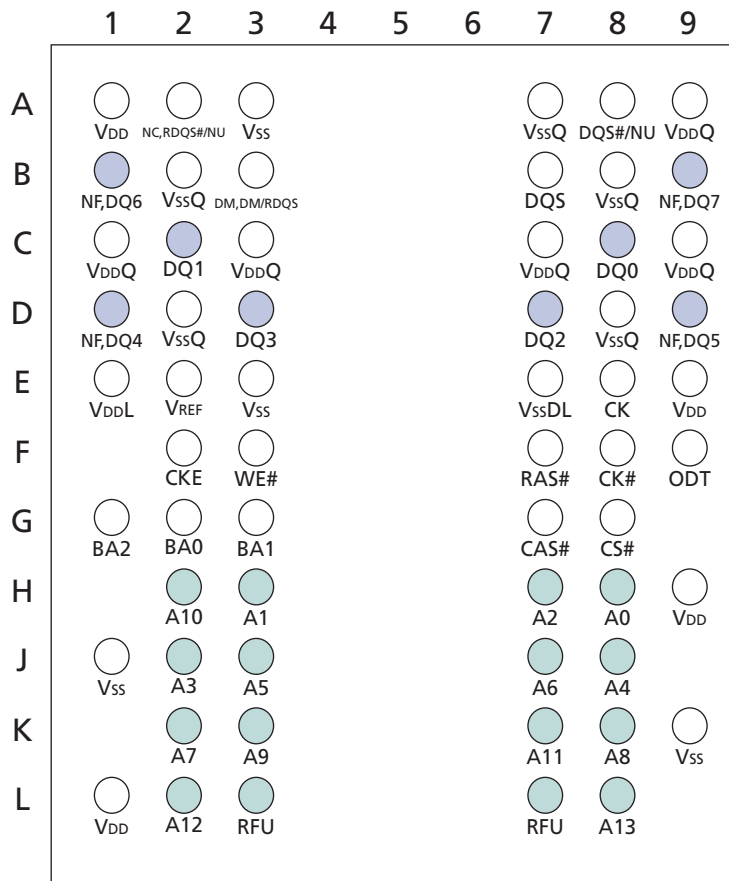
- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes, the lower byte and upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Ball Assignments and Descriptions

## Ball Assignments and Descriptions

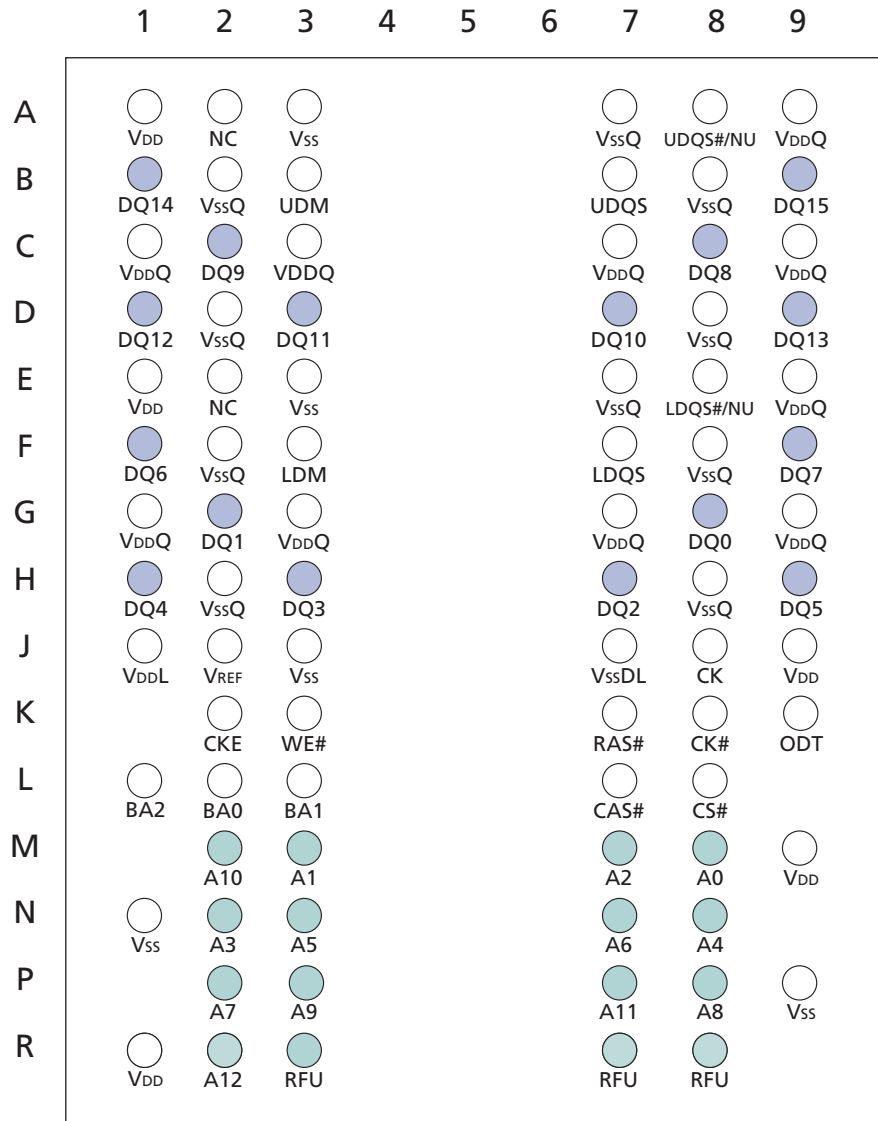
Figure 2: 60-Ball FBGA – x4, x8 Pin Assignments (Top View)





# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Ball Assignments and Descriptions

**Figure 3: 84-Ball FBGA – x16 Pin Assignments (Top View)**





## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Ball Assignments and Descriptions

**Table 3: FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions**

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2,	–	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA2–BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
–	H8, H3, H7, J2, J8, J3, J7, K2, K8, K3, H2, K7, L2, L8	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA2–BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
L2, L3, L1	G2, G3, G1	BA0, BA1 BA2	Input	<b>Bank address inputs:</b> BA0–BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
K9	F9	ODT	Input	<b>On-die termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
J8, K8	E8, F8	CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
K2	F2	CKE	Input	<b>Clock enable:</b> CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row active in any bank). CKE is synchronous for POWER-DOWN ENTRY, POWER-DOWN EXIT, OUTPUT DISABLE, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once VDD is applied during first power-up. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, VREF must be maintained.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Ball Assignments and Descriptions

**Table 3: FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions (continued)**

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
L8	G8	CS#	Input	<b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
F3, B3	B3	LDM, UDM DM	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
K7, L7, K3	F7, G7, F3	RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with CS#) define the command being entered.
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ2, DQ3–DQ5, DQ6–DQ8, DQ9–DQ11, DQ12–DQ14, DQ15	I/O	<b>Data input/output:</b> Bidirectional data bus for 64 Meg x 16.
–	C8, C2, D7, D3, D1, D9, B1, B9	DQ0–DQ2, DQ3–DQ5, DQ6–DQ7	I/O	<b>Data input/output:</b> Bidirectional data bus for 128 Meg x 8.
–	C8, C2, D7, D3	DQ0–DQ2, DQ3	I/O	<b>Data input/output:</b> Bidirectional data bus for 256 Meg x 4.
–	B7, A8	DQS, DQS#	I/O	<b>Data strobe:</b> Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7, E8	–	LDQS, LDQS#	I/O	<b>Data strobe for lower byte:</b> Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
B7, A8	–	UDQS, UDQS#	I/O	<b>Data strobe for upper byte:</b> Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B3, A2	RDQS, RDQS#	Output	<b>Redundant data strobe:</b> For 128 Meg x 8 only. RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, pin B3 becomes data mask (see DM pin). RDQS# is only used when RDQS is enabled <i>and</i> differential data strobe mode is enabled.
A1, E1, M9, R1, J9	A1, E9, L1, H9	VDD	Supply	<b>Power supply:</b> +1.5V –0.075V, +0.125V.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Ball Assignments and Descriptions

**Table 3: FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions (continued)**

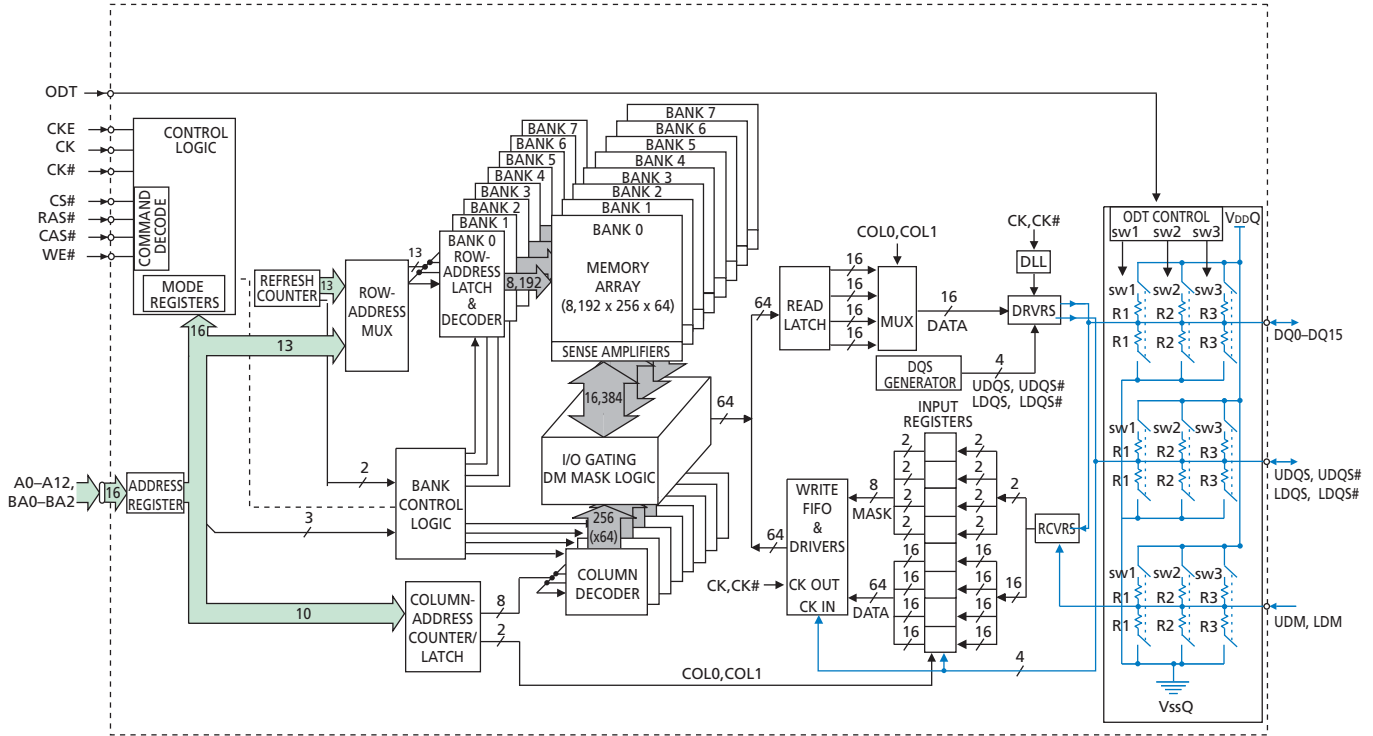
x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
A9, C1, C3, C7, C9, G3, E9, G1, G7, G9,	A9, C1, C3, C7, C9	VDDQ	Supply	<b>DQ power supply:</b> +1.5V –0.075V, +0.125V.
J1	E1	VDDL	Supply	<b>DLL power supply:</b> +1.5V –0.075V, +0.125V..
J2	E2	VREF	Supply	VDDQ/2 reference voltage.
A3, E3, J3, N1, P9	A3, E3, J1, K9	VSS	Supply	Ground.
J7	E7	VSSDL	Supply	<b>DLL ground:</b> Isolated on the device from VSS and VSSQ.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8	A7, B2, B8, D2, D8	VSSQ	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
A2, E2	–	NC	–	<b>No connect:</b> These pins should be left unconnected.
–	B1, B9, D1, D9	NF	–	<b>No function:</b> x8: these pins are used as DQ4–DQ7; x4: they are no function.
A8, E8	A2, A8	NU	–	<b>Not used:</b> If EMR[E10] = 0: x16, A8 = UDQS# and E8 = LDQS#; x8, A2 = RDQS# and A8 = DQS#; x4, A2 = NU and A8 = NU. If EMR[E10] = 1: x16, A8 = NU and E8 = NU; x8, A2 = NU and A8 = NU; x4, A2 = NU and A8 = NU.
R8, R3, R7	L3, L7	RFU	–	<b>Reserved for future use:</b> Row address bits A13 (x16 only), A14, and A15.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Functional Block Diagrams

## Functional Block Diagrams

Figure 4: 64 Meg x 16 Functional Block Diagram

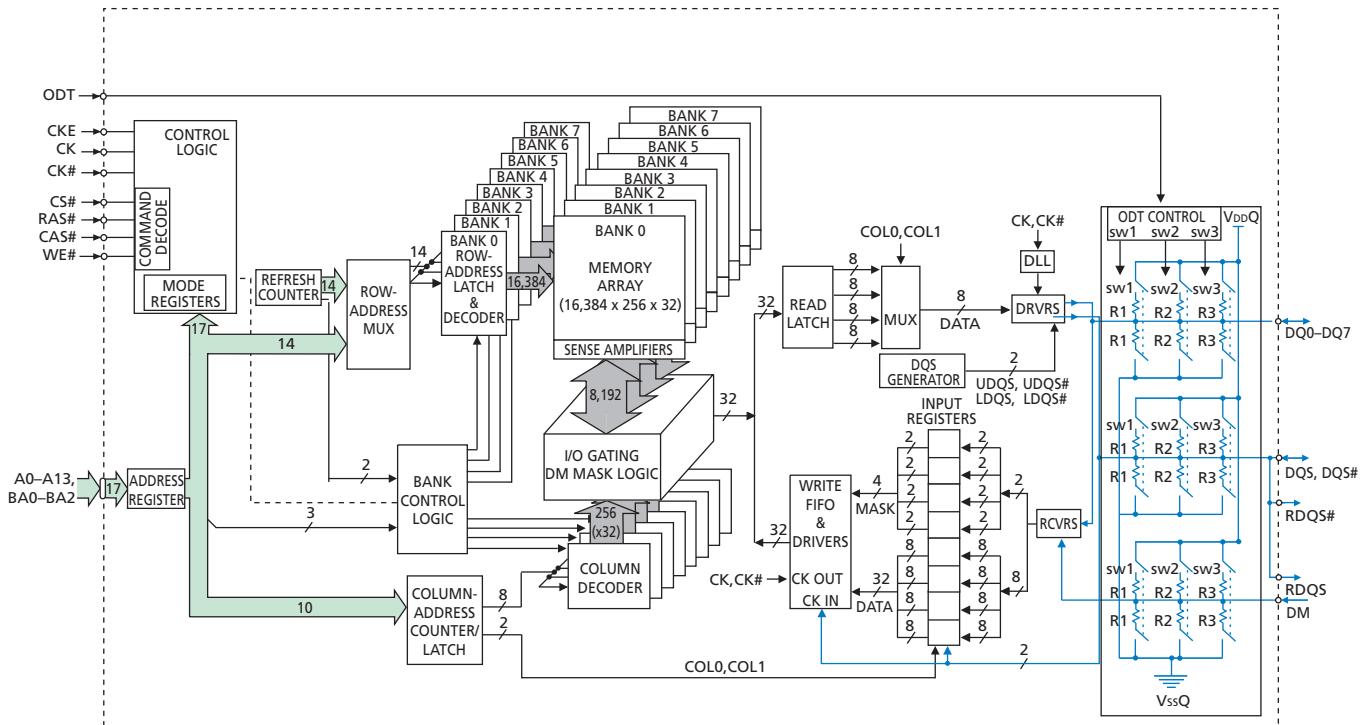




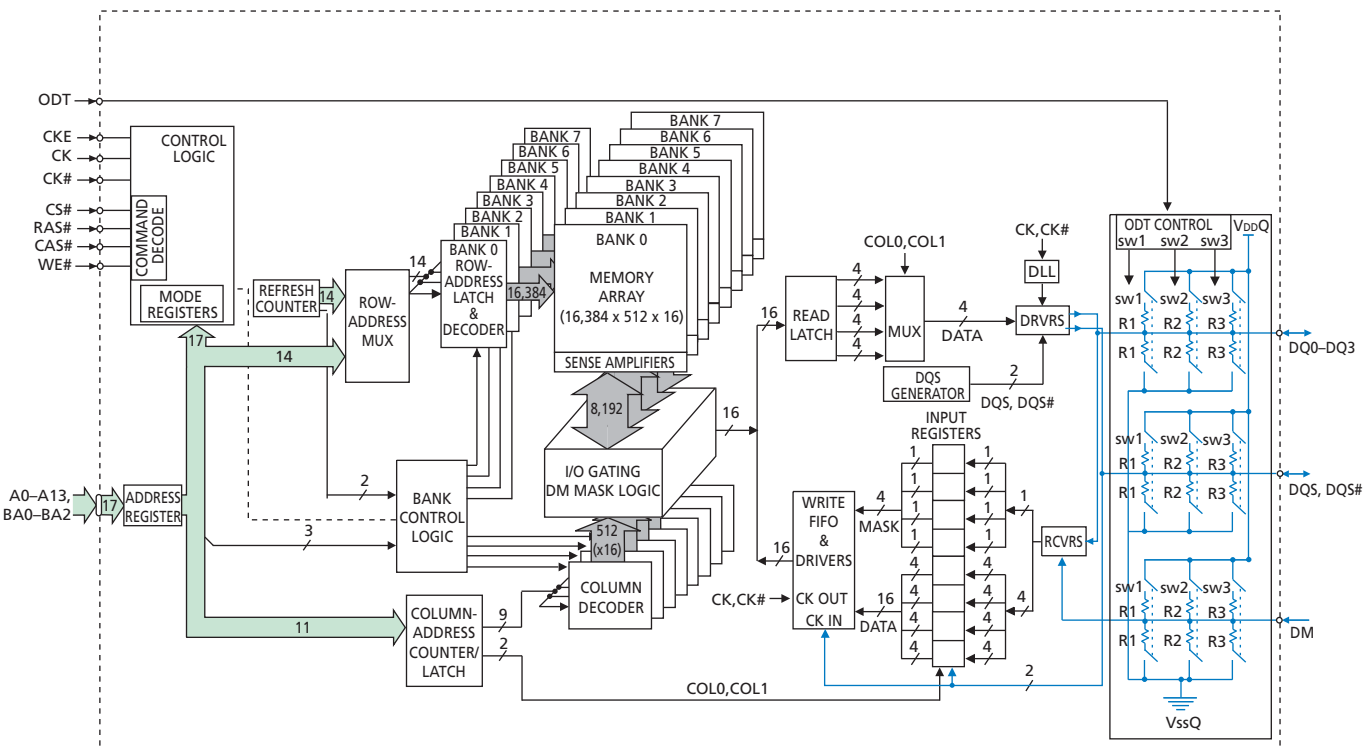


# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Functional Block Diagrams

**Figure 5: 128 Meg x 8 Functional Block Diagram**



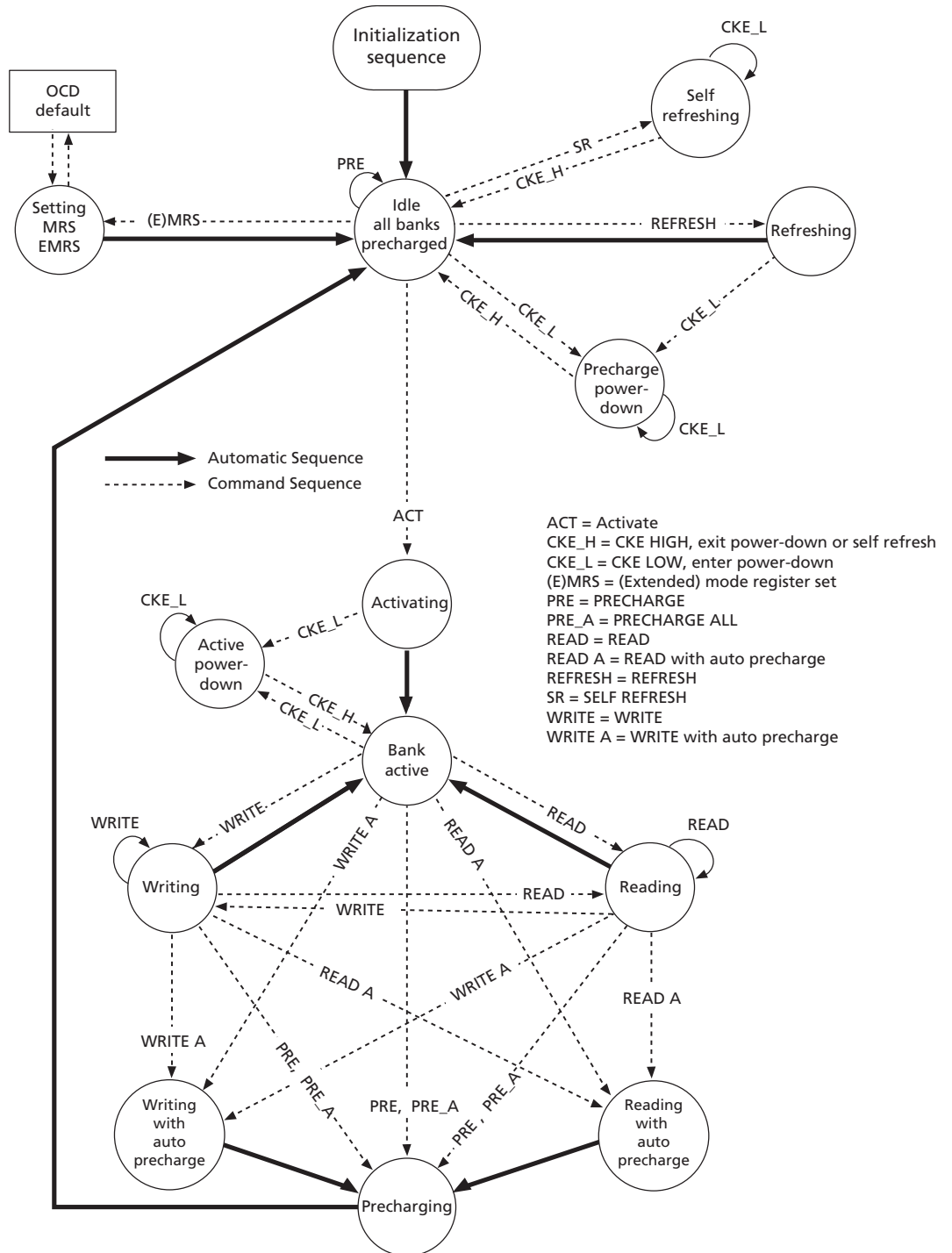
**Figure 6: 256 Meg x 4 Functional Block Diagram**





## State Diagram

Figure 7: Simplified State Diagram

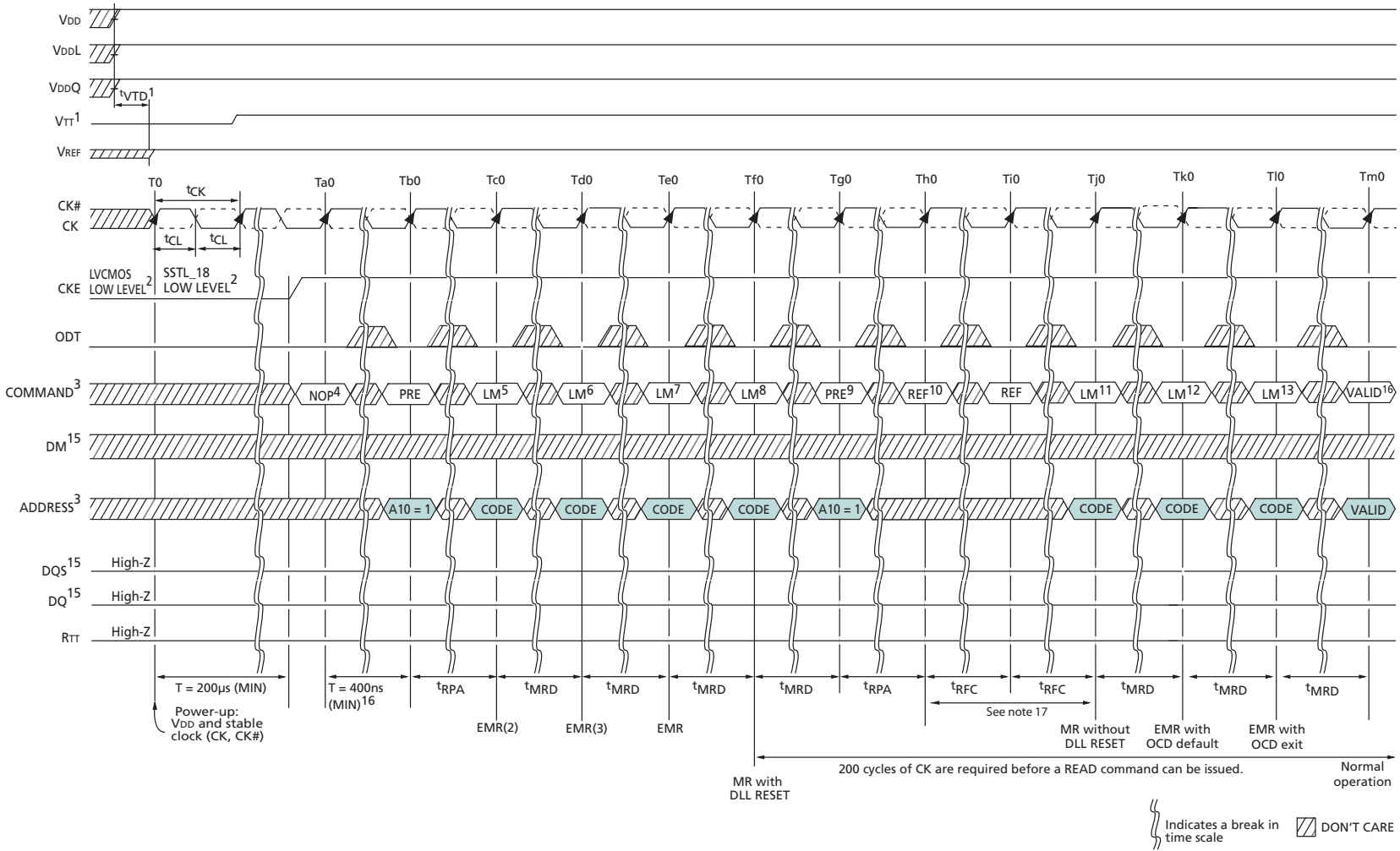


Notes: 1. This diagram provides the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions.

# Initialization

1.5V DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Figure 8 illustrates the sequence required for power-up and initialization.

**Figure 8: 1.5V DDR2 Power-Up and Initialization**





## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Initialization

- Notes:
1. Applying power; if CKE is maintained below  $0.2 \times V_{DDQ}$ , outputs remain disabled. To guarantee  $R_{TT}$  (ODT resistance) is off,  $V_{REF}$  must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined; I/Os and outputs must be less than  $V_{DDQ}$  during voltage ramp time to avoid 1.5V DDR2 SDRAM device latch-up).  $V_{TT}$  is not applied directly to the device; however,  $V_{TD}$  should be  $\leq 0$  to avoid device latch-up. At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as  $V_{DD}$ ,  $V_{DDL}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , and  $V_{TT}$  are between their minimum and maximum values as stated in Table 15 on page 81:
    - A) Single power source: The  $V_{DD}$  voltage ramp from 300mV to  $V_{DD}$  (MIN) must not exceed 200ms during the  $V_{DD}$  voltage ramp,  $|V_{DD} - V_{DDQ}| \leq 0.3V$ . Once supply voltage ramping is complete (when  $V_{DDQ}$  crosses  $V_{DD}$  [MIN]), Table 15 on page 81 specifications apply.
      - $V_{DD}$ ,  $V_{DDL}$ , and  $V_{DDQ}$  are driven from a single power converter output
      - $V_{TT}$  is limited to 0.95V MAX
      - $V_{REF}$  tracks  $V_{DDQ}/2$ ;  $V_{REF}$  must be within  $\pm 0.3V$  with respect to  $V_{DDQ}/2$  during supply ramp time
      - $V_{DDQ} \leq V_{REF}$  at all times
    - B) Multiple power sources:  $V_{DD} \leq V_{DDL} \leq V_{DDQ}$  must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes ( $V_{DDQ}$  crosses  $V_{DD}$  [MIN]). Once supply voltage ramping is complete, Table 15 on page 81 specifications apply.
      - Apply  $V_{DD}$  and  $V_{DDL}$  before or at the same time as  $V_{DDQ}$ ;  $V_{DD}/V_{DDL}$  voltage ramp time must be  $\leq 200ms$  from when  $V_{DD}$  ramps from 300mV to  $V_{DD}$  (MIN)
      - Apply  $V_{DDQ}$  before or at the same time as  $V_{TT}$ ; the  $V_{DDQ}$  voltage ramp time from when  $V_{DD}$  (MIN) is achieved to when  $V_{DDQ}$  (MIN) is achieved must be  $\leq 500ms$ ; while  $V_{DD}$  is ramping, current can be supplied from  $V_{DD}$  through the device to  $V_{DDQ}$
      - $V_{REF}$  must track  $V_{DDQ}/2$ ;  $V_{REF}$  must be within  $\pm 0.3V$  with respect to  $V_{DDQ}/2$  during supply ramp time;  $V_{DDQ} \leq V_{REF}$  must be met at all times
      - Apply  $V_{TT}$ ; the  $V_{TT}$  voltage ramp time from when  $V_{DDQ}$  (MIN) is achieved to when  $V_{TT}$  (MIN) is achieved must be no greater than 500ms
  2. CKE requires LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to  $V_{REF}$  being stable. After state T0, CKE is required to have SSTL<sub>18</sub> input levels. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
  3. PRE = PRECHARGE command, LM = LOAD MODE command, MR = Mode Register, EMR = extended mode register, EMR2 = extended mode register 2, EMR3 = extended mode register 3, REF = REFRESH command, ACT = ACTIVE command, A10 = PRECHARGE ALL, CODE = desired values for mode registers (bank addresses are required to be decoded), VALID = any valid command/address, RA = row address, bank address.
  4. For a minimum of 200 $\mu$ s after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
  5. Issue a LOAD MODE command to the EMR(2). To issue an EMR(2) command, provide LOW to BA0, and provide HIGH to BA1; set register E7 to "0" or "1" to select appropriate self refresh rate; remaining EMR(2) bits must be "0." See "Extended Mode Register 2" on page 30 for all EMR(2) requirements.
  6. Issue a LOAD MODE command to the EMR(3). To issue an EMR(3) command, provide HIGH to BA0 and BA1; remaining EMR(3) bits must be "0." See "Extended Mode Register 3" on page 31 for all EMR(3) requirements.
  7. Issue a LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0; provide HIGH to BA0; bits E7, E8, and E9 can be set to "0" or "1;" Micron recommends setting them to "0;" remaining EMR bits must be "0." See "Extended Mode Register (EMR)" on page 26 for all EMR requirements.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Initialization

8. Issue a LOAD MODE command to the MR for DLL RESET. 200 cycles of clock input is required to lock the DLL. To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1 and BA0; CKE must be HIGH the entire time the DLL is resetting; remaining MR bits must be "0." See "Mode Register (MR)" on page 22 for all MR requirements.
9. Issue PRECHARGE ALL command.
10. Issue two or more REFRESH commands.
11. Issue a LOAD MODE command to the MR with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL). To access the mode register MR, set BA0 and BA1 LOW; remaining MR bits must be set to desired settings. See "Mode Register (MR)" on page 22 for all MR requirements.
12. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters. To access the extended mode register EMR, set BA0 LOW and BA1 HIGH. See "Extended Mode Register (EMR)" on page 26 for all EMR requirements.
13. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. To access the extended mode registers, EMR, set BA0 LOW and BA1 HIGH. for all EMR requirements.
14. The 1.5V DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at Tf0.
15. DM represents DM for x4, x8 configurations and UDM, LDM for x16 configuration; DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16); DQ represents DQ0–DQ3 for x4, DQ–DQ7 for x8, and DQ0–DQ15 for x16.
16. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.



## Mode Register (MR)

The mode register is used to define the specific mode of operation of the 1.5V DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 9 on page 23. Contents of the mode register can be altered by reexecuting the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables must be programmed when the command is issued.

The MR is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

## Burst Length

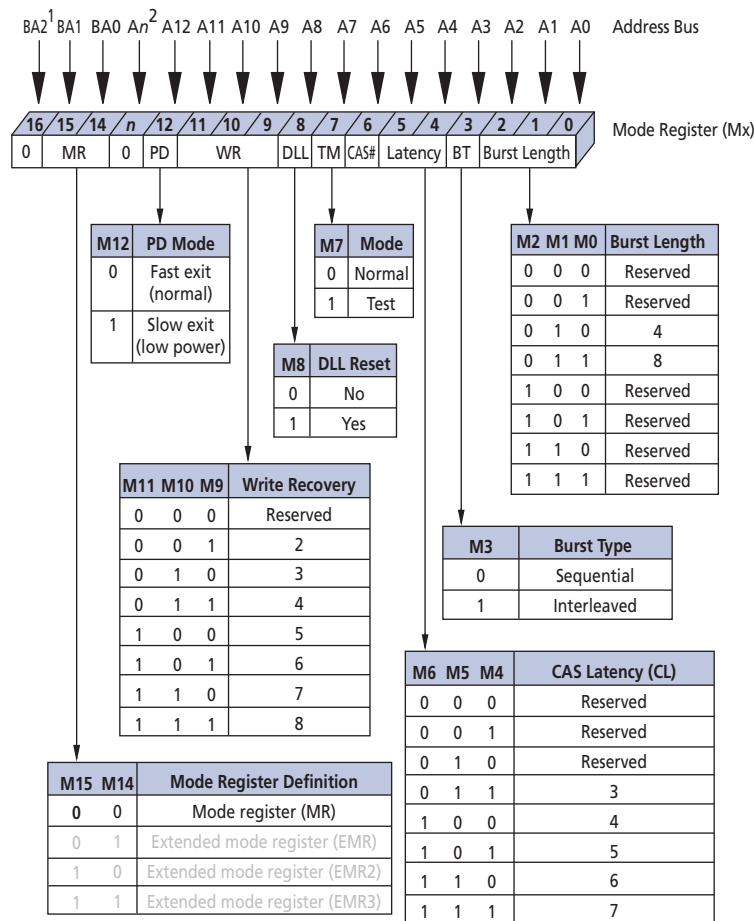
Burst length is defined by bits M0–M3, as shown in Figure 9 on page 23. Read and write accesses to the 1.5V DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by  $A2-A_i$  when  $BL = 4$  and by  $A3-A_i$  when  $BL = 8$  (where  $A_i$  is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Mode Register (MR)

**Figure 9: Mode Register (MR) Definition**



- Notes:
1. M16 (BA2) is only applicable for densities  $\geq$  1Gb, reserved for future use, and must be programmed to "0."
  2. Mode bits (M<sub>n</sub>) with corresponding address pins (A<sub>n</sub>) greater than M12 (A12) are reserved for future use and must be programmed to "0."
  3. Not all listed WR and CL options are supported in any individual speed grade.

## Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 9. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 4 on page 24. 1.5V DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleaved address ordering is supported; however, sequential address ordering is nibble-based.


**Table 4: Burst Definition**

Burst Length	Starting Column Address (A2, A1, A0)	Order of Accesses Within a Burst	
		Burst Type = Sequential	Burst Type = Interleaved
4	0 0	0, 1, 2, 3	0, 1, 2, 3
	0 1	1, 2, 3, 0	1, 0, 3, 2
	1 0	2, 3, 0, 1	2, 3, 0, 1
	1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

## Operating Mode

The normal operating mode is selected by issuing a command with bit M7 set to “0,” and all other bits set to the desired values, as shown in Figure 9 on page 23. When bit M7 is “1,” no other bits of the mode register are programmed. Programming bit M7 to “1” places the 1.5V DDR2 SDRAM into a test mode that is only used by the manufacturer and should *not* be used. No operation or functionality is guaranteed if M7 bit is “1.”

## DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 9 on page 23. Programming bit M8 to “1” will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of “0” after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to permit time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the  $t_{AC}$  or  $t_{DQCK}$  parameters.

## Write Recovery

Write recovery (WR) time is defined by bits M9–M11, as shown in Figure 9 on page 23. The WR register is used by the 1.5V DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the 1.5V DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of WRITE with auto precharge is shown in Figure 38 on page 58.

WR values of 2, 3, 4, 5, 6, 7, or 8 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing  $t_{WR}$  (in nanoseconds) by  $t_{CK}$  (in nanoseconds) and rounding up a noninteger value to the next integer;  $WR \text{ (cycles)} = t_{WR} \text{ (ns)} / t_{CK} \text{ (ns)}$ . Reserved states should not be used as unknown operation or incompatibility with future versions may result.





## Power-Down Mode

Active power-down (PD) mode is defined by bit M12, as shown in Figure 9 on page 23. PD mode enables the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode.

When bit M12 = 0, standard active PD mode, or “fast-exit” active PD mode, is enabled. The  $t_{XARD}$  parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode, or “slow-exit” active PD mode, is enabled. The  $t_{XARDS}$  parameter is used for slow-exit active PD exit timing. The DLL can be enabled but “frozen” during active PD mode since the exit-to-READ command timing is relaxed. The power difference expected between IDD3P normal and IDD3P low-power mode is defined in Table 41 on page 106.

## CAS Latency (CL)

The CAS latency (CL) is defined by bits M4–M6, as shown in Figure 9 on page 23. CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, 6, or 7 clocks, depending on the speed grade option being used.

1.5V DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as unknown operation otherwise incompatibility with future versions may result.

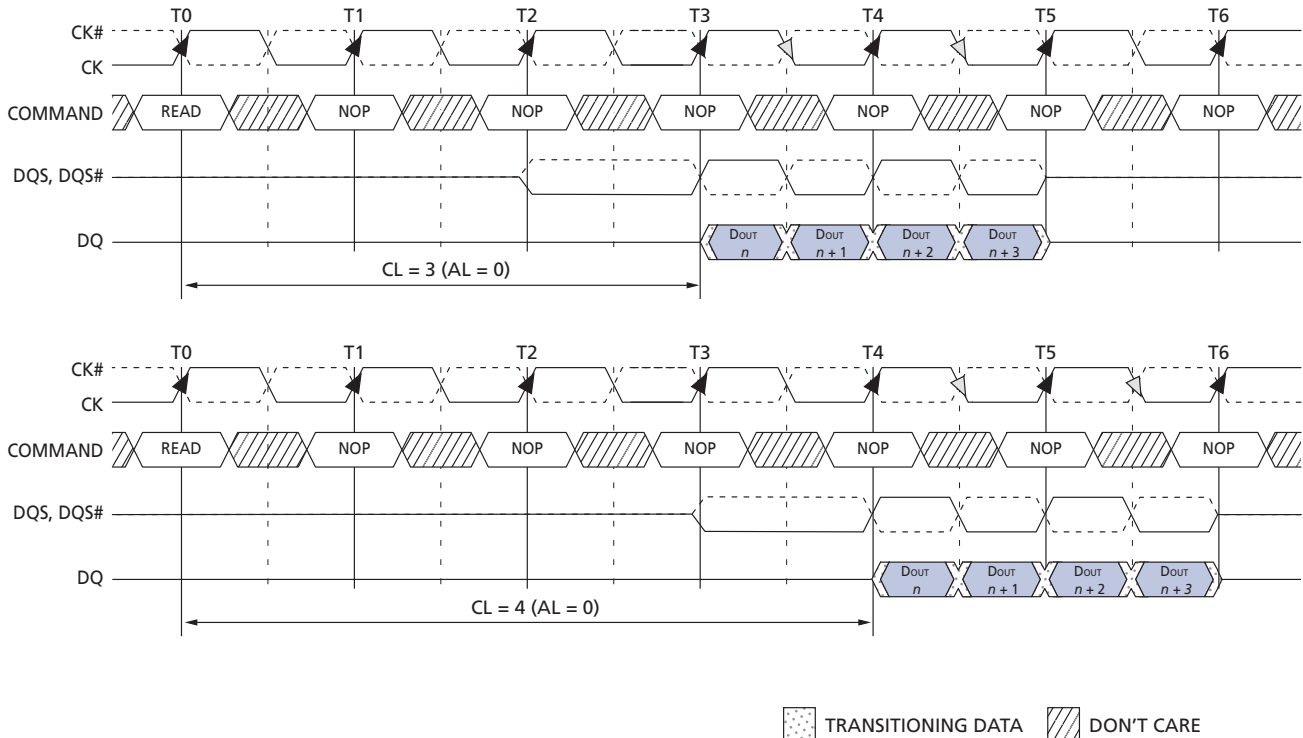
1.5V DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature enables the READ command to be issued prior to  $t_{RCD}(\text{MIN})$  by delaying the internal command to the 1.5V DDR2 SDRAM by AL clocks. The AL feature is described in more detail in “Posted CAS Additive Latency (AL)” on page 29.

Examples of CL = 3 and CL = 4 are shown in Figure 10 on page 26; both assume AL = 0. If a READ command is registered at clock edge  $n$ , and the CL is  $m$  clocks, the data will be available nominally coincident with clock edge  $n + m$  (this assumes AL = 0).



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Extended Mode Register (EMR)

**Figure 10: CAS Latency (CL)**



- Notes:
1. BL = 4.
  2. Posted CAS# additive latency (AL) = 0.
  3. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .

## Extended Mode Register (EMR)

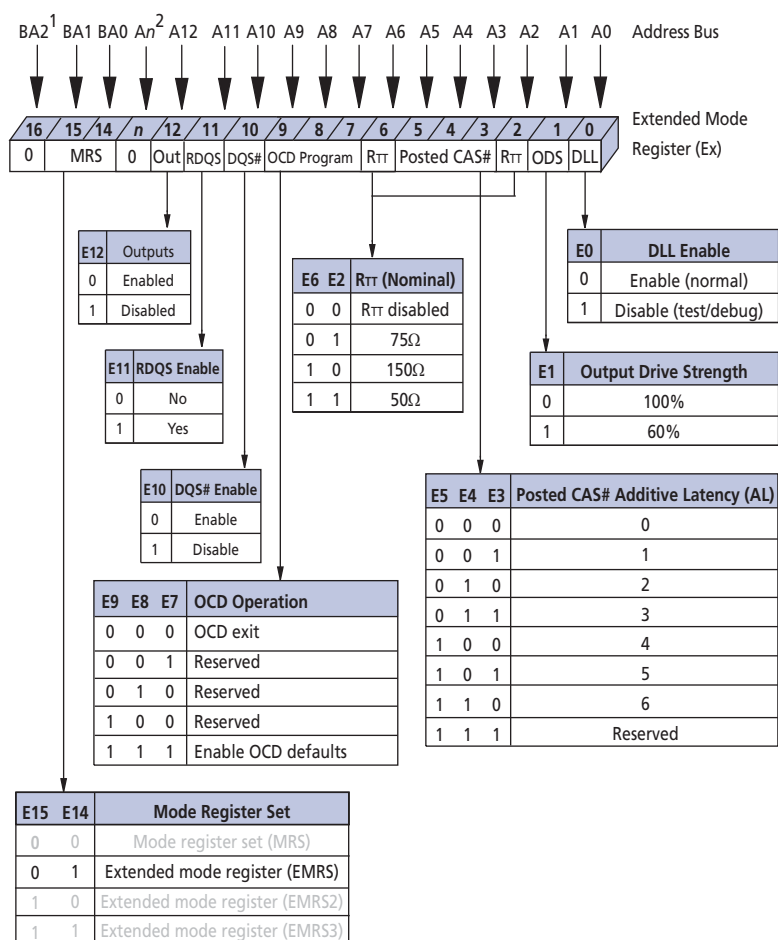
The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on-die termination (ODT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 11 on page 27. The EMR is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Extended Mode Register (EMR)

**Figure 11: Extended Mode Register Definition**



- Notes:
1. E16 (BA2) is only applicable for densities  $\geq 1\text{Gb}$ , reserved for future use, and must be programmed to "0."
  2. Mode bits ( $E_n$ ) with corresponding address pins ( $A_n$ ) greater than E12 (A12) are reserved for future use and must be programmed to "0."
  3. Not all listed AL options are supported in any individual speed grade.
  4. During initialization, all three bits must be set to "1" for OCD default state, then must be set to "0" before initialization is finished, as detailed in the notes on page 20.

## DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 11. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation.



Anytime the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to permit time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the  $t^{AC}$  or  $t^{DQCK}$  parameters.

## Output Drive Strength

The output drive strength is defined by bit E1, as shown in Figure 11 on page 27. The normal drive strength for all outputs are specified to be SSTL\_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 45 to 60 percent of the SSTL\_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

## DQS# Enable/Disable

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (E10 = 1), DQS is used in a single-ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

## RDQS Enable/Disable

The RDQS ball is enabled by bit E11, as shown in Figure 11 on page 27. This feature is only applicable to the x8 configuration. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the 1.5V DDR2 SDRAM.

## Output Enable/Disable

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 11 on page 27. When enabled (E12 = 0), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all 1.5V DDR2 SDRAM outputs (DQ, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during IDD characterization of read current.

## On-Die Termination (ODT)

ODT effective resistance,  $R_{TT}$  (EFF), is defined by bits E2 and E6 of the EMR, as shown in Figure 11 on page 27. The ODT feature is designed to improve signal integrity of the memory channel by enabling the 1.5V DDR2 SDRAM controller to independently turn on/off ODT for any or all devices.  $R_{TT}$  effective resistance values of 50Ω, 75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off “sw1,” “sw2,” or “sw3.” The ODT effective resistance value is selected by enabling switch “sw1,” which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω ( $R_{TT2}$  [EFF] = R2/2). Similarly, if “sw2” is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω ( $R_{TT2}$  [EFF] = R2/2). Switch “sw3” enables R1 values of 100Ω, enabling effective resistance of 50Ω. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Extended Mode Register (EMR)

The ODT control ball is used to determine when  $R_{TT}$  (EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation.

ODT must be turned off prior to entering self refresh mode. During power-up and initialization of the 1.5V DDR2 SDRAM, ODT should be disabled until issuing the EMR command to enable the ODT feature, at which point the ODT ball will determine the  $R_{TT}$  (EFF) value. Anytime the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled. See Figure 54 on page 75 for ODT timing diagrams.

### Off-Chip Driver (OCD) Impedance Calibration

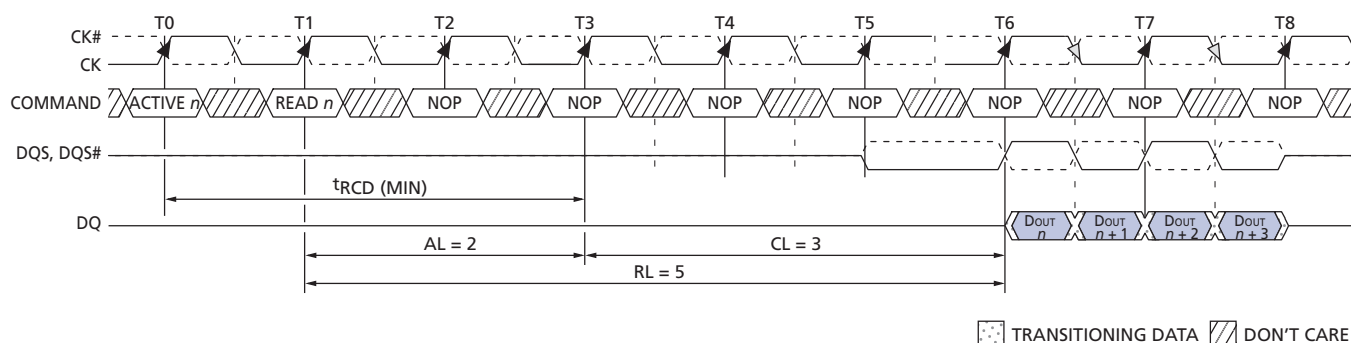
The OFF-CHIP DRIVER function is an optional 1.5V DDR2 JEDEC feature not supported by Micron and thereby must be set to the default state. Enabling OCD beyond the default settings will alter the I/O drive characteristics and the timing and output I/O specifications will no longer be valid. See “Initialization” on page 19 for proper setting of OCD defaults.

### Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in 1.5V DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 11 on page 27. Bits E3–E5 permit the user to program the 1.5V DDR2 SDRAM with an inverse AL of 0, 1, 2, 3, 4, 5, or 6 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the 1.5V DDR2 SDRAM allows a READ or WRITE command to be issued prior to  $t_{RCD}$  (MIN) with the requirement that  $AL \leq t_{RCD}$  (MIN). A typical application using this feature would set  $AL = t_{RCD}$  (MIN) -  $1 \times t_{CK}$ . The READ or WRITE command is held for the time of the AL before it is issued internally to the 1.5V DDR2 SDRAM device. RL is controlled by the sum of AL and CL;  $RL = AL + CL$ . Write latency (WL) is equal to RL minus one clock;  $WL = AL + CL - 1 \times t_{CK}$ . An example of RL is shown in Figure 12 on page 29. An example of a WL is shown in Figure 13 on page 30.

**Figure 12: READ Latency**

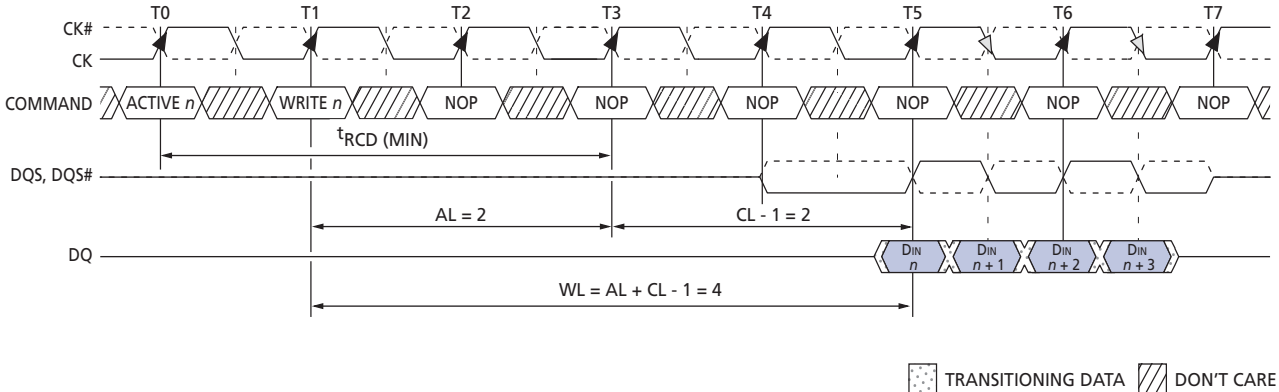


- Notes:
1. BL = 4.
  2. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .
  3.  $RL = AL + CL = 5$ .



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Extended Mode Register 2

Figure 13: WRITE Latency



- Notes:
1. BL = 4.
  2. CL = 3.
  3. WL = AL + CL - 1 = 4.

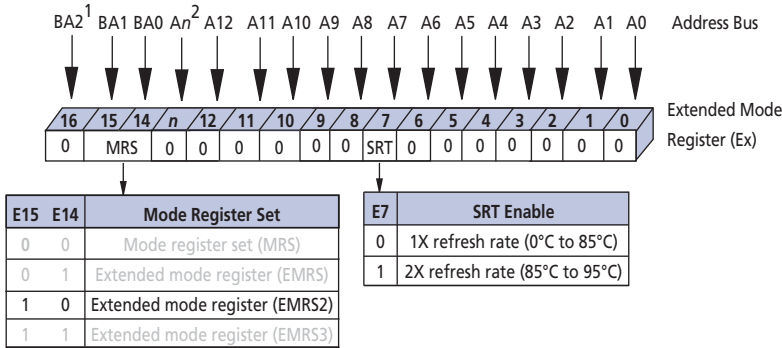
## Extended Mode Register 2

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, except for E7, which is used in commercial or high-temperature operations, as shown in Figure 14. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

Bit E7 (A7) must be programmed as “1” to provide a faster refresh rate if T<sub>C</sub> exceeds 85°C.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time <sup>t</sup>MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 14: Extended Mode Register 2 (EMR2) Definition



- Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to “0.”
  2. Mode bits (En) with corresponding address pins (An) greater than A12 (A12) are reserved for future use and must be programmed to “0.”

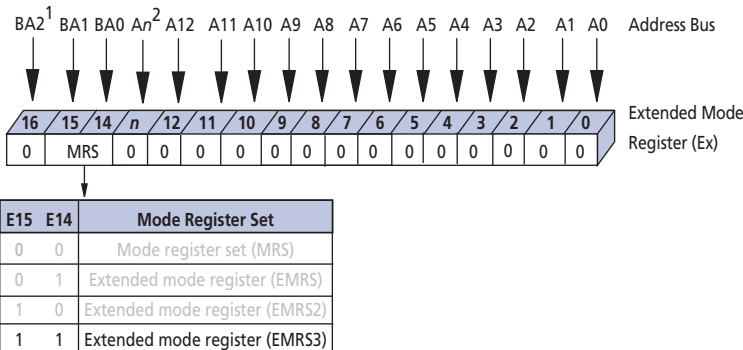


### Extended Mode Register 3

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved, as shown in Figure 15 on page 31. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time <sup>t</sup>MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 15: Extended Mode Register 3 (EMR3) Definition



- Notes:
1. E16 (BA2) is only applicable for densities  $\geq 1\text{Gb}$ , is reserved for future use, and must be programmed to "0."
  2. Mode bits (En) with corresponding address pins (An) greater than E12 (A12) are reserved for future use and must be programmed to "0."



## Command Truth Tables

The following tables provide a quick reference of 1.5V DDR2 SDRAM available commands, including CKE power-down modes and bank-to-bank commands.

**Table 5: Truth Table – 1.5V DDR2 Commands**

Notes: 1, 5, and 6 apply to the entire table

Function	CKE		CS#	RAS#	CAS#	WE#	BA2 <sup>8</sup> – BA0	An <sup>9</sup> –A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
LOAD MODE	H	H	L	L	L	L	BA	OP code			2
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH exit	L	H	H	X	X	X	X	X	X	X	7
			L	H	H	H					
Single bank PRECHARGE	H	H	L	L	H	L	BA	X	L	X	2
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank activate	H	H	L	L	H	H	BA	Row address			
WRITE	H	H	L	H	L	L	BA	Column address	L	Column address	2, 3, 9
WRITE with auto precharge	H	H	L	H	L	L	BA	Column address	H	Column address	2, 3, 9
READ	H	H	L	H	L	H	BA	Column address	L	Column address	2, 3, 9
READ with auto precharge	H	H	L	H	L	H	BA	Column address	H	Column address	2, 3, 9
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
Power-down entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H					
Power-down exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H					

- Notes:
- All 1.5V DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
  - Bank addresses (BA) determine which bank is to be operated upon. BA during a LM command selects which mode register is programmed.
  - Burst reads or writes at BL = 4 cannot be terminated or interrupted. See Figure 21 on page 42 and Figure 34 on page 54 for other restrictions and details.
  - The power-down mode does not perform any REFRESH operations. The duration of power-down is limited by the refresh requirements outlined in the AC parametric section.
  - The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See "ODT Timing" on page 74 for details.
  - "X" means "H or L" (but a defined logic level) for valid IDD measurements.
  - SELF REFRESH exit is asynchronous.
  - BA2 is only applicable for densities  $\geq 1\text{Gb}$ .
  - An is the most significant address bit for a given density and configuration. Some larger address bits may be "Don't Care" during column addressing, depending on density and configuration.




**Table 6: Truth Table – Current State Bank *n* – Command to Bank *n***

Notes: 1–6 apply to the entire table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row active	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto-precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9, 10
	L	L	H	L	PRECHARGE (start PRECHARGE)	8
Write (auto-precharge disabled)	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (start PRECHARGE)	8

- Notes:
- This table applies when  $CKE_{n-1}$  was HIGH and  $CKE_n$  is HIGH and after  $t_{XSNR}$  has been met (if the previous state was self refresh).
  - This table is bank-specific, except where noted (the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
  - Current state definitions:
    - Idle:** The bank has been precharged,  $t_{RP}$  has been met, and any READ burst is complete.
    - Row active:** A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress.
    - Read:** A READ burst has been initiated, with auto precharge disabled and has not yet terminated.
    - Write:** A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.
  - The following states must not be interrupted by a command issued to the same bank. Issue DESELECT or NOP commands, or allowable commands to the other bank, on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to Table 7 on page 35.
    - Precharge:** Starts with registration of a PRECHARGE command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, the bank will be in the idle state.
    - Read with auto precharge enabled:** Starts with registration of a READ command with auto precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.
    - Row activate:** Starts with registration of an ACTIVE command and ends when  $t_{RCD}$  is met. Once  $t_{RCD}$  is met, the bank will be in the row active state.
    - Write with auto precharge enabled:** Starts with registration of a WRITE command with auto precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Command Truth Tables

5. The following states must not be interrupted by any executable command (DESELECT or NOP commands must be applied on each positive clock edge during these states):
  - Refresh:** Starts with registration of a REFRESH command and ends when  $t_{RFC}$  is met. Once  $t_{RFC}$  is met, the 1.5V DDR2 SDRAM will be in the all banks idle state.
  - Accessing mode register:** Starts with registration of the LM command and ends when  $t_{MRD}$  has been met. Once  $t_{MRD}$  is met, the 1.5V DDR2 SDRAM will be in the all banks idle state.
  - Precharge all:** Starts with registration of a PRECHARGE ALL command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. A WRITE command may be applied after the completion of the READ burst.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Command Truth Tables

**Table 7: Truth Table – Current State Bank  $n$  – Command to Bank  $m$**

Notes: 1–6 apply to the entire table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank $m$	
Row active, active, or precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto-precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (with auto-precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	

- Notes:
- This table applies when  $CKE_{n-1}$  was HIGH and  $CKE_n$  is HIGH and after  $t_{XSNR}$  has been met (if the previous state was self refresh).
  - This table describes alternate bank operation, except where noted (the current state is for bank  $n$  and the commands shown are those allowed to be issued to bank  $m$ , assuming that bank  $m$  is in such a state that the given command is allowable). Exceptions are covered in the notes below.
  - Current state definitions:
    - Idle:** The bank has been precharged,  $t_{RP}$  has been met, and any READ burst is complete.
    - Row active:** A row in the bank has been activated and  $t_{RCD}$  has been met. No data bursts/ accesses and no register accesses are in progress.
    - Read:** A READ burst has been initiated with auto precharge disabled and has not yet terminated.
    - Write:** A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Command Truth Tables

**READ with auto precharge enabled/ WRITE with auto precharge enabled:** The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For WRITE with auto precharge, the precharge period begins when  $t_{WR}$  ends, with  $t_{WR}$  measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or  $t_{RP}$ ) begins. This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (contention between read data and write data must be avoided).

The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized in Table 8:

**Table 8: Minimum Delay with Auto Precharge Enabled**

From Command (Bank <i>n</i> )	To Command (Bank <i>m</i> )	Minimum Delay (with Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ with auto precharge	$(CL - 1) + (BL/2) + t_{WTR}$	$t_{CK}$
	WRITE or WRITE with auto precharge	$(BL/2)$	$t_{CK}$
	PRECHARGE or ACTIVE	1	$t_{CK}$
READ with auto precharge	READ or READ with auto precharge	$(BL/2)$	$t_{CK}$
	WRITE or WRITE with auto precharge	$(BL/2) + 2$	$t_{CK}$
	PRECHARGE or ACTIVE	1	$t_{CK}$

4. REFRESH and LM commands may only be issued when all banks are idle.
5. Not used.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM.
9. A WRITE command may be applied after the completion of the READ burst.
10. The number of clock cycles required to meet  $t_{WTR}$  is either 2 or  $t_{WTR}/t_{CK}$ , whichever is greater.



## DESELECT, NOP, and LM Commands

### DESELECT

The Deselect function (CS# HIGH) prevents new commands from being executed by the 1.5V DDR2 SDRAM. The 1.5V DDR2 SDRAM is effectively deselected. Operations already in progress are not affected. Deselect is also referred to as COMMAND INHIBIT.

### NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected 1.5V DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

### LOAD MODE (LM)

The mode registers are loaded via bank address and address inputs. The bank address pins determine which mode register will be programmed. See “Mode Register (MR)” on page 22. The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until  $t_{MRD}$  is met.

## Bank/Row Activation

### ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the bank address inputs determines the bank, and the address inputs select the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

### ACTIVE Operation

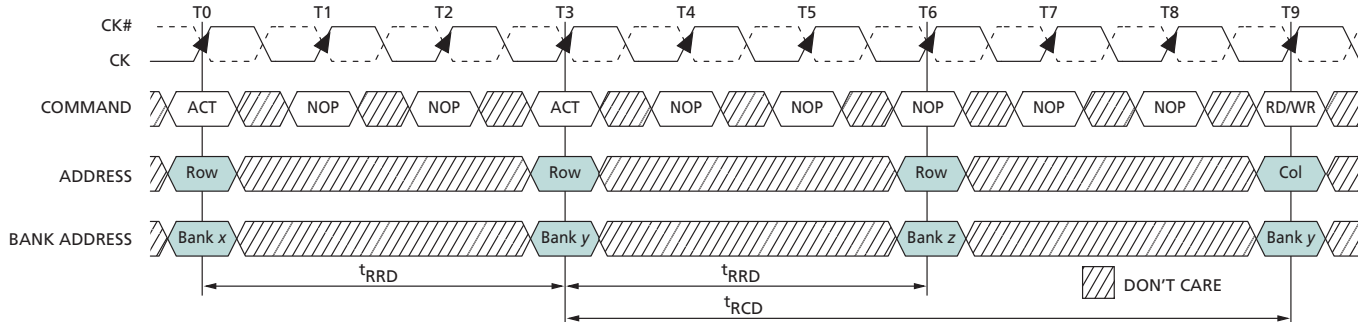
Before any READ or WRITE commands can be issued to a bank within the 1.5V DDR2 SDRAM, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row subject to the  $t_{RCD}$  specification.  $t_{RCD}(\text{MIN})$  should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a  $t_{RCD}(\text{MIN})$  specification of 20ns with a 266 MHz clock ( $t_{CK} = 3.75\text{ns}$ ) results in 5.3 clocks, rounded up to 6. This is reflected in Figure 16 on page 38, which covers any case where  $5 < t_{RCD}(\text{MIN})/t_{CK} \leq 6$ . Figure 16 also shows the case for  $t_{RRD}$  where  $2 < t_{RRD}(\text{MIN})/t_{CK} \leq 3$ .



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

**Figure 16: Example: Meeting  $t_{RRD}^{(MIN)}$  and  $t_{RCD}^{(MIN)}$**

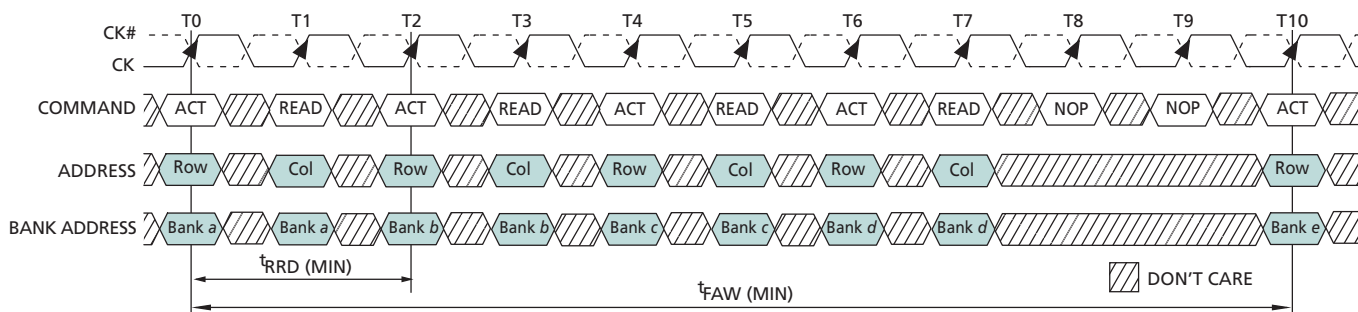


A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by  $t_{RC}$ .

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by  $t_{RRD}$ .

1.5V DDR2 devices with 8-banks (1Gb or larger) have an additional  $t_{FAW}$  timing requirement. This requires no more than four ACTIVE commands to be issued in any given  $t_{FAW}^{(MIN)}$  period, as shown in Figure 17.

**Figure 17: Multibank Activate Restriction**



Notes: 1. 1.5V DDR2-533 (-37E, x4 or x8),  $t_{CK} = 3.75ns$ , BL = 4, AL = 3, CL = 4,  $t_{RRD}^{(MIN)} = 7.5ns$ ,  $t_{FAW}^{(MIN)} = 37.5ns$ .

## READ Command

The READ command is used to initiate a burst read access to an active row. The value on the bank address inputs determine the bank, and the address provided on address inputs A0-i (where  $A_i$  is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.



1.5V DDR2 SDRAM also supports the AL feature, which permits a READ or WRITE command to be issued prior to  $t^{\text{RCD}}(\text{MIN})$  by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

## READ Operation

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL;  $RL = AL + CL$ . The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 18 on page 40 shows examples of RL based on different AL and CL settings.

DQS/DQS# is driven by the 1.5V DDR2 SDRAM along with output data. The initial LOW state on DQS and HIGH state on DQS# is known as the read preamble ( $t^{\text{RPRE}}$ ). The LOW state on DQS and HIGH state on DQS# coincident with the last data-out element is known as the read postamble ( $t^{\text{RPST}}$ ).

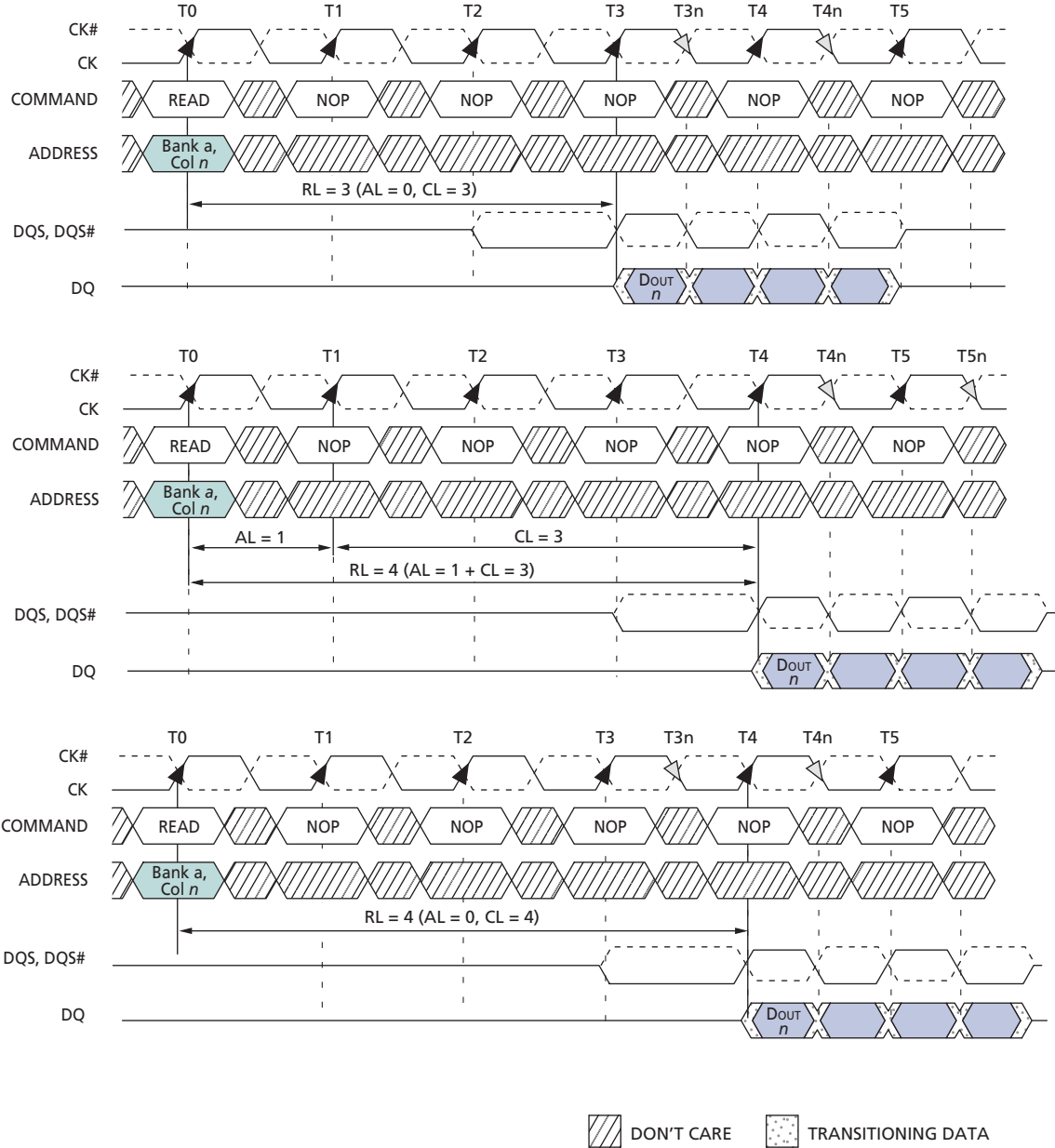
Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of  $t^{\text{DQSQ}}$  (valid data-out skew),  $t^{\text{QH}}$  (data-out window hold), and the valid data window are depicted in Figure 27 on page 47 and Figure 28 on page 48. A detailed explanation of  $t^{\text{DQSCK}}$  (DQS transition skew to CK) and  $t^{\text{AC}}$  (data-out transition skew to CK) is shown in Figure 29 on page 49.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued  $x$  cycles after the first READ command, where  $x$  equals  $BL/2$  cycles. This is shown in Figure 19 on page 41.



1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
READ Command

Figure 18: READ Latency



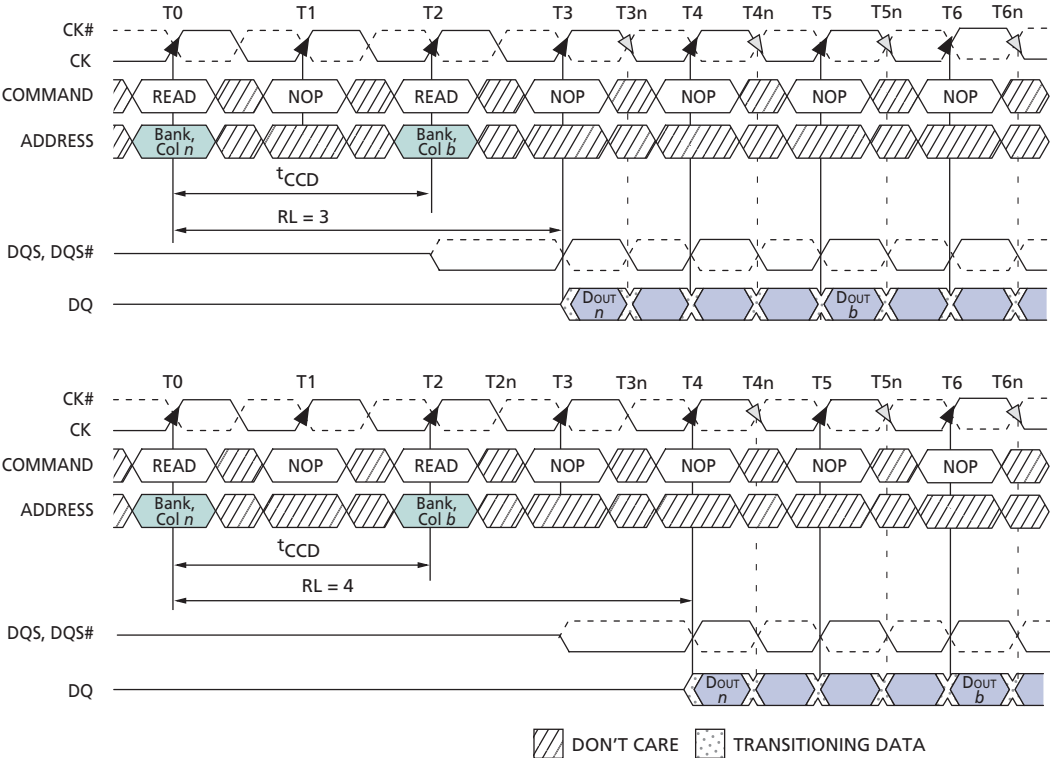
- Notes:
1. DOUT n = data-out from column n.
  2. BL = 4.
  3. Three subsequent elements of data-out appear in the programmed order following DOUT n.
  4. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .





1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

Figure 19: Consecutive READ Bursts



- Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
  2. BL = 4.
  3. Three subsequent elements of data-out appear in the programmed order following DOUT *n*.
  4. Three subsequent elements of data-out appear in the programmed order following DOUT *b*.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .
  6. Example applies only when READ commands are issued to same device.

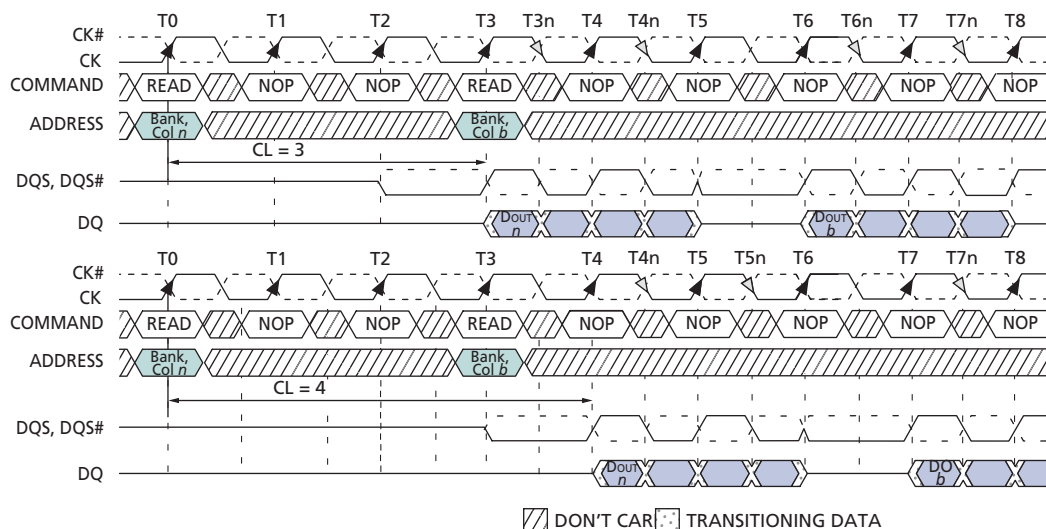
Nonconsecutive read data is illustrated in Figure 20 on page 42. Full-speed random read accesses within a page (or pages) can be performed. 1.5V DDR2 SDRAM supports the use of concurrent auto precharge timing, shown in Table 9 on page 43.

1.5V DDR2 SDRAM does not permit interrupting or truncating of any READ burst using BL = 4 operations. Once the BL = 4 READ command is registered, it must be allowed to complete the entire READ burst. However, a READ (with auto precharge disabled) using BL = 8 operation may be interrupted and truncated *only* by another READ burst as long as the interruption occurs on a 4-bit boundary due to the 4*n* prefetch architecture of 1.5V DDR2 SDRAM. READ burst BL = 8 operations may not be interrupted or truncated with any command except another READ command, as shown in Figure 21 on page 42.



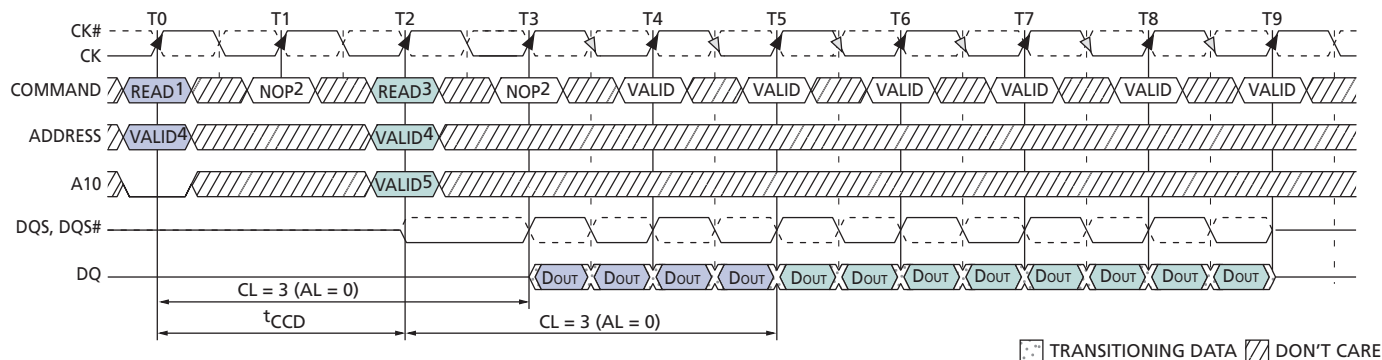
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

**Figure 20: Nonconsecutive READ Bursts**



- Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
  2. BL = 4.
  3. Three subsequent elements of data-out appear in the programmed order following DOUT *n*.
  4. Three subsequent elements of data-out appear in the programmed order following DOUT *b*.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCk}$ , and  $t_{DQSQ}$ .
  6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

**Figure 21: READ Interrupted by READ**



- Notes:
1. BL = 8 required; auto precharge must be disabled (A10 = LOW).
  2. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for READs at T0 and T2.
  3. Interrupting READ command must be issued exactly  $2 \times t_{CK}$  from previous READ.
  4. READ command can be issued to any valid bank and row address (READ command at T0 and T2 can be either same bank or different bank).
  5. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting READ command.
  6. Example shown uses AL = 0; CL = 3, BL = 8, shown with nominal  $t_{AC}$ ,  $t_{DQSCk}$ , and  $t_{DQSQ}$ .


**Table 9: READ Using Concurrent Auto Precharge**

From Command (Bank <i>n</i> )	To Command (Bank <i>m</i> )	Minimum Delay (with Concurrent Auto Precharge)	Units
READ with auto precharge	READ or READ with auto precharge	BL/2	<sup>t</sup> CK
	WRITE or WRITE with auto precharge	(BL/2) + 2	<sup>t</sup> CK
	PRECHARGE or ACTIVE	1	<sup>t</sup> CK

Data from any READ burst must be completed before a subsequent WRITE burst is permitted. An example of a READ burst followed by a WRITE burst is shown in Figure 24 on page 44. The <sup>t</sup>DQSS (MIN) case is shown; the <sup>t</sup>DQSS (MAX) case has a longer bus idle time. (<sup>t</sup>DQSS [MIN] and <sup>t</sup>DQSS [MAX] are defined in Figure 30 on page 52.)

A READ burst may be followed by a PRECHARGE command to the same bank, provided that auto precharge was not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is AL + BL/2 clocks and must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ-to-PRECHARGE command. This READ-to-PRECHARGE time is called <sup>t</sup>RTP. For BL = 4 this is the time from the actual READ (AL after the READ command) to PRECHARGE command. For BL = 8 this is the time from AL + 2CK after the READ-to-PRECHARGE command. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until <sup>t</sup>RP is met.

**Note:** Part of the row precharge time is hidden during the access of the last data elements.

Examples of READ-to-PRECHARGE are shown in Figure 22 on page 44 for BL = 4 and Figure 23 on page 44 for BL = 8. The delay from READ-to-PRECHARGE command to the same bank is AL + BL/2 + MAX (<sup>t</sup>RTP/<sup>t</sup>CK or 2CK) - 2CK.

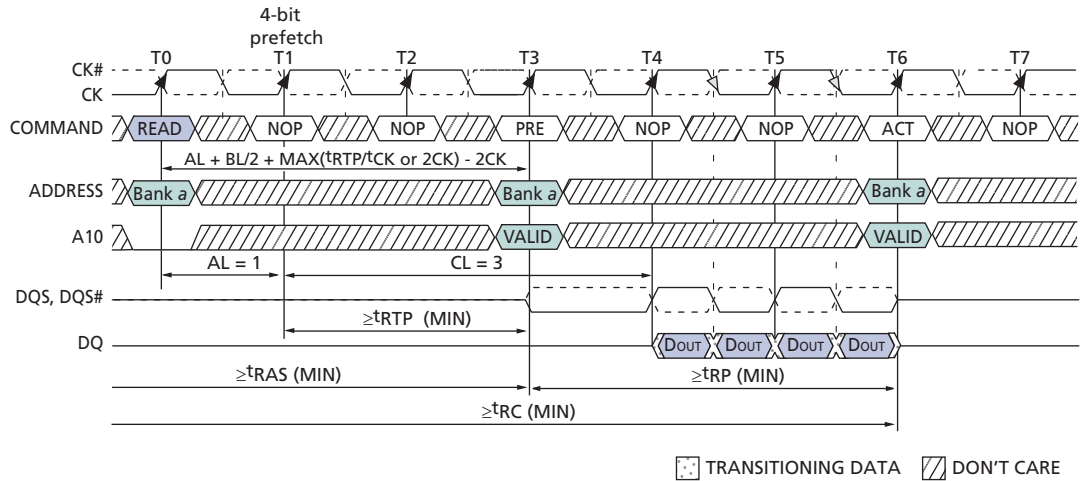
If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The 1.5V DDR2 SDRAM starts an auto precharge operation on the rising edge, which is AL + (BL/2) cycles later than the READ with AUTO PRECHARGE command if <sup>t</sup>RAS (MIN) and <sup>t</sup>RTP are satisfied. If <sup>t</sup>RAS (MIN) is not satisfied at the edge, the start point of auto precharge operation will be delayed until <sup>t</sup>RAS (MIN) is satisfied. If <sup>t</sup>RTP (MIN) is not satisfied at the edge, the start point of the auto precharge operation will be delayed until <sup>t</sup>RTP (MIN) is satisfied. In case the internal precharge is pushed out by <sup>t</sup>RTP, <sup>t</sup>RP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). For BL = 4, the minimum time from READ with auto precharge to the next ACTIVATE command becomes AL + (<sup>t</sup>RTP + <sup>t</sup>RP)\*, shown in Figure 22 on page 44; for BL = 8, the time from READ with auto precharge to the next ACTIVATE command is AL + 2 clocks + (<sup>t</sup>RTP + <sup>t</sup>RP)\*, shown in Figure 23 on page 44.

**Note:** The asterisk (\*) indicates each parameter term is divided by <sup>t</sup>CK and rounded up to the next integer. In any event, internal precharge does not start earlier than two clocks after the last 4-bit prefetch.



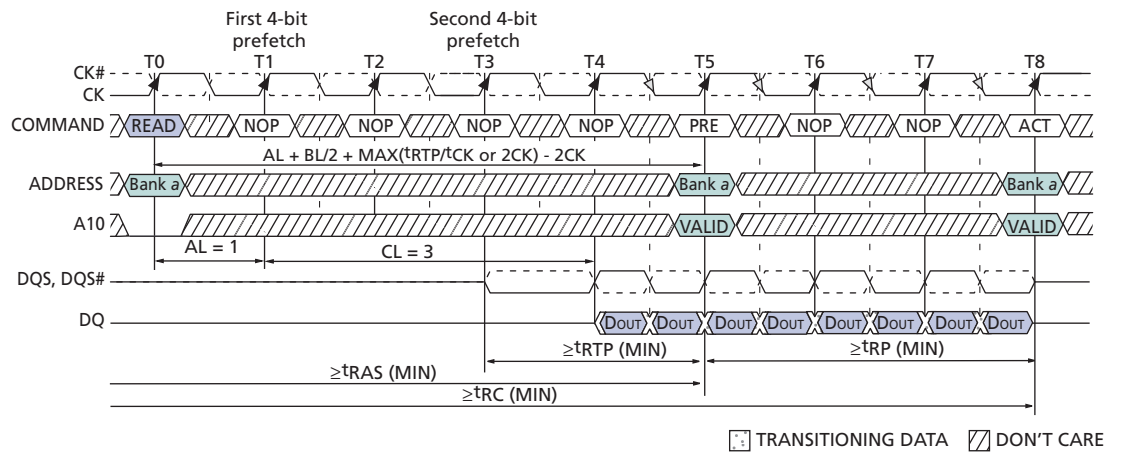
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

**Figure 22: READ-to-PRECHARGE – BL = 4**



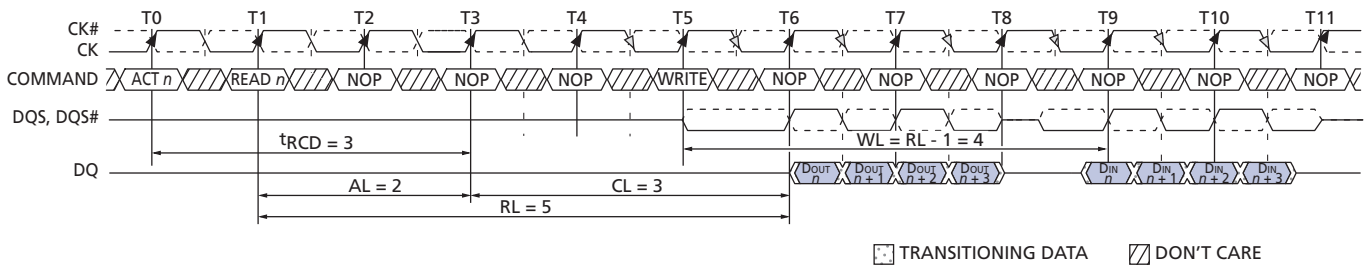
- Notes:
1. RL = 4 (AL = 1, CL = 3); BL = 4.
  2.  $t_{RTP} \geq 2$  clocks.
  3. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .

**Figure 23: READ-to-PRECHARGE – BL = 8**



- Notes:
1. RL = 4 (AL = 1, CL = 3); BL = 8.
  2.  $t_{RTP} \geq 2$  clocks.
  3. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .

**Figure 24: READ-to-WRITE**

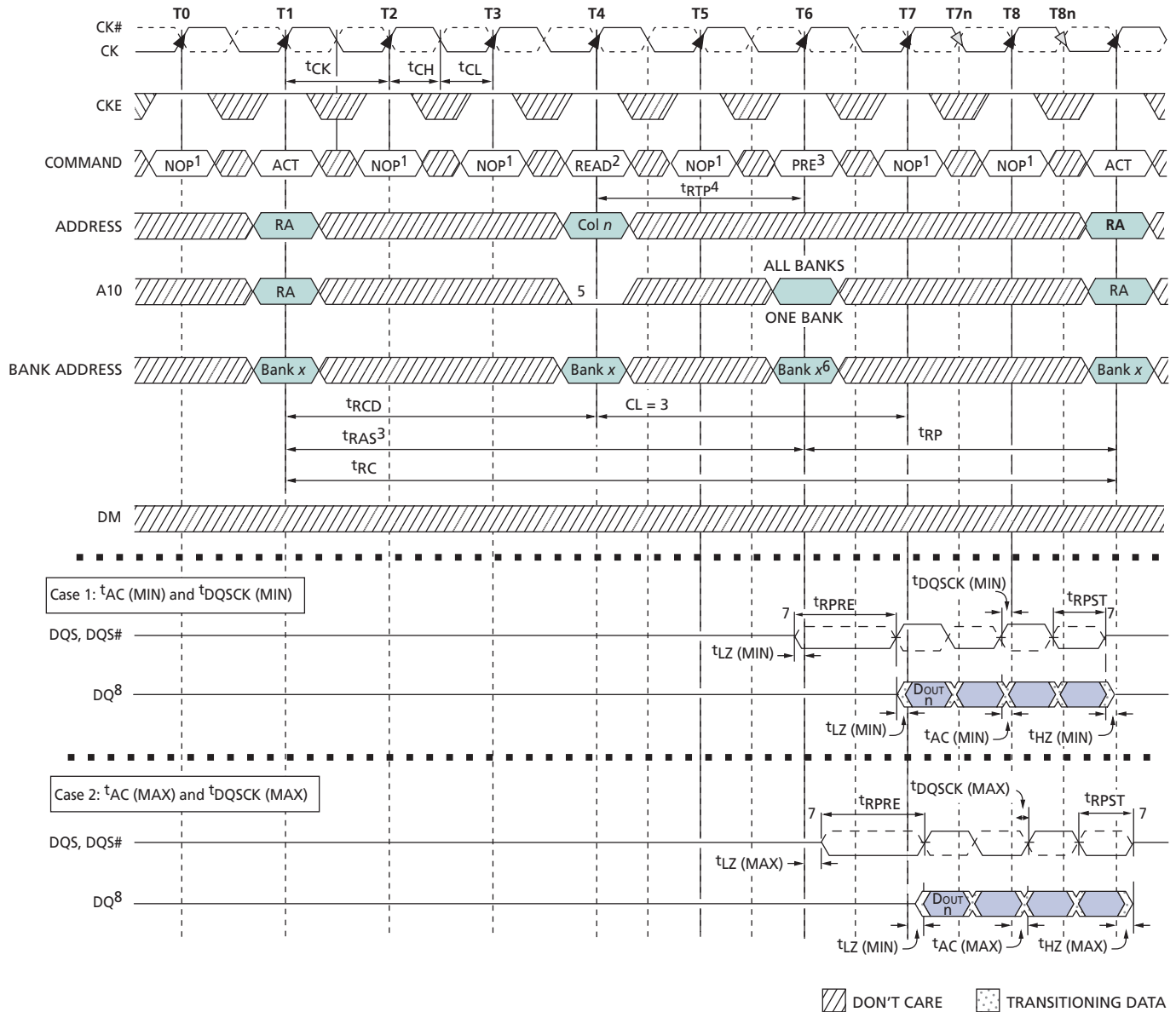


- Notes:
1. BL = 4; CL = 3; AL = 2.
  2. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .



**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
READ Command**

**Figure 25: Bank Read – Without Auto Precharge**

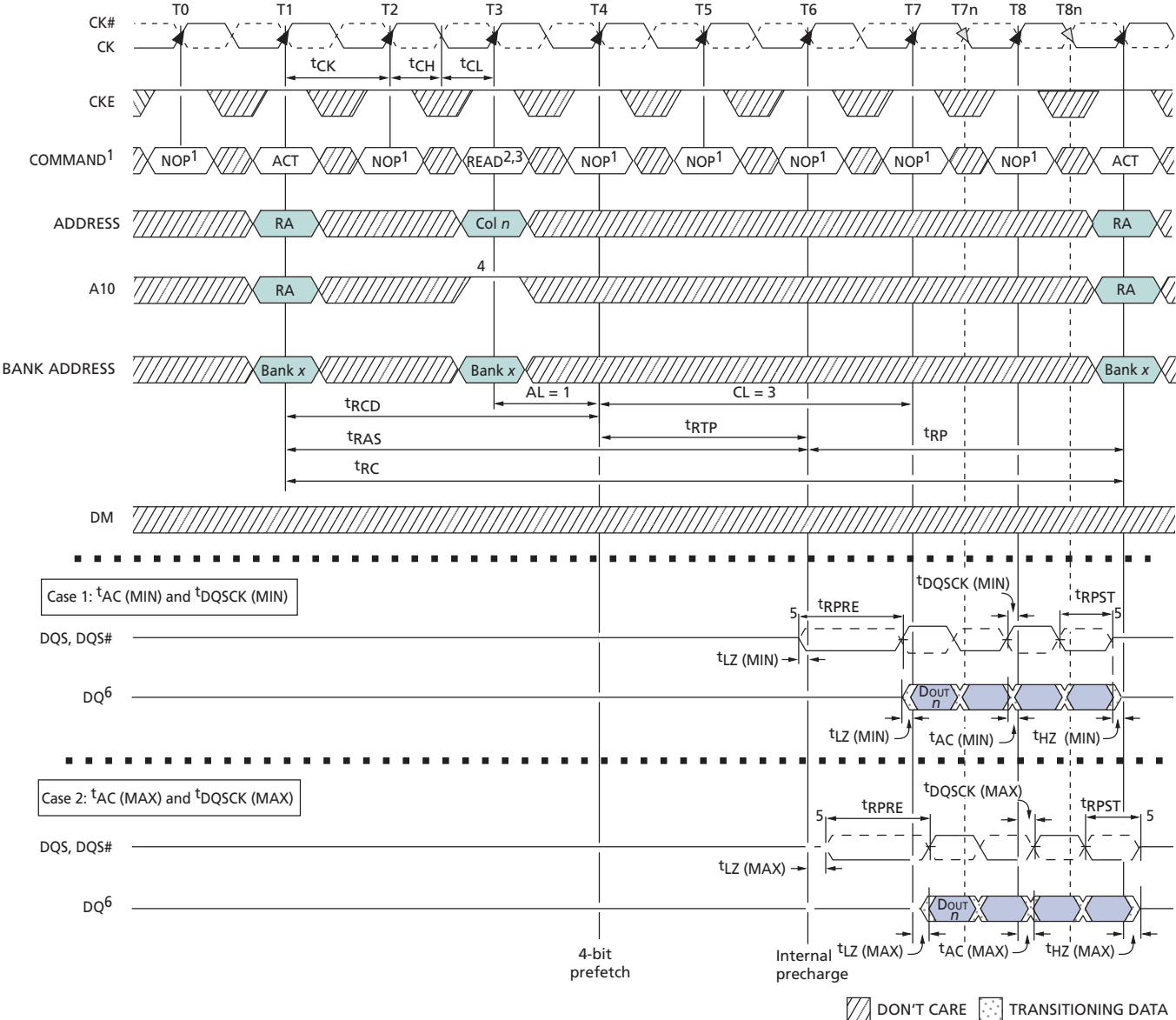


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4 and AL = 0 in the case shown.
  3. The PRECHARGE command can only be applied at T6 if  $t_{RAS} (MIN)$  is met.
  4. READ-to-PRECHARGE = AL + BL/2 + ( $t_{RTP}$  - 2 clocks).
  5. Disable auto precharge.
  6. "Don't Care" if A10 is HIGH at T5.
  7. The I/O balls, when entering or exiting HIGH-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
  8. DOUT  $n$  = data-out from column  $n$ ; subsequent elements are applied in the programmed order.



1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

Figure 26: Bank Read – with Auto Precharge

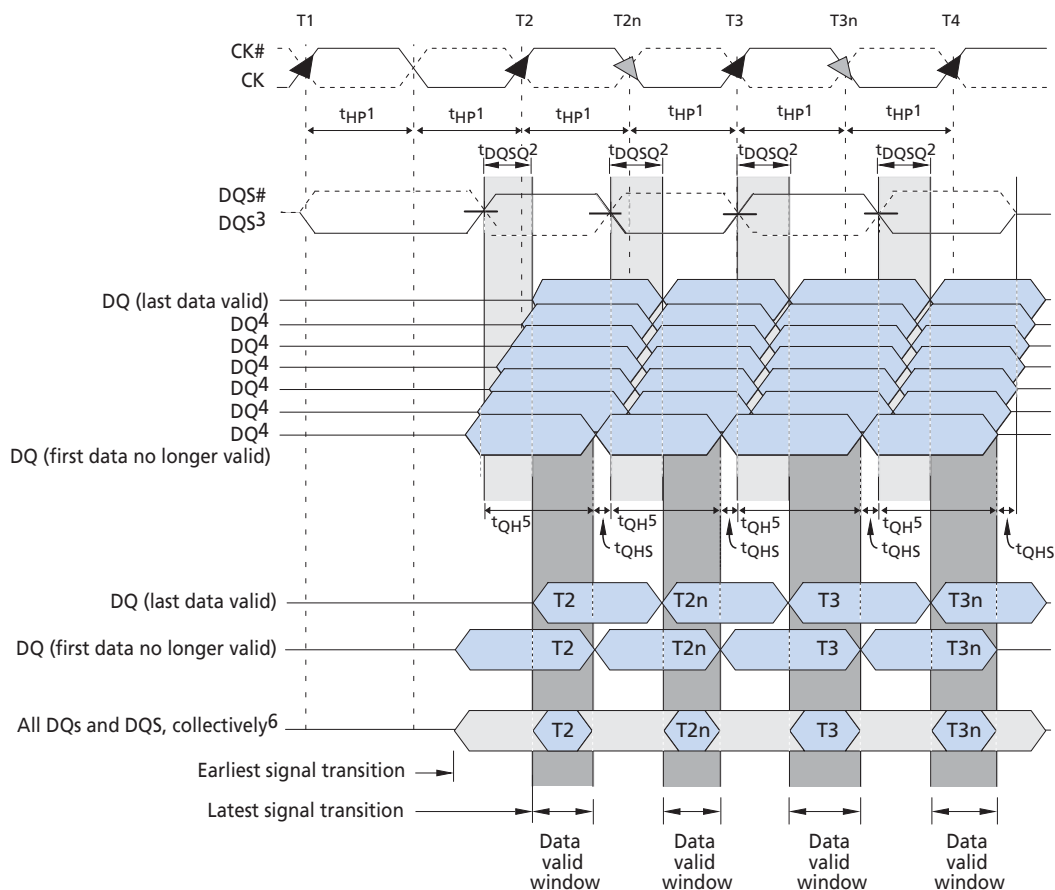


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4, RL = 4 (AL = 1, CL = 3) in the case shown.
  3. The 1.5V DDR2 SDRAM internally delays auto precharge until both  $t_{RAS}$  (MIN) and  $t_{RTP}$  (MIN) have been satisfied.
  4. Enable auto precharge.
  5. The I/O balls, when entering or exiting HIGH-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
  6. DOUT  $n$  = data-out from column  $n$ ; subsequent elements are applied in the programmed order.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

**Figure 27: x4, x8 Data Output Timing –  $t_{DQSQ}$ ,  $t_{QH}$ , and Data Valid Window**

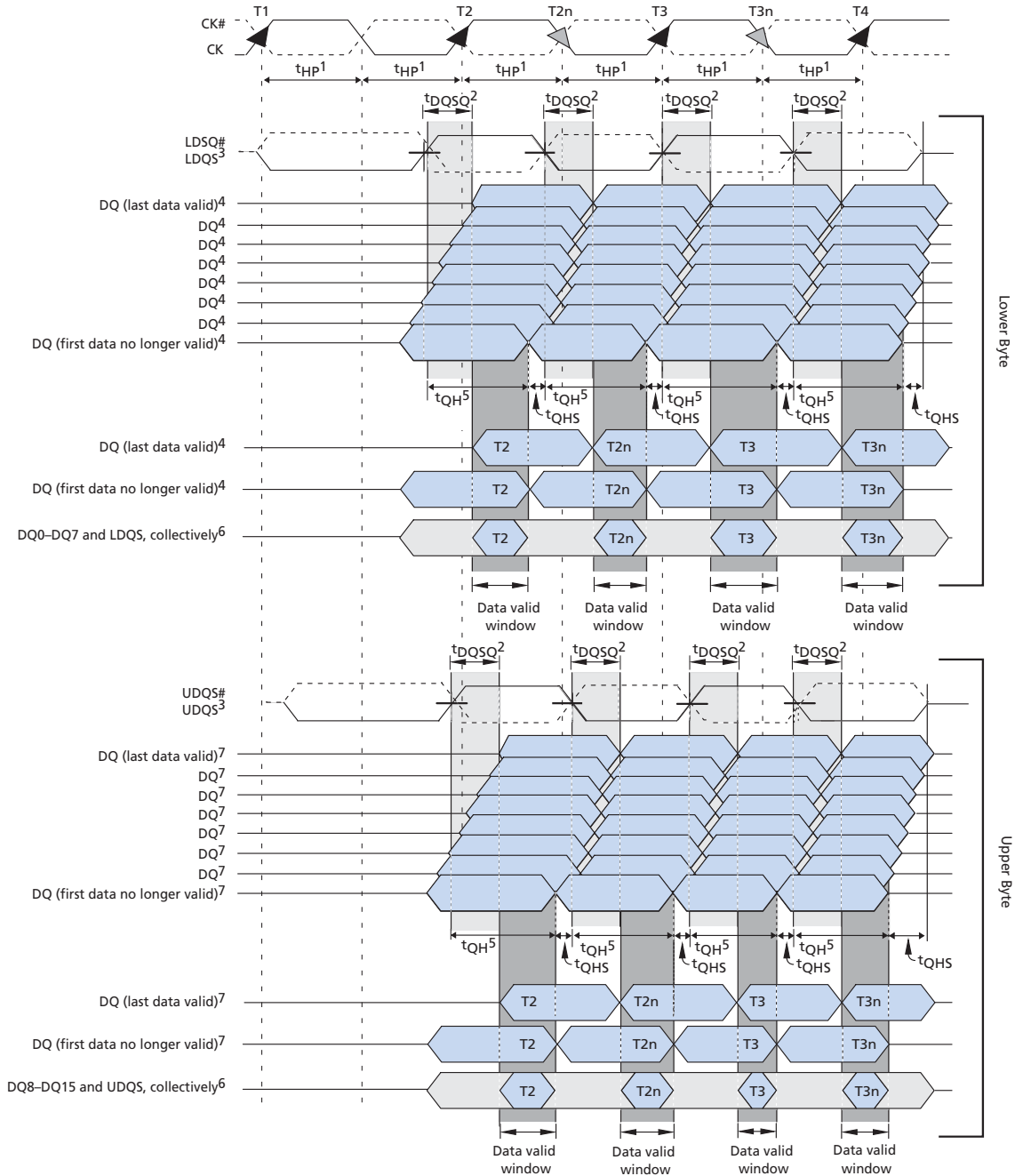


- Notes:
1.  $t_{HP}$  is the lesser of  $t_{CL}$  or  $t_{CH}$  clock transitions collectively when a bank is active.
  2.  $t_{DQSQ}$  is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
  3. DQ transitioning after DQS transition define  $t_{DQSQ}$  window. DQS transitions at T2 and at T2n are "early DQS," at T3 are "nominal DQS," and at T3n are "late DQS."
  4. DQ0, DQ1, DQ2, DQ3 for x4 or DQ0–DQ7 for x8.
  5.  $t_{QH}$  is derived from  $t_{HP}$ :  $t_{QH} = t_{HP} - t_{QHS}$ .
  6. The data valid window is derived for each DQS transition and is defined as  $t_{QH} - t_{DQSQ}$ .



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM READ Command

**Figure 28: x16 Data Output Timing –  $t_{DQSQ}$ ,  $t_{QH}$ , and Data Valid Window**

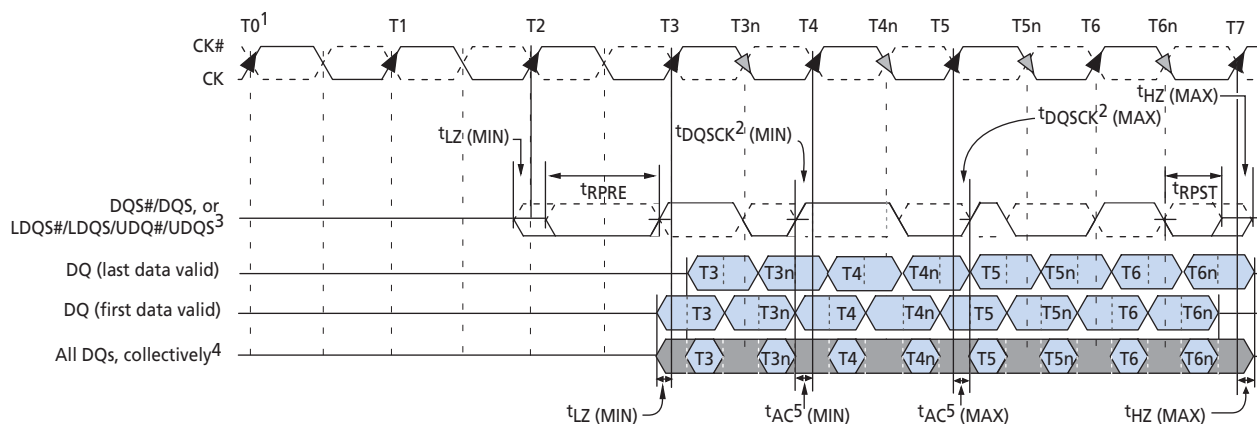


- Notes:
- $t_{HP}$  is the lesser of  $t_{CL}$  or  $t_{CH}$  clock transitions collectively when a bank is active.
  - $t_{DQSQ}$  is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
  - DQ transitioning after DQS transitions define the  $t_{DQSQ}$  window. LDQS defines the lower byte, and UDQS defines the upper byte.
  - DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
  - $t_{QH}$  is derived from  $t_{HP}$ :  $t_{QH} = t_{HP} - t_{QHS}$ .
  - The data valid window is derived for each DQS transition and is  $t_{QH} - t_{DQSQ}$ .
  - DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.





Figure 29: Data Output Timing –  $t_{AC}$  and  $t_{DQSK}$



- Notes:
1. READ command with CL = 3, AL = 0 issued at T0.
  2.  $t_{DQSK}^2$  is the DQS output window relative to CK and is the long-term component of DQS skew.
  3. DQ transitioning after DQS transitions define  $t_{DQSQ}$  window.
  4. All DQ must transition by  $t_{DQSQ}$  after DQS transitions, regardless of  $t_{AC}$ .
  5.  $t_{AC}$  is the DQ output window relative to CK and is the "long term" component of DQ skew.
  6.  $t_{LZ} (MIN)$  and  $t_{AC} (MIN)$  are the first valid signal transitions.
  7.  $t_{HZ} (MAX)$  and  $t_{AC} (MAX)$  are the latest valid signal transitions.
  8. The I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.



## WRITE Command

The WRITE command is used to initiate a burst write access to an active row. The value on the bank select inputs selects the bank, and the address provided on inputs A0–A<sub>i</sub> (where A<sub>i</sub> is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

1.5V DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to <sup>t</sup>RCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location (Figure 39 on page 59).

## WRITE Operation

WRITE bursts are initiated with a WRITE command. 1.5V DDR2 SDRAM uses WL equal to RL minus one clock cycle [ $WL = RL - 1CK = AL + (CL - 1CK)$ ]. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

**Note:** For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The low state on DQS between the WRITE command and the first rising edge is known as the write preamble; the low state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is  $WL \pm {}^tDQSS$ . Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as  $\pm {}^tDQSS$ . <sup>t</sup>DQSS is specified with a relatively wide range (25 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (<sup>t</sup>DQSS [MIN] and <sup>t</sup>DQSS [MAX]) might not be intuitive, they have also been included. Figure 30 on page 52 shows the nominal case and the extremes of <sup>t</sup>DQSS for BL = 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued  $x$  cycles after the first WRITE command, where  $x$  equals BL/2.

Figure 31 on page 53 shows concatenated bursts of BL = 4. An example of nonconsecutive WRITES is shown in Figure 32 on page 53. Full-speed random write accesses within a page or pages can be performed as shown in Figure 33 on page 54. 1.5V DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 10 on page 51.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

This device does not permit interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be permitted to complete the entire WRITE burst cycle. However, a WRITE BL = 8 operation (with auto precharge disabled) might be interrupted and truncated *only* by another WRITE burst as long as the interruption occurs on a 4-bit boundary, due to the 4n prefetch architecture of 1.5V DDR2 SDRAM. WRITE burst BL = 8 operations may *not* be interrupted or truncated with any command except another WRITE command, as shown in Figure 34 on page 54.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE,  $t_{WTR}$  should be met, as shown in Figure 35 on page 55. The number of clock cycles required to meet  $t_{WTR}$  is either 2 or  $t_{WTR}/t_{CK}$ , whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command.  $t_{WR}$  must be met, as shown in Figure 36 on page 56.  $t_{WR}$  starts at the end of the data burst, regardless of the data mask condition.

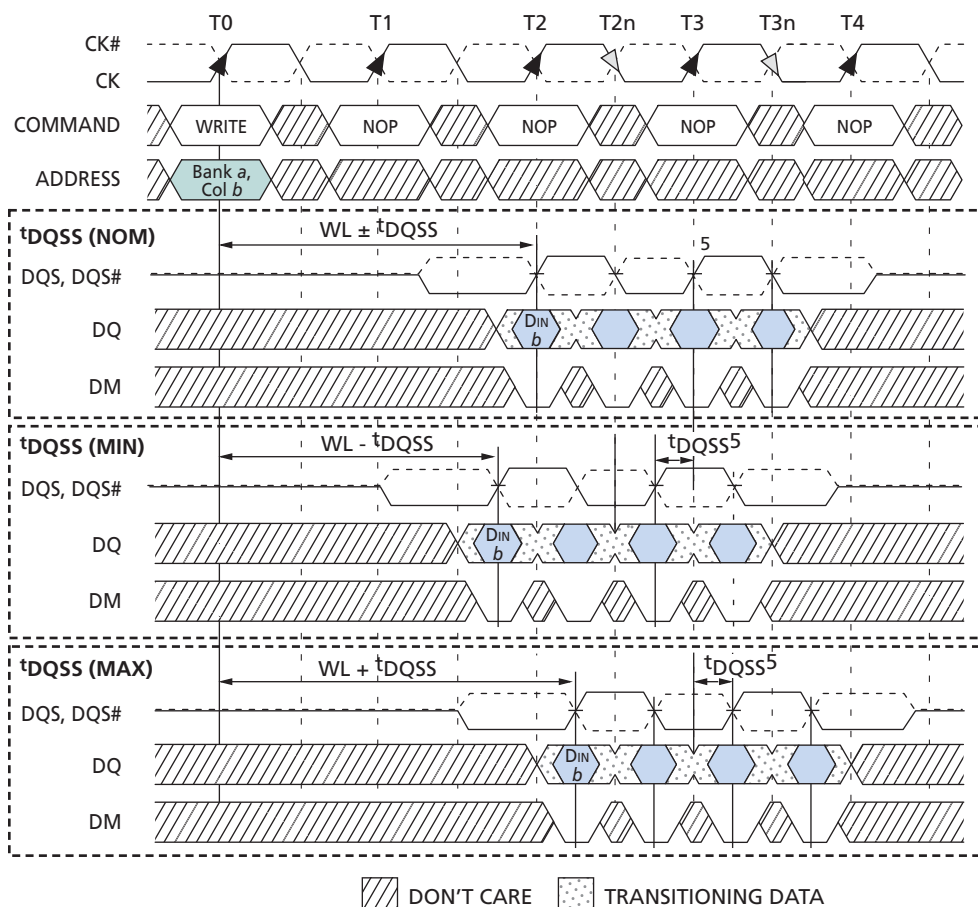
**Table 10: WRITE Using Concurrent Auto Precharge**

From Command (Bank <i>n</i> )	To Command (Bank <i>m</i> )	Minimum Delay (with Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ with auto precharge	$(CL - 1) + (BL/2) + t_{WTR}$	$t_{CK}$
	WRITE or WRITE with auto precharge	$(BL/2)$	$t_{CK}$
	PRECHARGE or ACTIVE	1	$t_{CK}$



**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
WRITE Command**

**Figure 30: WRITE Burst**

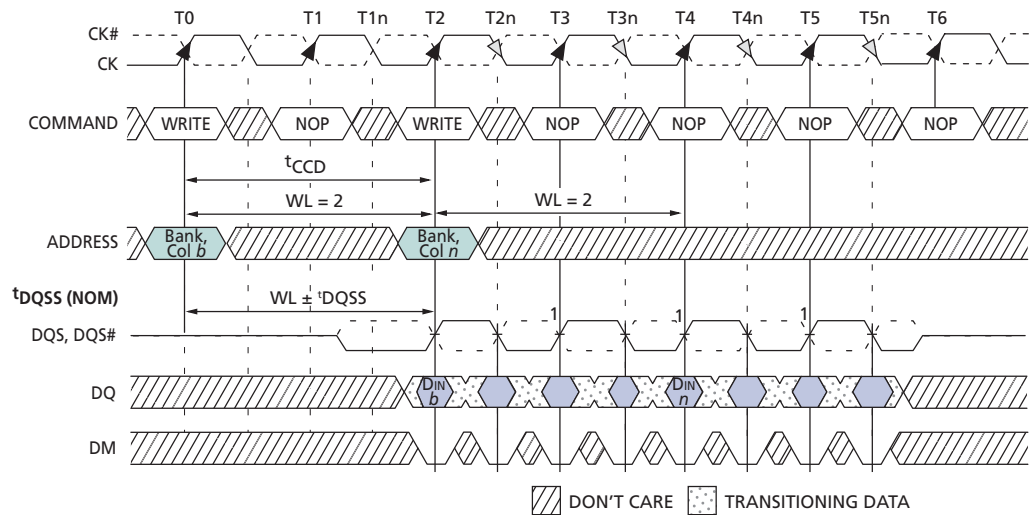


- Notes:
1. Subsequent rising DQS signals must align to the clock within  $t^{\text{DQSS}}$ .
  2.  $\text{DIN } b$  = data-in for column  $b$ .
  3. Three subsequent elements of data-in are applied in the programmed order following  $\text{DI } b$ .
  4. Shown with  $\text{BL} = 4$ ,  $\text{AL} = 0$ ,  $\text{CL} = 3$ ; thus,  $\text{WL} = 2$ .
  5.  $\text{A10}$  is LOW with the WRITE command (auto precharge is disabled).



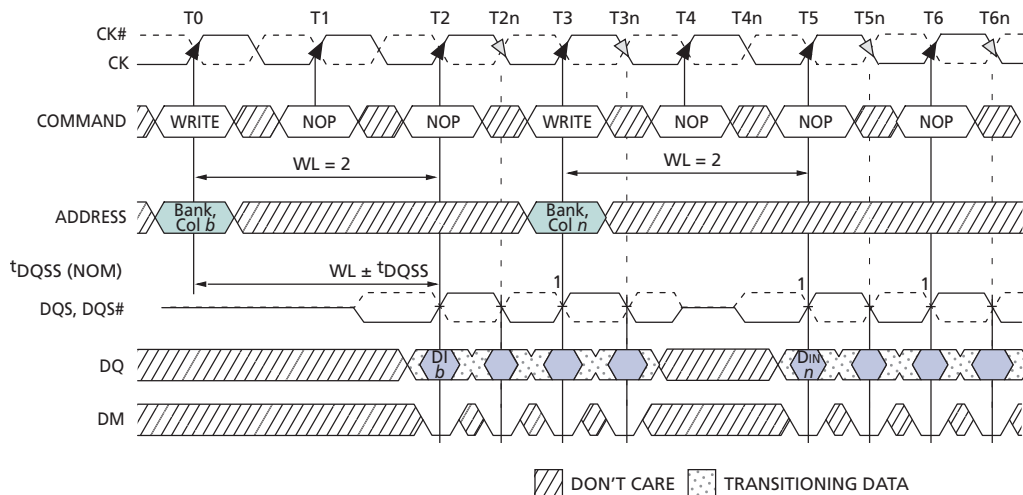
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

**Figure 31: Consecutive WRITE-to-WRITE**

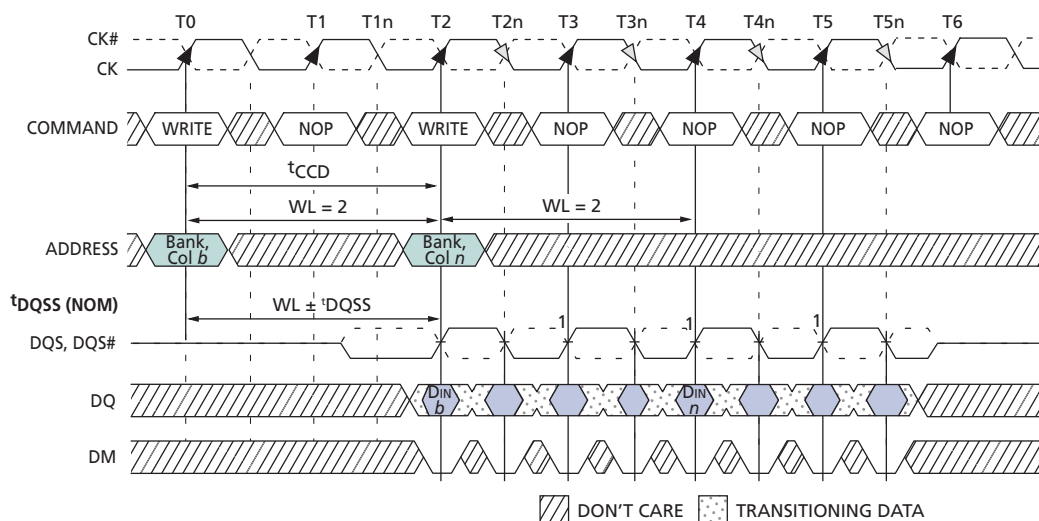


- Notes:
1. Subsequent rising DQS signals must align to the clock within  $t^{\text{DQS}}$ .
  2.  $\text{DIN } b$ , etc. = data-in for column  $b$ , etc.
  3. Three subsequent elements of data-in are applied in the programmed order following  $\text{DIN } b$ .
  4. Three subsequent elements of data-in are applied in the programmed order following  $\text{DIN } n$ .
  5. Shown with  $\text{BL} = 4$ ,  $\text{AL} = 0$ ,  $\text{CL} = 3$ ; thus,  $\text{WL} = 2$ .
  6. Each WRITE command may be to any bank.

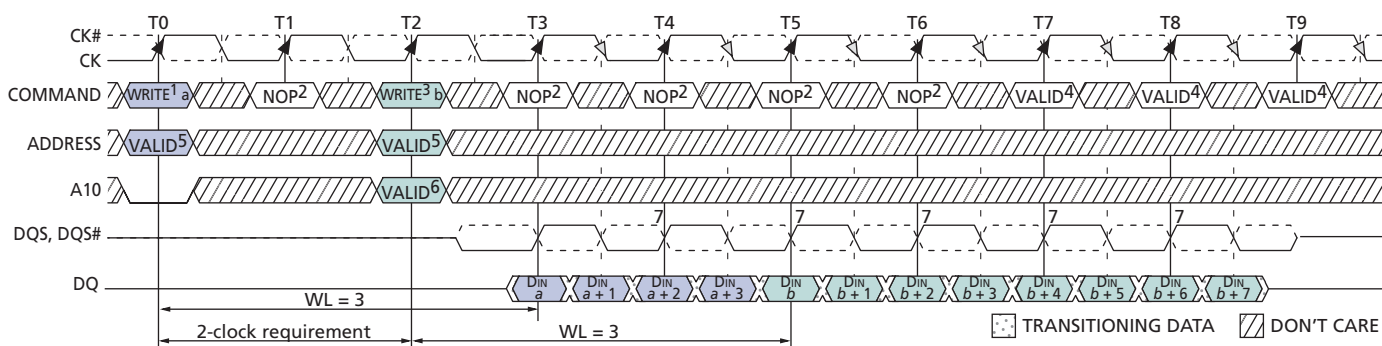
**Figure 32: Nonconsecutive WRITE-to-WRITE**



- Notes:
1. Subsequent rising DQS signals must align to the clock within  $t^{\text{DQS}}$ .
  2.  $\text{DIN } b$  (or  $n$ ), etc. = data-in for column  $b$  (or column  $n$ ).
  3. Three subsequent elements of data-in are applied in the programmed order following  $\text{DIN } b$ .
  4. Three subsequent elements of data-in are applied in the programmed order following  $\text{DIN } n$ .
  5. Shown with  $\text{BL} = 4$ ,  $\text{AL} = 0$ ,  $\text{CL} = 3$ ; thus,  $\text{WL} = 2$ .
  6. Each WRITE command may be to any bank.


**Figure 33: Random WRITE Cycles**


- Notes:
1. Subsequent rising DQS signals must align to the clock within  $t_{DQS}$ .
  2.  $D_{In} b$  (or  $n$ ), etc. = data-in for column  $b$  (or column  $n$ ).
  3. Three subsequent elements of data-in are applied in the programmed order following  $D_{In} b$ .
  4. Three subsequent elements of data-in are applied in the programmed order following  $D_{In} n$ .
  5. Shown with  $BL = 4$ ,  $AL = 0$ ,  $CL = 3$ ; thus,  $WL = 2$ .
  6. Each WRITE command may be to any bank.

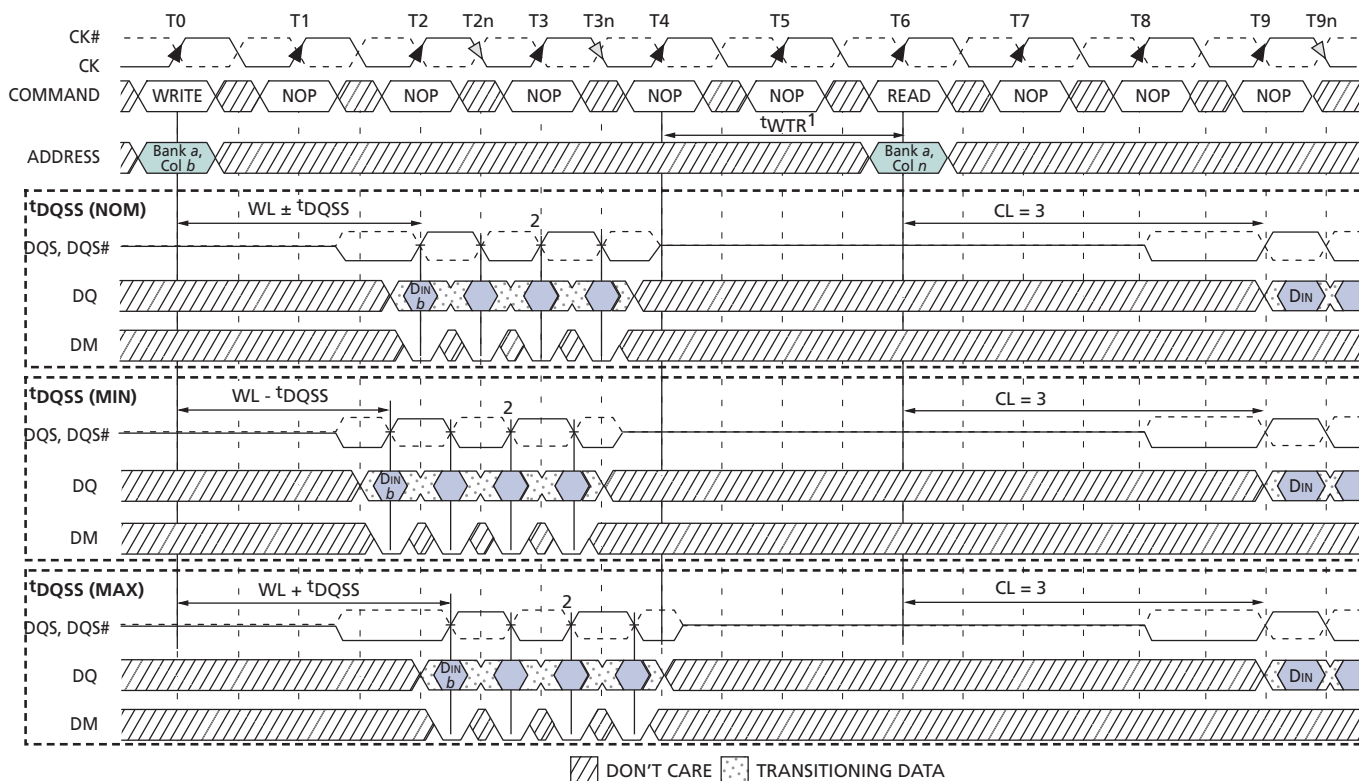
**Figure 34: WRITE Interrupted by WRITE**


- Notes:
1.  $BL = 8$  required and auto precharge must be disabled ( $A10 = LOW$ ).
  2. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for WRITES at  $T0$  and  $T2$ .
  3. Interrupting WRITE command must be issued exactly  $2 \times t_{CK}$  from previous WRITE.
  4. Earliest WRITE-to-PRECHARGE timing for WRITE at  $T0$  is  $WL + BL/2 + t_{WR}$  where  $t_{WR}$  starts with  $T7$  and not  $T5$  (since  $BL = 8$  from MR and not the truncated length).
  5. WRITE command can be issued to any valid bank and row address (WRITE command at  $T0$  and  $T2$  can be either same bank or different bank).
  6. Auto precharge can be either enabled ( $A10 = HIGH$ ) or disabled ( $A10 = LOW$ ) by the interrupting WRITE command.
  7. Subsequent rising DQS signals must align to the clock within  $t_{DQS}$ .
  8. Example shown uses  $AL = 0$ ;  $CL = 4$ ,  $BL = 8$ .



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

**Figure 35: WRITE-to-READ**

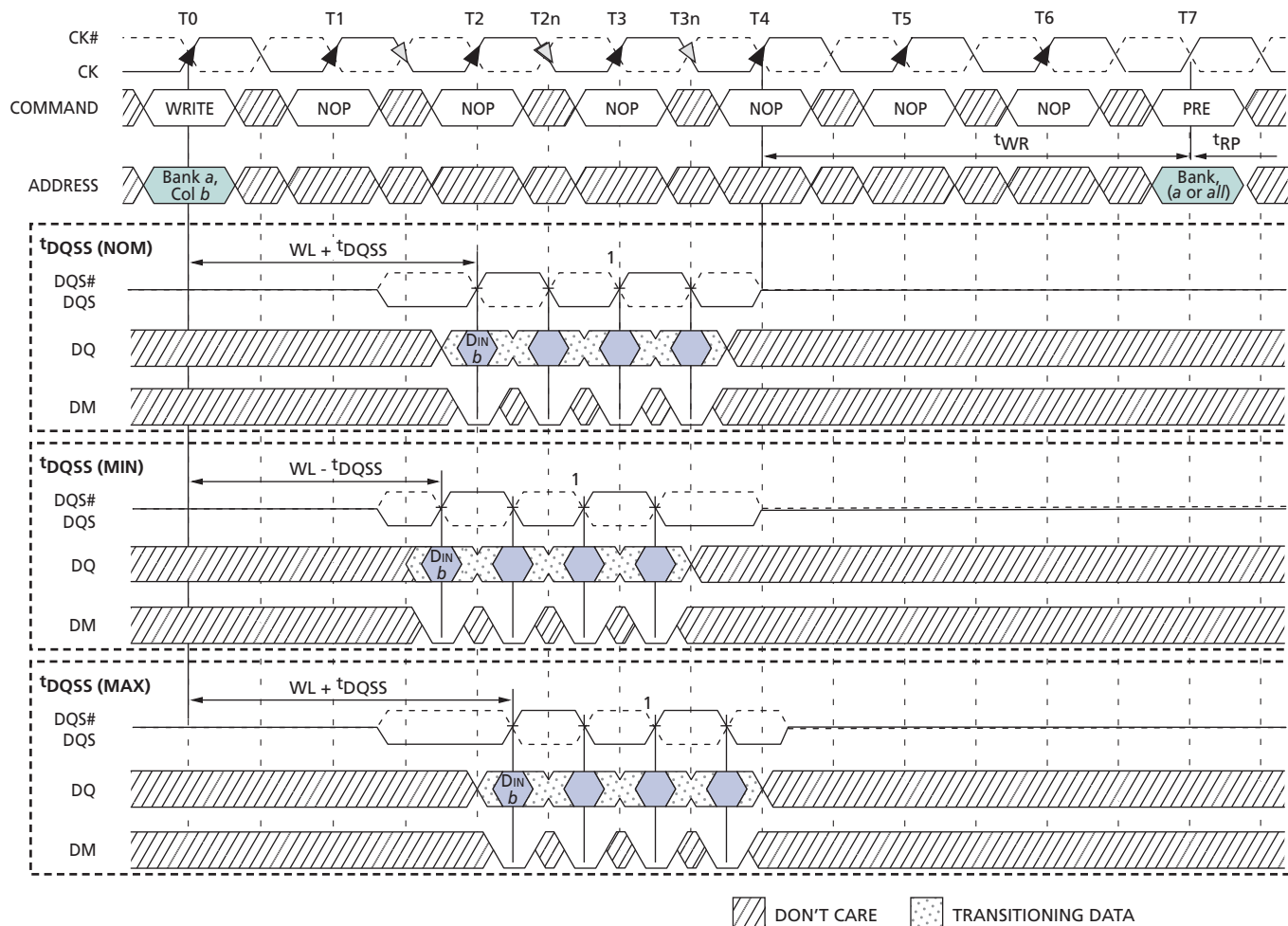


- Notes:
1.  $t_{WTR}$  is required for any READ following a WRITE to the same device, but it is not required between module ranks.
  2. Subsequent rising DQS signals must align to the clock within  $t_{DQSS}$ .
  3.  $D_{IN} b$  = data-in for column  $b$ ;  $D_{OUT} n$  = data-out from column  $n$ .
  4.  $BL = 4$ ,  $AL = 0$ ,  $CL = 3$ ; thus,  $WL = 2$ .
  5. One subsequent element of data-in is applied in the programmed order following  $D_{I} b$ .
  6.  $t_{WTR}$  is referenced from the first positive CK edge after the last data-in pair.
  7. A10 is LOW with the WRITE command (auto precharge is disabled).
  8. The number of clock cycles required to meet  $t_{WTR}$  is either 2 or  $t_{WTR}/t_{CK}$ , whichever is greater.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

**Figure 36: WRITE-to-PRECHARGE**

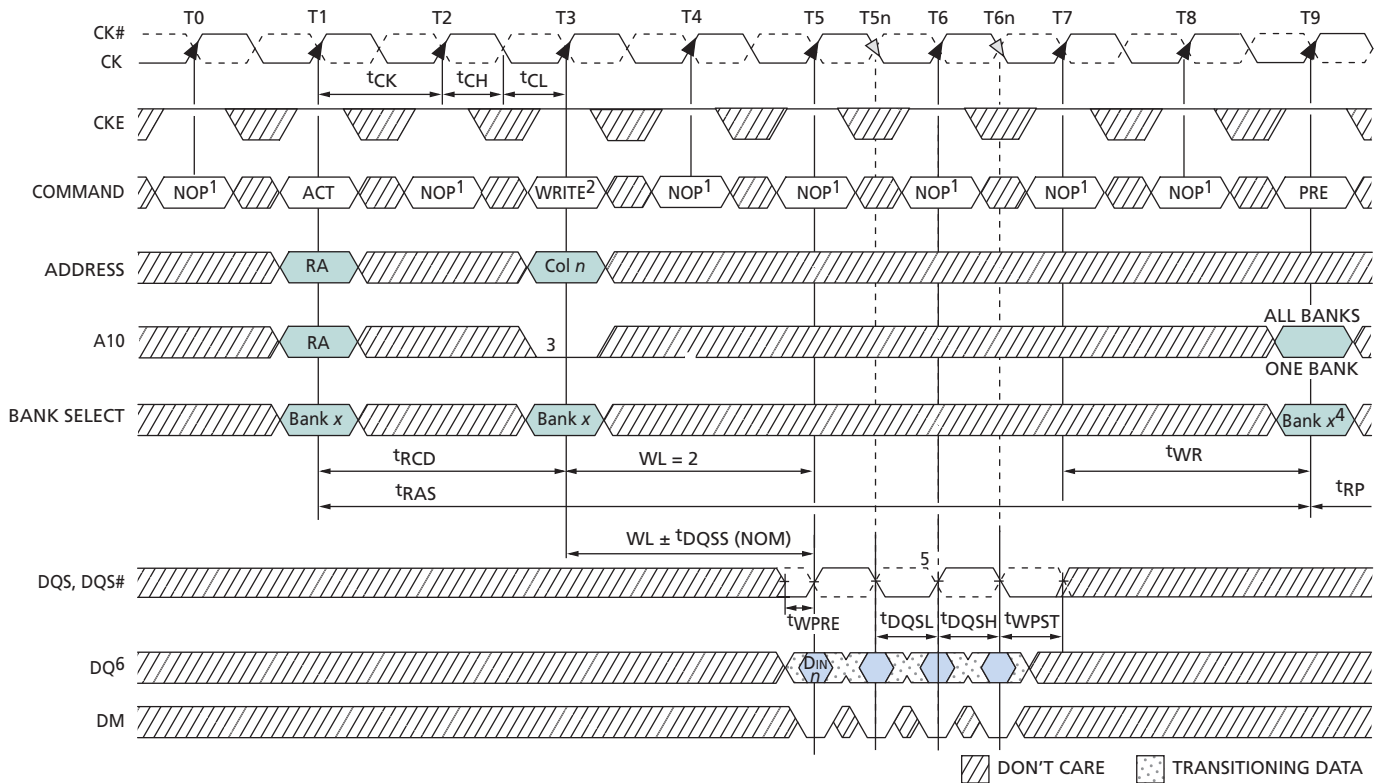


- Notes:
1. Subsequent rising DQS signals must align to the clock within  $t_{DQSS}$ .
  2.  $DIN\ b$  = data-in for column  $b$ .
  3. Three subsequent elements of data-in are applied in the programmed order following  $DI\ b$ .
  4.  $BL = 4$ ,  $CL = 3$ ,  $AL = 0$ ; thus,  $WL = 2$ .
  5.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  6. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks, in which case  $t_{WR}$  is not required and the PRECHARGE command could be applied earlier.
  7. A10 is LOW with the WRITE command (auto precharge is disabled).





Figure 37: Bank Write – Without Auto Precharge

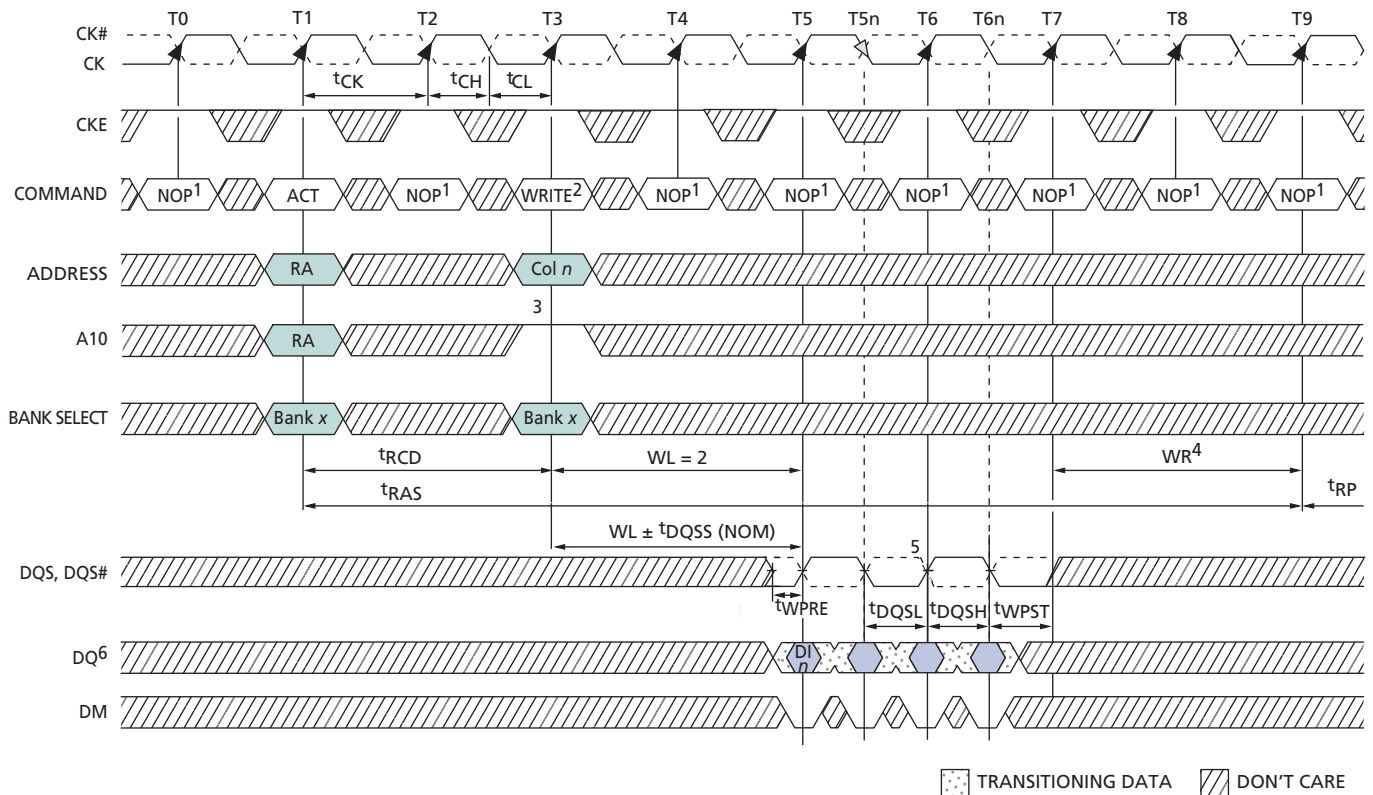


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4 and AL = 0 in the case shown.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T9.
  5. Subsequent rising DQS signals must align to the clock within  $t^{\text{DQSS}}$ .
  6. DIN  $n$  = data-in from column  $n$ ; subsequent elements are applied in the programmed order.
  7.  $t^{\text{DSH}}$  is applicable during  $t^{\text{DQSS}}$  (MIN) and is referenced from CK T5 or T6.
  8.  $t^{\text{DSS}}$  is applicable during  $t^{\text{DQSS}}$  (MAX) and is referenced from CK T6 or T7.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

**Figure 38: Bank Write – with Auto Precharge**

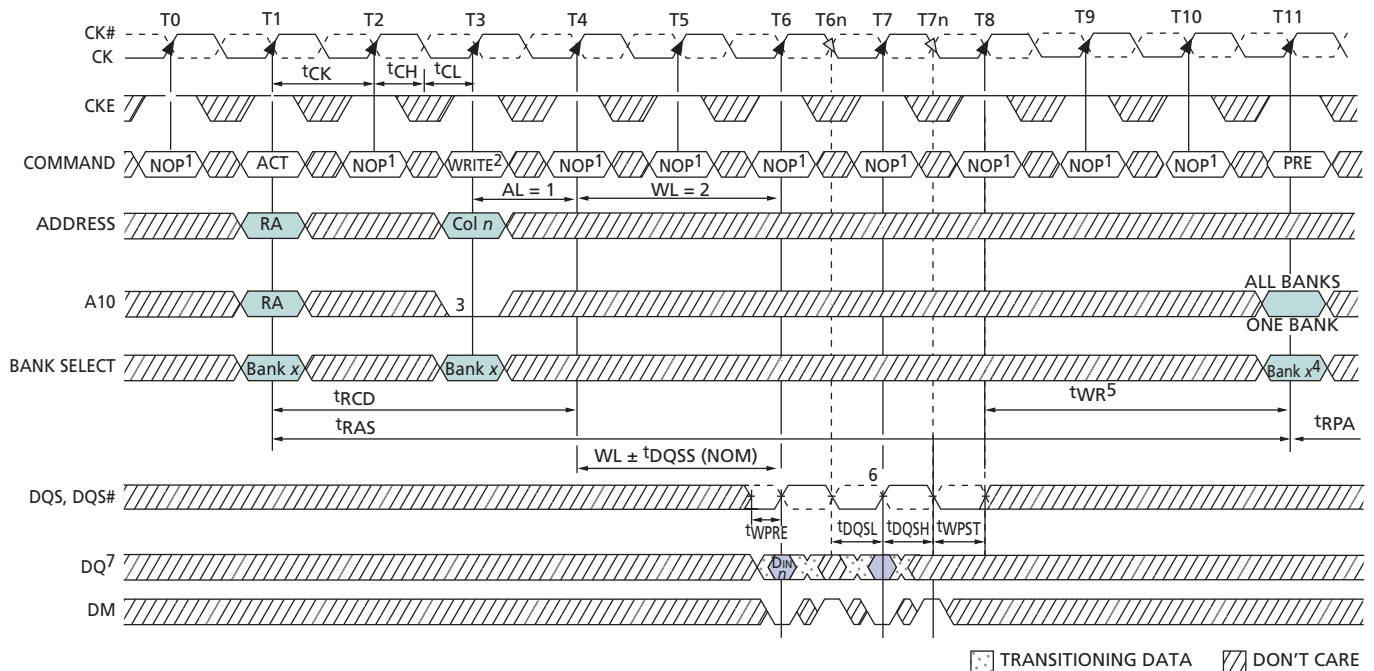


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4 and AL = 0 in the case shown.
  3. Enable auto precharge.
  4. WR is programmed via MR9–MR11 and is calculated by dividing  $t^{\text{WR}}$  (in ns) by  $t^{\text{CK}}$  and rounding up to the next integer value.
  5. Subsequent rising DQS signals must align to the clock within  $t^{\text{DQSS}}$ .
  6.  $\text{DIN } n$  = data-in from column  $n$ ; subsequent elements are applied in the programmed order.
  7.  $t^{\text{DSH}}$  is applicable during  $t^{\text{DQSS}}$  (MIN) and is referenced from CK T5 or T6.
  8.  $t^{\text{DSS}}$  is applicable during  $t^{\text{DQSS}}$  (MAX) and is referenced from CK T6 or T7.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

**Figure 39: WRITE – DM Operation**

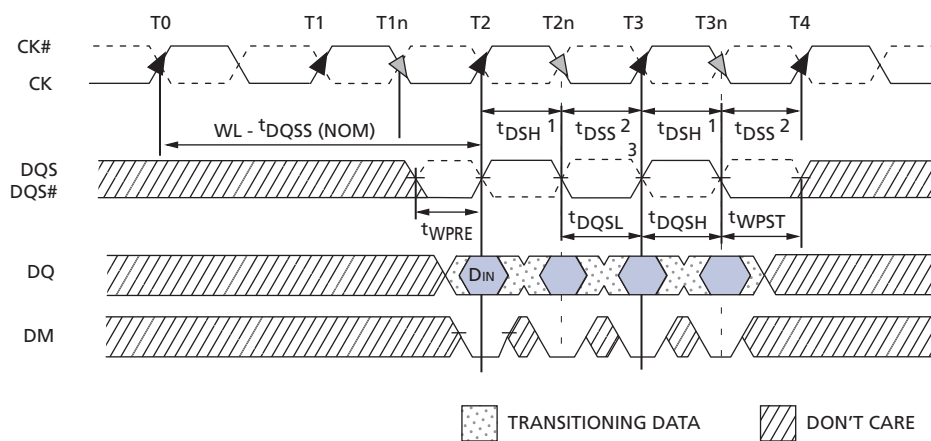


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4, AL = 1, and WL = 2 in the case shown.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T11.
  5.  $t_{WR}$  starts at the end of the data burst regardless of the data mask condition.
  6. Subsequent rising DQS signals must align to the clock within  $t_{DQSS}$ .
  7. DI n = data-in from column n; subsequent elements are applied in the programmed order.
  8.  $t_{DSH}$  is applicable during  $t_{DQSS} (MIN)$  and is referenced from CK T6 or T7.
  9.  $t_{DSS}$  is applicable during  $t_{DQSS} (MAX)$  and is referenced from CK T7 or T8.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM WRITE Command

**Figure 40: Data Input Timing**



- Notes:
1.  $t_{DSH}^{(MIN)}$  generally occurs during  $t_{DQSS}^{(MIN)}$ .
  2.  $t_{DSS}^{(MIN)}$  generally occurs during  $t_{DQSS}^{(MAX)}$ .
  3. Subsequent rising DQS signals must align to the clock within  $t_{DQSS}$ .
  4. WRITE command issued at T0.
  5. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
  6. WRITE command with  $WL = 2$  ( $CL = 3$ ,  $AL = 0$ ) issued at T0.



## PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time ( $t_{RP}$ ) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

## PRECHARGE Operation

Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, bank address inputs determine the bank. Otherwise the bank address inputs are treated as “Don’t Care.”

When all banks are to be precharged, the bank address inputs are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. When a single-bank PRECHARGE command is issued,  $t_{RP}$  timing applies. When the PRECHARGE (ALL) command is issued,  $t_{RPA}$  timing applies regardless of the number of banks opened.

## SELF REFRESH Command

The SELF REFRESH command can be used to retain data in the 1.5V DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the 1.5V DDR2 SDRAM retains data without external clocking. All power supply inputs (including  $V_{REF}$ ) must be maintained at valid levels upon entry/exit *and* during SELF REFRESH operation.

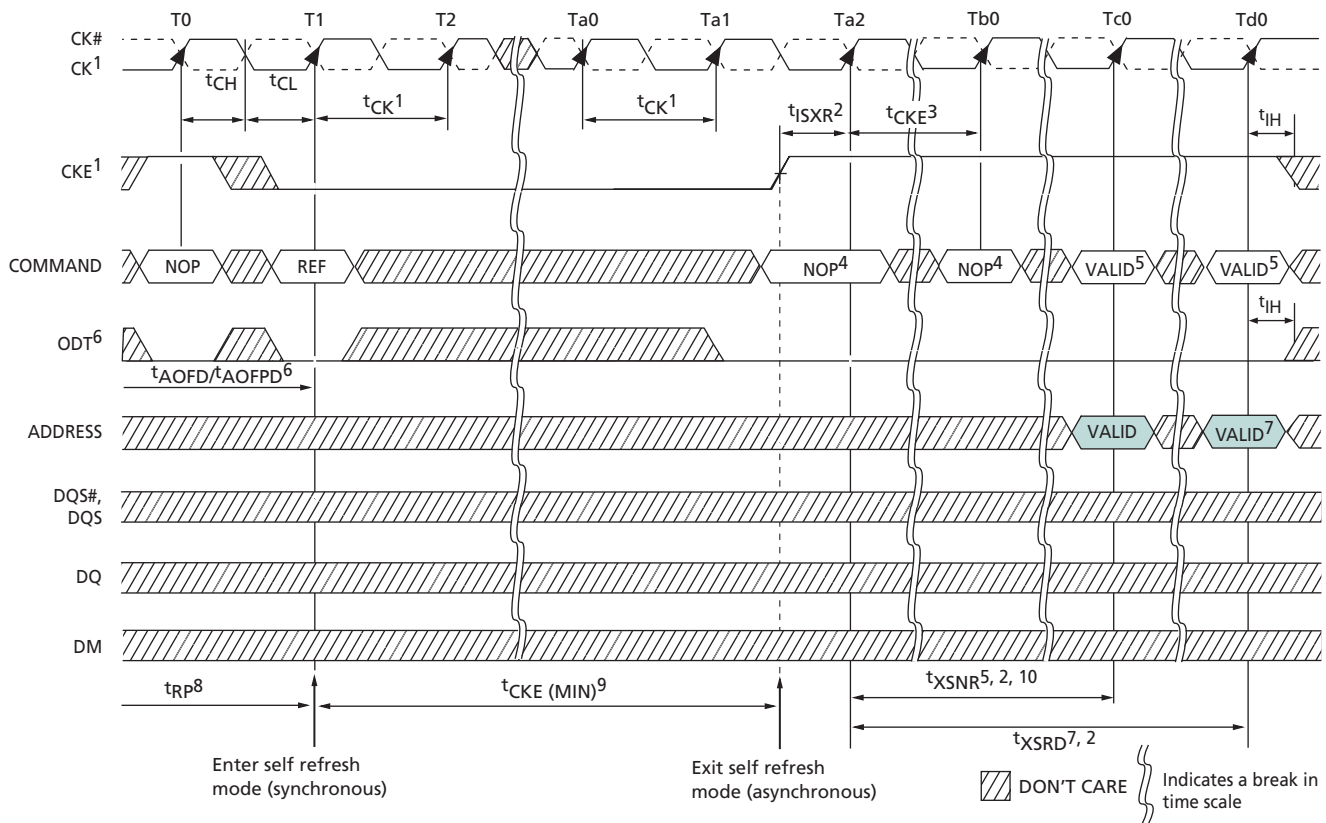
The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh (200 clock cycles must then occur before a READ command can be issued). The differential clock should remain stable and meet  $t_{CKE}$  specifications at least  $1 \times t_{CK}$  after entering self refresh mode. All command and address input signals except CKE are “Don’t Care” during self refresh.

The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet  $t_{CK}$  specifications at least  $1 \times t_{CK}$  prior to CKE going back HIGH. Once CKE is HIGH ( $t_{CKE}$  [MIN] has been satisfied with four clock registrations), the 1.5V DDR2 SDRAM must have NOP or DESELECT commands issued for  $t_{XSNR}$  because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM SELF REFRESH Command

**Figure 41: Self Refresh**



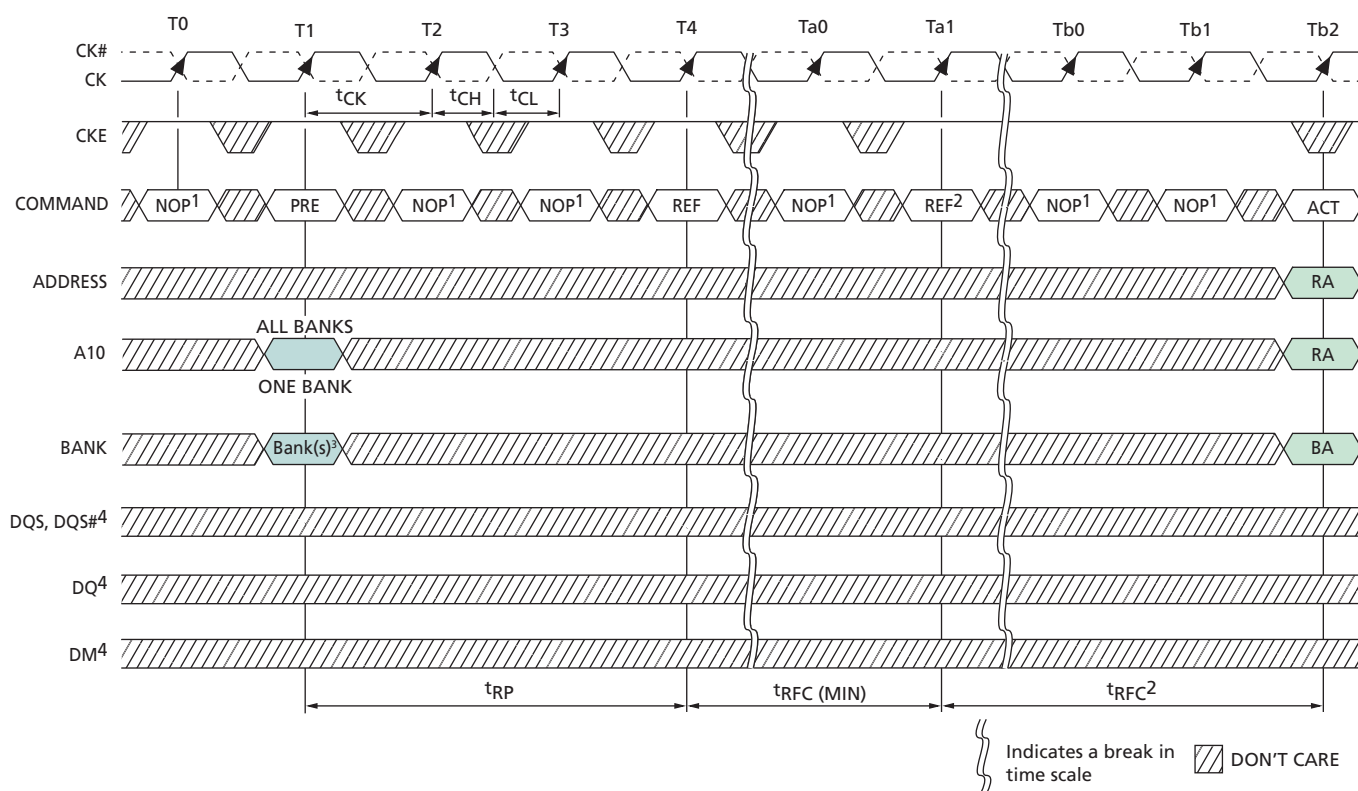
- Notes:
1. Clock must be stable and meeting  $t_{CK}$  specifications at least  $1 \times t_{CK}$  after entering self refresh mode and at least  $1 \times t_{CK}$  prior to exiting self refresh mode.
  2. Self refresh exit is asynchronous; however,  $t_{XSNR}$  and  $t_{XSRD}$  timing starts at the first rising clock edge where CKE HIGH satisfies  $t_{ISXR}$ .
  3. CKE must stay HIGH until  $t_{XSRD}$  is met; however, if self refresh is being reentered, CKE may go back LOW after  $t_{XSNR}$  is satisfied.
  4. NOP or DESELECT commands are required prior to exiting self refresh until state Tc0, which allows any nonREAD command.
  5.  $t_{XSNR}$  is required before any nonREAD command can be applied.
  6. ODT must be disabled and RTT off ( $t_{AOFD}$  and  $t_{AOFDP}$  have been satisfied) prior to entering SELF REFRESH at state T1.
  7.  $t_{XSRD}$  (200 cycles of CK) is required before a READ command can be applied at state Td0.
  8. Device must be in the all banks idle state prior to entering self refresh mode.
  9. Once self refresh has been entered,  $t_{CKE(MIN)}$  must be satisfied prior to exiting self refresh.
  10. Once exiting SELF REFRESH, ODT must remain LOW until  $t_{XSRD}$  is satisfied.



## REFRESH Command

REFRESH is used during normal operation of the 1.5V DDR2 SDRAM and is analogous to CAS#-Before-RAS# (CBR) refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command. The commercial temperature 1.5V DDR2 SDRAM requires REFRESH cycles at an average interval of 7.8125 $\mu$ s (MAX) and all rows in all banks must be refreshed at least once every 64ms. The refresh period begins when the REFRESH command is registered and ends  $t_{RFC}$  (MIN) later.

**Figure 42: Refresh Mode**



- Notes:
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
  2. The second REFRESH is not required and is only shown as an example of two back-to-back REFRESH commands.
  3. “Don’t Care” if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
  4. DM, DQ, and DQS signals are all “Don’t Care”/High-Z for operations shown.



## Power-Down Mode

These devices support multiple power-down modes that enable significant power savings over normal operating modes. CKE is used to enter and exit different power-down modes. Power-down entry and exit timings are shown in Figure 43 on page 65. Detailed power-down entry conditions are shown in Figures 44–51. The CKE Truth Table, Table 11, is shown on page 66.

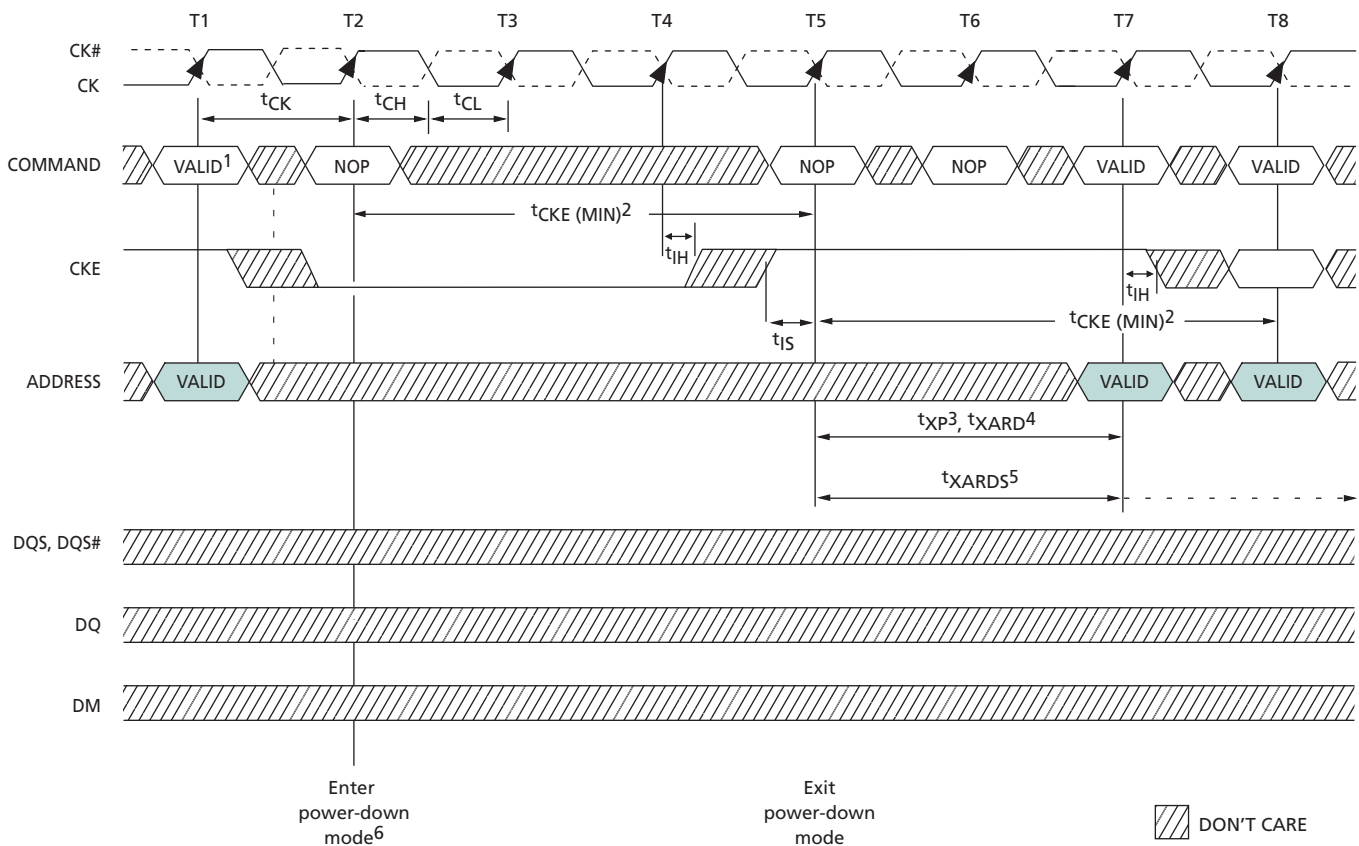
1.5V DDR2 SDRAMs require CKE to be registered HIGH (active) at all times that an access is in progress—from the issuing of a READ or WRITE command until completion of the burst. Thus, a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and  $t_{WR}$  or  $t_{WTR}$  are satisfied, as shown in Figures 46 and 47 on page 68. The number of clock cycles required to meet  $t_{WTR}$  is either two or  $t_{WTR}/t_{CK}$ , whichever is greater.

Power-down mode (see Figure 43 on page 65) is entered when CKE is registered LOW coincident with a NOP or DESELECT command. CKE is not allowed to go LOW during a mode register or EXTENDED MODE REGISTER command time, or while a READ or WRITE operation is in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, and CKE. For maximum power savings, the DLL is frozen during precharge power-down. Exiting active power-down requires the device to be at the same voltage and frequency as when it entered power-down. Exiting precharge power-down requires the device to be at the same voltage as when it entered power-down; however, the clock frequency is allowed to change. (See “Precharge Power-Down Clock Frequency Change” on page 71.)

The maximum duration for either active or precharge power-down is limited by the refresh requirements of the device  $t_{RFC}$  (MAX). The minimum duration for power-down entry and exit is limited by the  $t_{CKE}$  (MIN) parameter. While in power-down mode, CKE LOW, a stable clock signal, and stable power supply signals must be maintained at the inputs of the 1.5V DDR2 SDRAM, while all other input signals are “Don’t Care” except ODT. Detailed ODT timing diagrams for different power-down modes are shown in Figures 54–61.

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command), as shown in Figure 43 on page 65.




**Figure 43: Power-Down**


- Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
  2.  $t_{CKE} (MIN)$  of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + 2 \times t_{CK} + t_{IH}$ . CKE must not transition during its  $t_{IS}$  and  $t_{IH}$  window.
  3.  $t_{XP}$  timing is used for exit precharge power-down and active power-down to any nonREAD command.
  4.  $t_{XARD}$  timing is used for exit active power-down to READ command if fast exit is selected via MR (bit 12 = 0).
  5.  $t_{XARDS}$  timing is used for exit active power-down to READ command if slow exit is selected via MR (bit 12 = 1).
  6. No column accesses are permitted to be in progress at the time power-down is entered. If the DLL was not in a locked state when CKE went LOW, the DLL must be reset after exiting power-down mode for proper READ operation.


**Table 11: CKE Truth Table**

Notes 1–3 and 12 apply to the entire table

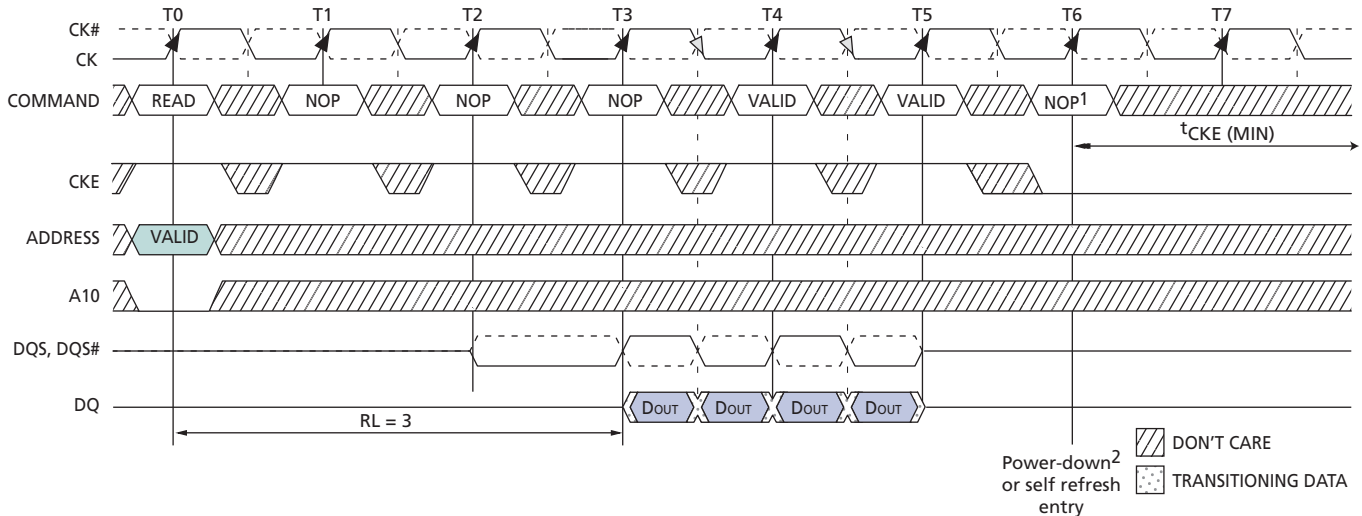
Current State	CKE		Command (n) CS#, RAS#, CAS#, WE#	Action (n)	Notes
	Previous Cycle (n - 1)	Current Cycle (n)			
Power-down	L	L	X	Maintain power-down	13, 14
	L	H	DESELECT or NOP	Power-down exit	4, 8
Self refresh	L	L	X	Maintain self refresh	14
	L	H	DESELECT or NOP	Self refresh exit	4, 5, 9
Bank(s) active	H	L	DESELECT or NOP	Active power-down entry	4, 8, 10, 11
All banks idle	H	L	DESELECT or NOP	Precharge power-down entry	4, 8, 10
	H	L	REFRESH	Self refresh entry	6, 9, 11
	H	H	Shown in Table 5 on page 32		7

- Notes:
1. CKE (n) is the logic state of CKE at clock edge n; CKE (n - 1) was the state of CKE at the previous clock edge.
  2. Current state is the state of the 1.5V DDR2 SDRAM immediately prior to clock edge n.
  3. Command (n) is the command registered at clock edge n, and action (n) is a result of command (n).
  4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
  5. On self refresh exit, DESELECT or NOP commands must be issued on every clock edge occurring during the  $t_{XSNR}$  period. READ commands may be issued only after  $t_{XSRD}$  (200 clocks) is satisfied.
  6. Self refresh mode can only be entered from the all banks idle state.
  7. Must be a legal command, as defined in Table 5 on page 32.
  8. Valid commands for power-down entry and exit are NOP and DESELECT only.
  9. Valid commands for self refresh exit are NOP and DESELECT only.
  10. Power-down and self refresh can not be entered while READ or WRITE operations, LOAD MODE operations, or PRECHARGE operations are in progress. See "Power-Down Mode" on page 64 and "SELF REFRESH Command" on page 61 for a list of detailed restrictions.
  11. Minimum CKE HIGH time is  $t_{CKE} = 3 \times t_{CK}$ . Minimum CKE LOW time is  $t_{CKE} = 3 \times t_{CK}$ . This requires a minimum of 3 clock cycles of registration.
  12. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See "ODT Timing" on page 74 for more details and specific restrictions.
  13. Power-down modes do not perform any REFRESH operations. The duration of power-down mode is therefore limited by the refresh requirements.
  14. "X" means "Don't Care" (including floating around VREF) in self refresh and power-down. However, ODT must be driven HIGH or LOW in power-down if the ODT function is enabled via EMR(1).



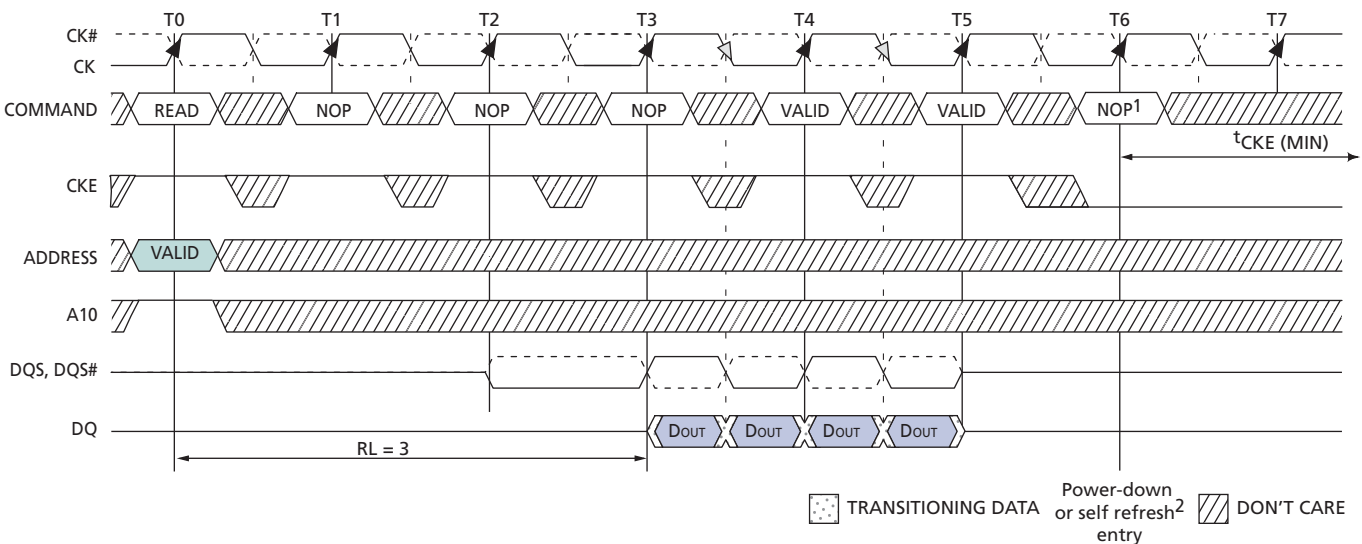
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Power-Down Mode

**Figure 44: READ to Power-Down or Self Refresh Entry**



- Notes: 1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.  
 2. Power-down or self refresh entry may occur after the READ burst completes.

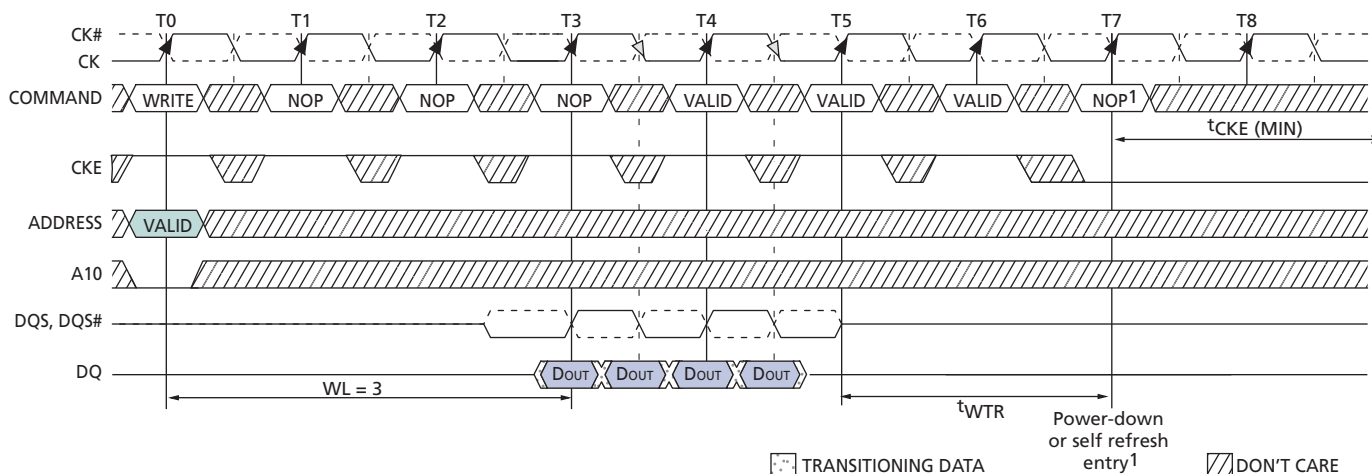
**Figure 45: READ with Auto Precharge to Power-Down or Self Refresh Entry**



- Notes: 1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.  
 2. Power-down or self refresh entry may occur after the READ burst completes.

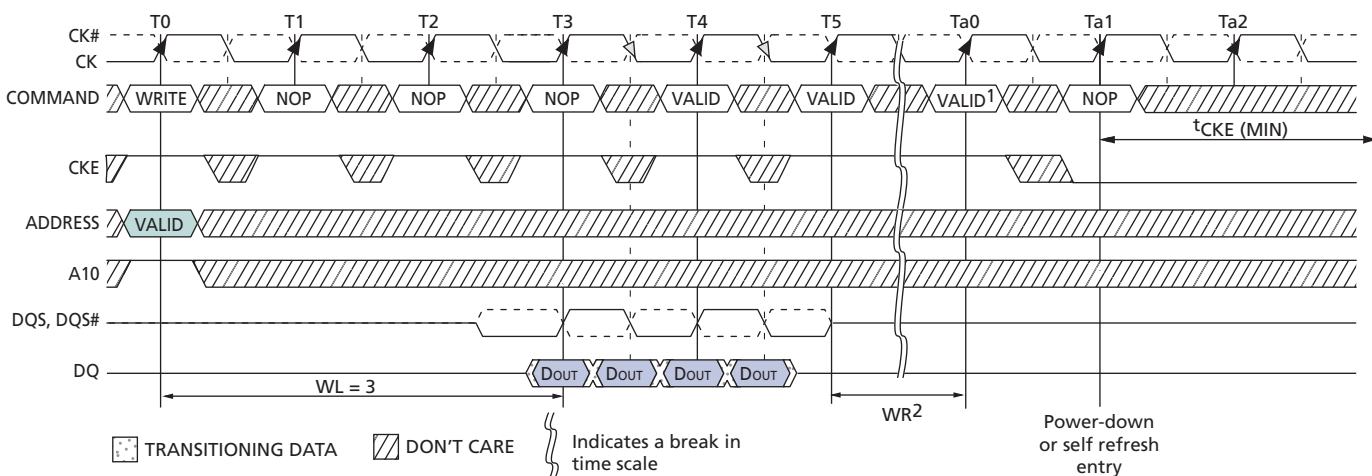


Figure 46: WRITE-to-Power-Down or Self-Refresh Entry



Notes: 1. Power-down or self refresh entry may occur after the WRITE burst completes.

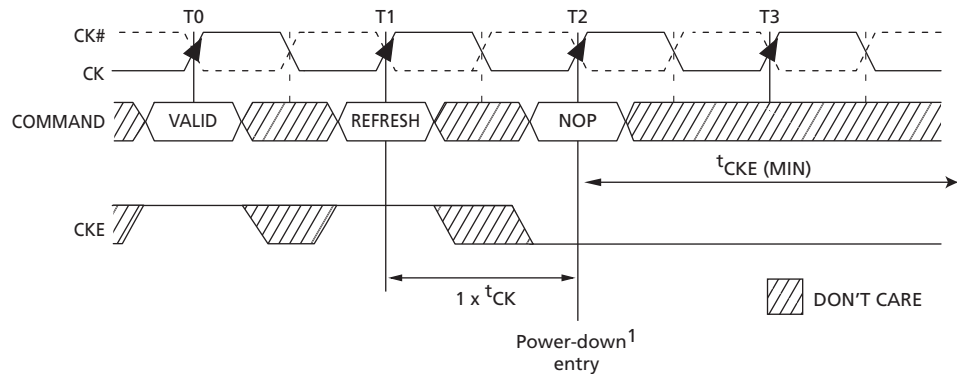
Figure 47: WRITE with Auto Precharge to Power-Down or Self Refresh Entry



Notes: 1. Internal PRECHARGE occurs at Ta0 when WR has completed; power-down entry may occur  $1 \times t_{CK}$  later at Ta1, prior to  $t_{RP}$  being satisfied.  
2. WR is programmed through MR9–MR11 and represents  $(t_{WR} [MIN] \text{ ns} / t_{CK})$  rounded up to next integer  $t_{CK}$ .

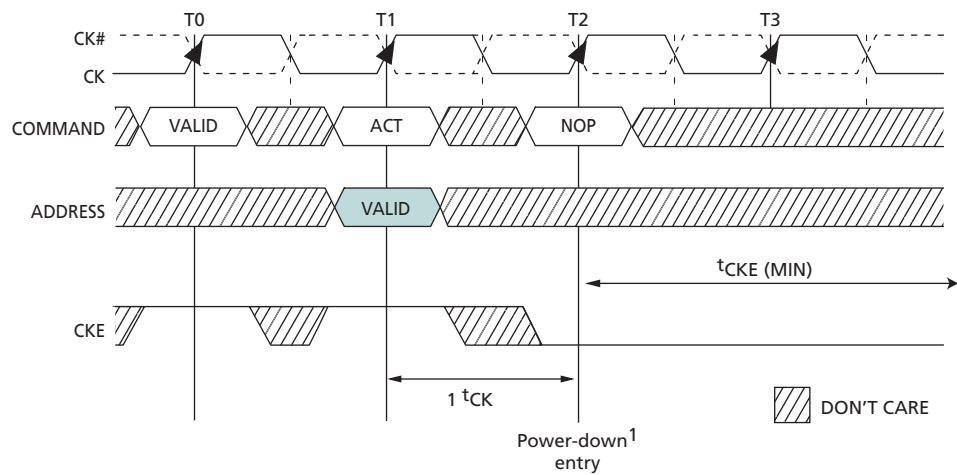


Figure 48: REFRESH Command to Power-Down Entry



Notes: 1. The earliest precharge power-down entry may occur is at T2, which is  $1 \times t_{CK}$  after the REFRESH command. Precharge power-down entry occurs prior to  $t_{RFC} (MIN)$  being satisfied.

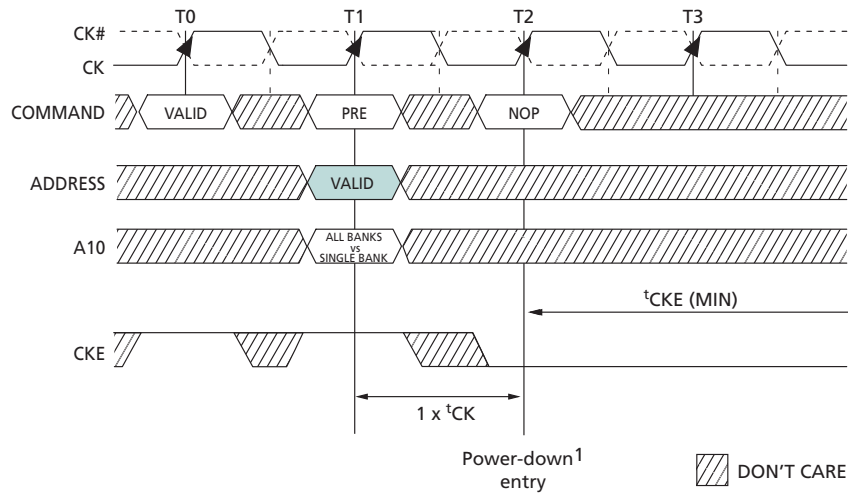
Figure 49: ACTIVE Command to Power-Down Entry



Notes: 1. The earliest active power-down entry may occur is at T2, which is  $1 \times t_{CK}$  after the ACTIVE command. Active power-down entry occurs prior to  $t_{RCD} (MIN)$  being satisfied.

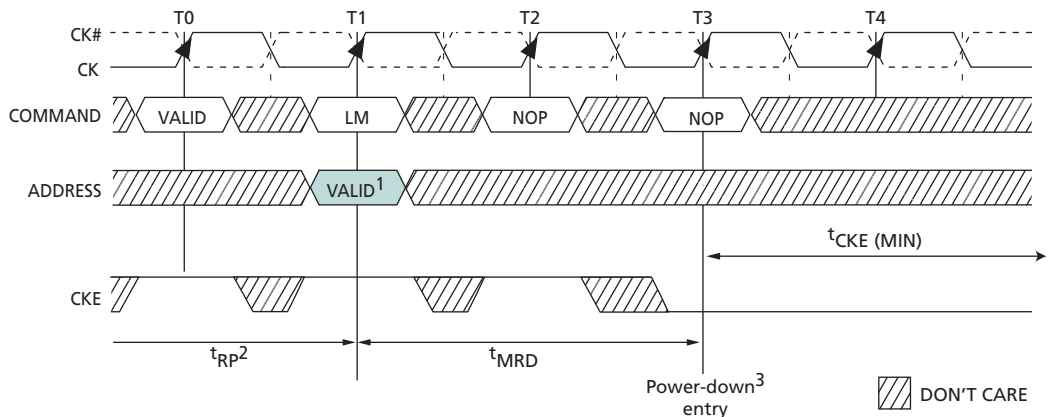


Figure 50: PRECHARGE Command to Power-Down Entry



Notes: 1. The earliest precharge power-down entry may occur is at T2, which is  $1 \times t_{CK}$  after the PRECHARGE command. Precharge power-down entry occurs prior to  $t_{RP}$  (MIN) being satisfied.

Figure 51: LOAD MODE Command to Power-Down Entry



Notes: 1. Valid address for LM command includes MR, EMR, EMR(2), and EMR(3) registers.  
2. All banks must be in the precharged state and  $t_{RP}$  met prior to issuing LM command.  
3. The earliest precharge power-down entry is at T3, which is after  $t_{MRD}$  is satisfied.

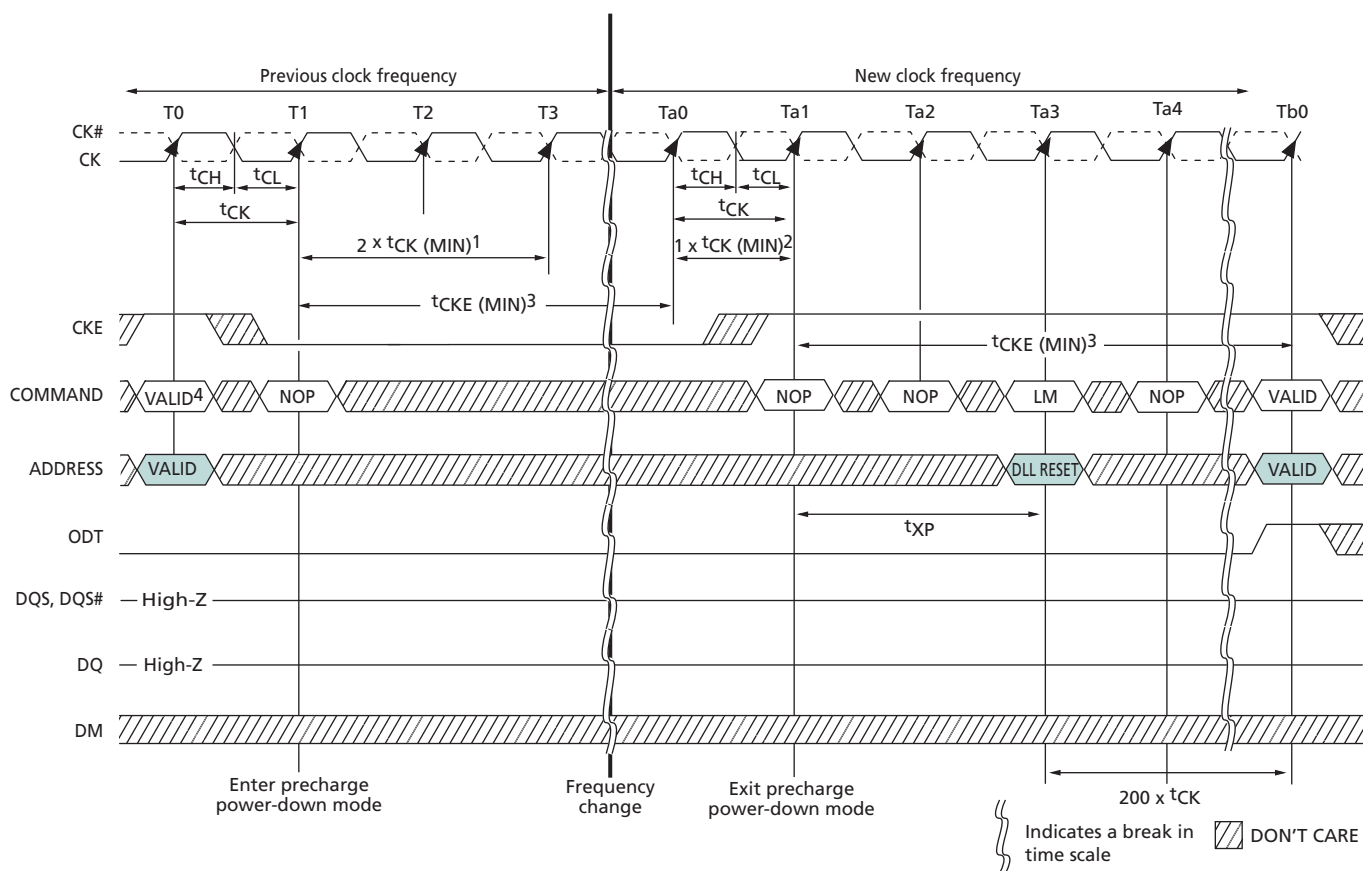


## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Precharge Power-Down Clock Frequency Change

### Precharge Power-Down Clock Frequency Change

When this device is in precharge power-down mode, ODT must be turned off and CKE must be at a logic LOW level. A minimum of two differential clock cycles must pass after CKE goes LOW before clock frequency may change. The device input clock frequency is permitted to change only within minimum and maximum operating frequencies specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, new stable clocks must be provided to the device before precharge power-down may be exited, and DLL must be reset via EMR after precharge power-down exit. Depending on the new clock frequency, an additional LM command might be required to appropriately set the WR MR9, MR10, MR11. During the DLL relock period of 200 cycles, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

**Figure 52: Input Clock Frequency Change During Precharge Power-Down Mode**



- Notes:
1. A minimum of  $2 \times t_{CK}$  is required after entering precharge power-down prior to changing clock frequencies.
  2. Once the new clock frequency has changed and is stable, a minimum of  $1 \times t_{CK}$  is required prior to exiting precharge power-down.
  3. Minimum CKE HIGH time is  $t_{CKE} = 3 \times t_{CK}$ . Minimum CKE LOW time is  $t_{CKE} = 3 \times t_{CK}$ . This requires a minimum of three clock cycles of registration.
  4. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down, which is required prior to the clock frequency change.



## RESET Function

### (CKE LOW Anytime)

1.5V DDR2 SDRAM applications may go into a reset state anytime during normal operation. If an application enters a reset condition, CKE is used to ensure the 1.5V DDR2 SDRAM device resumes normal operation after reinitializing. All data will be lost during a reset condition; however, the 1.5V DDR2 SDRAM device will continue to operate properly if the following conditions outlined in this section are satisfied.

The reset condition defined here assumes all supply voltages ( $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{DDL}$ , and  $V_{REF}$ ) are stable and meet all DC specifications prior to, during, and after the RESET operation. All other input pins of the 1.5V DDR2 SDRAM device are a “Don’t Care” during RESET with the exception of CKE.

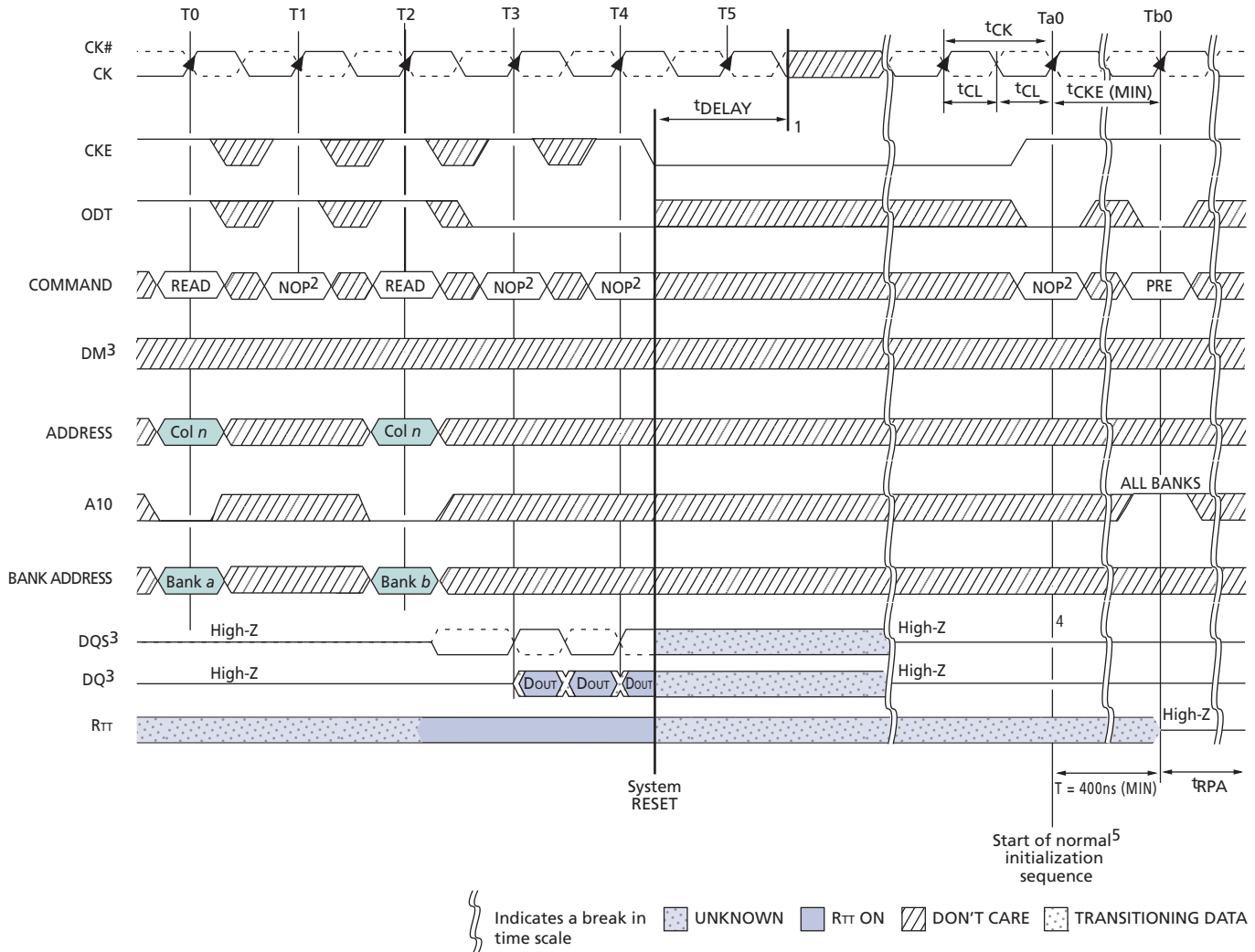
If CKE asynchronously drops LOW during any valid operation (including a READ or WRITE burst), the memory controller must satisfy the timing parameter  $t_{DELAY}$  before turning off the clocks. Stable clocks must exist at the CK, CK# inputs of the DRAM before CKE is raised HIGH, at which time the normal initialization sequence must occur. (See “Initialization” on page 19.) The 1.5V DDR2 SDRAM device is now ready for normal operation after the initialization sequence. Figure 53 on page 73 shows the proper sequence for a RESET operation.





# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM RESET Function

**Figure 53: RESET Function**



- Notes:
1. VDD, VDDL, VDDQ, VTT, and VREF must be valid at all times.
  2. Either NOP or DESELECT command may be applied.
  3. DM represents DM for x4/x8 configuration and UDM, LDM for x16 configuration. DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16).
  4. In certain cases where a READ cycle is interrupted, CKE going HIGH may result in the completion of the burst.
  5. Initialization timing is shown in Figure 8 on page 19.



## ODT Timing

Once a 12ns delay ( $t^{\text{MOD}}$ ) has been satisfied, and after the ODT function has been enabled via the EMR LOAD MODE command, ODT can be accessed under two timing categories. ODT will operate in either synchronous mode or asynchronous mode, depending on the state of CKE. ODT can switch anytime except during self refresh mode and a few clocks after being enabled via EMR, as shown in Figure 54 on page 75.

There are two timing categories for ODT—turn-on and turn-off. During active mode (CKE HIGH) and fast-exit power-down mode (any row of any bank open, CKE LOW, MR[12 = 0]),  $t^{\text{AOND}}$ ,  $t^{\text{AON}}$ ,  $t^{\text{AOFD}}$ , and  $t^{\text{AOF}}$  timing parameters are applied, as shown in Figure 56 on page 76.

During slow-exit power-down mode (any row of any bank open, CKE LOW, MR[12] = 1) and precharge power-down mode (all banks/rows precharged and idle, CKE LOW),  $t^{\text{AONPD}}$  and  $t^{\text{AOFPD}}$  timing parameters are applied, as shown in Figure 57 on page 76.

ODT turn-off timing, prior to entering any power-down mode, is determined by the parameter  $t^{\text{ANPD}}$  (MIN), as shown in Figure 58 on page 77. At state T2, the ODT HIGH signal satisfies  $t^{\text{ANPD}}$  (MIN) prior to entering power-down mode at T5. When  $t^{\text{ANPD}}$  (MIN) is satisfied,  $t^{\text{AOFD}}$  and  $t^{\text{AOF}}$  timing parameters apply. Figure 58 on page 77 also shows the example where  $t^{\text{ANPD}}$  (MIN) is *not* satisfied since ODT HIGH does not occur until state T3. When  $t^{\text{ANPD}}$  (MIN) is *not* satisfied,  $t^{\text{AOFPD}}$  timing parameters apply.

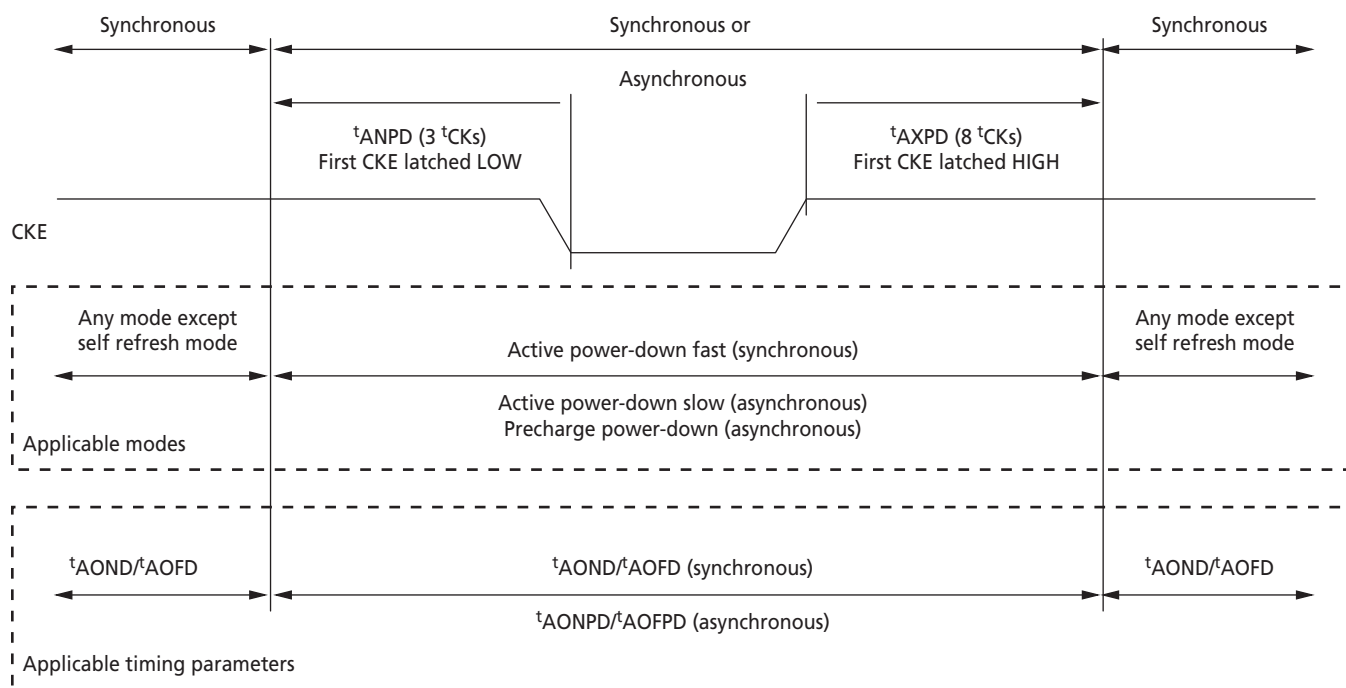
ODT turn-on timing prior to entering any power-down mode is determined by the parameter  $t^{\text{ANPD}}$ , as shown in Figure 59 on page 77. At state T2, the ODT HIGH signal satisfies  $t^{\text{ANPD}}$  (MIN) prior to entering power-down mode at T5. When  $t^{\text{ANPD}}$  (MIN) is satisfied,  $t^{\text{AOND}}$  and  $t^{\text{AON}}$  timing parameters apply. Figure 59 also shows the example where  $t^{\text{ANPD}}$  (MIN) is *not* satisfied since ODT HIGH does not occur until state T3. When  $t^{\text{ANPD}}$  (MIN) is *not* satisfied,  $t^{\text{AONPD}}$  timing parameters apply.

ODT turn-off timing after exiting any power-down mode is determined by the parameter  $t^{\text{AXPD}}$  (MIN), as shown in Figure 60 on page 78. At state Ta1, the ODT LOW signal satisfies  $t^{\text{AXPD}}$  (MIN) after exiting power-down mode at state T1. When  $t^{\text{AXPD}}$  (MIN) is satisfied,  $t^{\text{AOFD}}$  and  $t^{\text{AOF}}$  timing parameters apply. Figure 60 also shows the example where  $t^{\text{AXPD}}$  (MIN) is *not* satisfied since ODT LOW occurs at state Ta0. When  $t^{\text{AXPD}}$  (MIN) is *not* satisfied,  $t^{\text{AOFPD}}$  timing parameters apply.

ODT turn-on timing after exiting either slow-exit power-down mode or precharge power-down mode is determined by the parameter  $t^{\text{AXPD}}$  (MIN), as shown in Figure 61 on page 78. At state Ta1, the ODT HIGH signal satisfies  $t^{\text{AXPD}}$  (MIN) after exiting power-down mode at state T1. When  $t^{\text{AXPD}}$  (MIN) is satisfied,  $t^{\text{AOND}}$  and  $t^{\text{AON}}$  timing parameters apply. Figure 61 also shows the example where  $t^{\text{AXPD}}$  (MIN) is *not* satisfied since ODT HIGH occurs at state Ta0. When  $t^{\text{AXPD}}$  (MIN) is *not* satisfied,  $t^{\text{AONPD}}$  timing parameters apply.



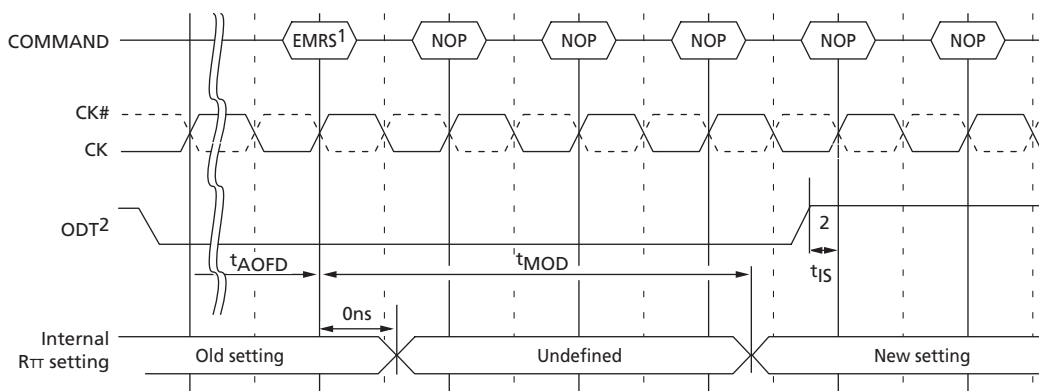
Figure 54: ODT Timing for Entering and Exiting Power-Down Mode



### MRS Command to ODT Update Delay

During normal operation, the value of the effective termination resistance can be changed with an EMRS set command.  $t_{MOD}$  (MAX) updates the RTT setting.

Figure 55: Timing for MRS Command to ODT Update Delay



- Notes:
1. LM command directed to mode register, which updates the information in EMR(1)[A6, A2], i.e., RTT (nominal).
  2. To prevent any impedance glitch on the channel, the following conditions must be met:  $t_{AOFD}$  must be met before issuing the LM command; ODT must remain LOW for the entire duration of the  $t_{MOD}$  window until  $t_{MOD}$  is met.



1Gb: x4, x8, x16 1.5V DDR2 SDRAM ODT Timing

Figure 56: ODT Timing for Active or Fast-Exit Power-Down Mode

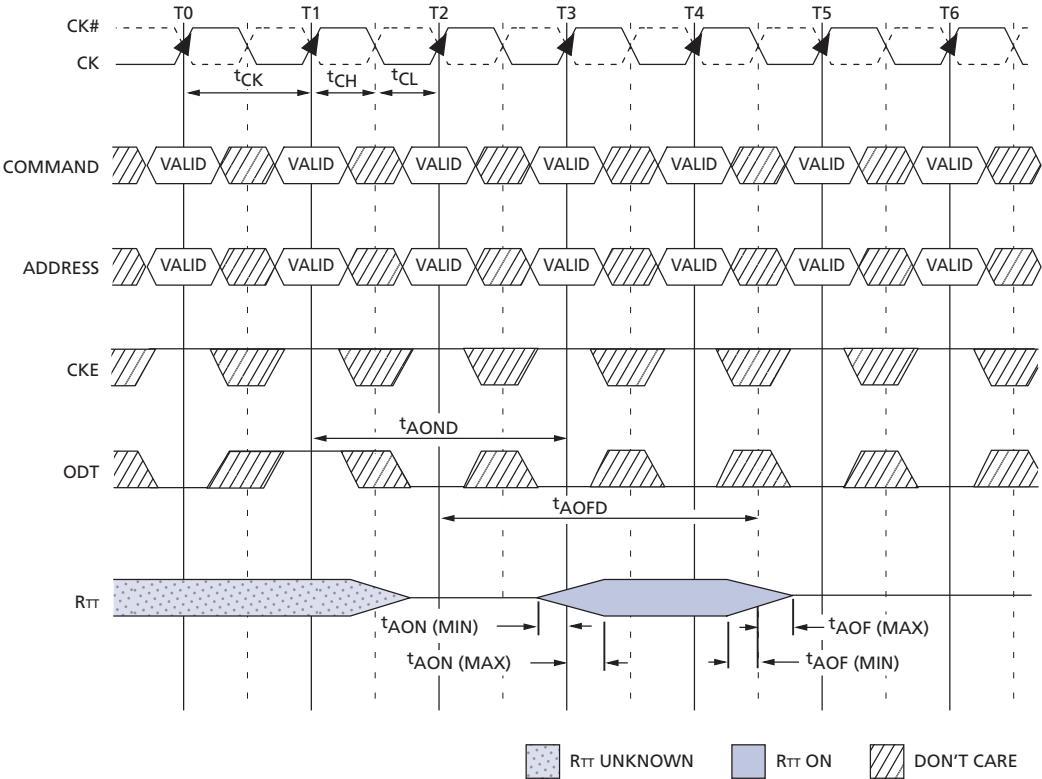


Figure 57: ODT Timing for Slow-Exit or Precharge Power-Down Modes

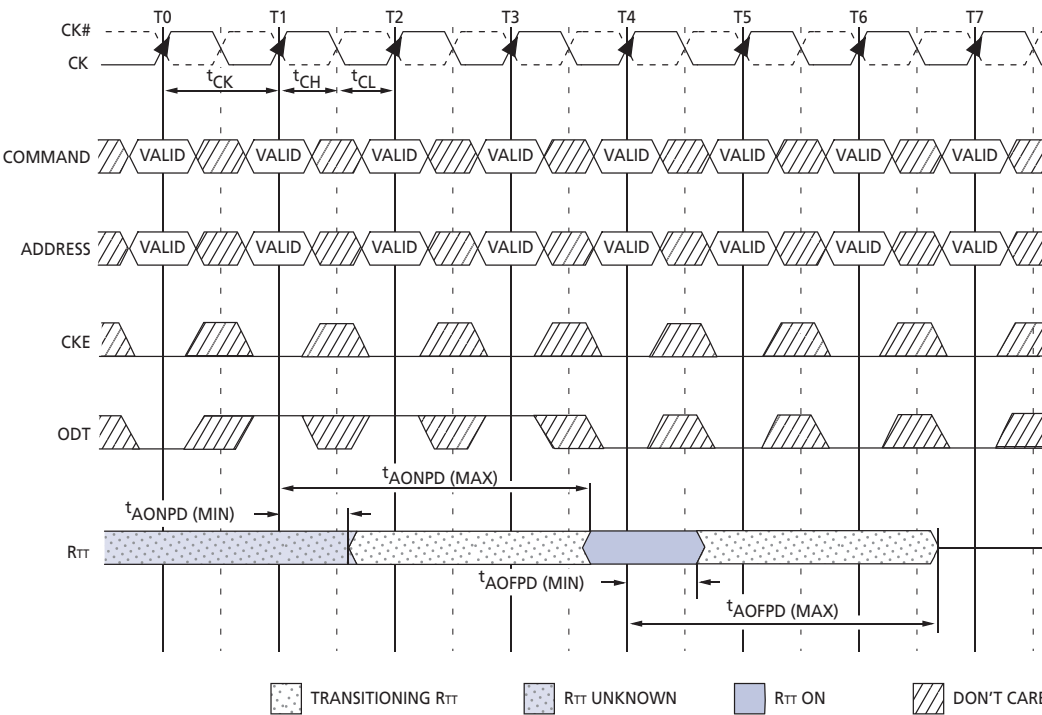




Figure 58: ODT Turn-Off Timings When Entering Power-Down Mode

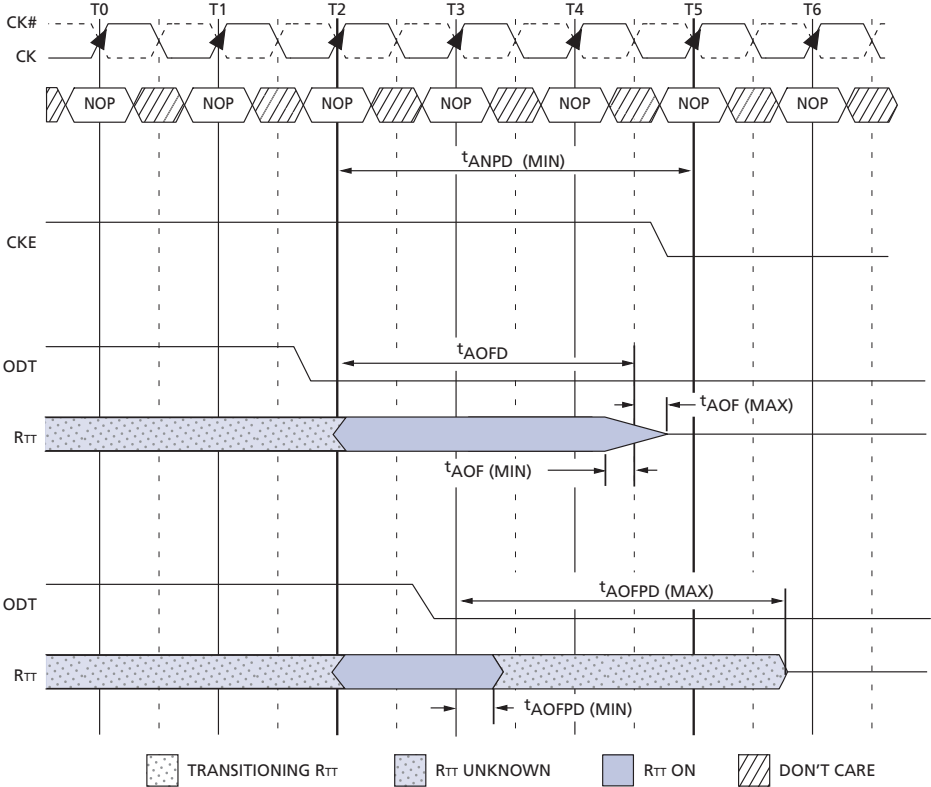
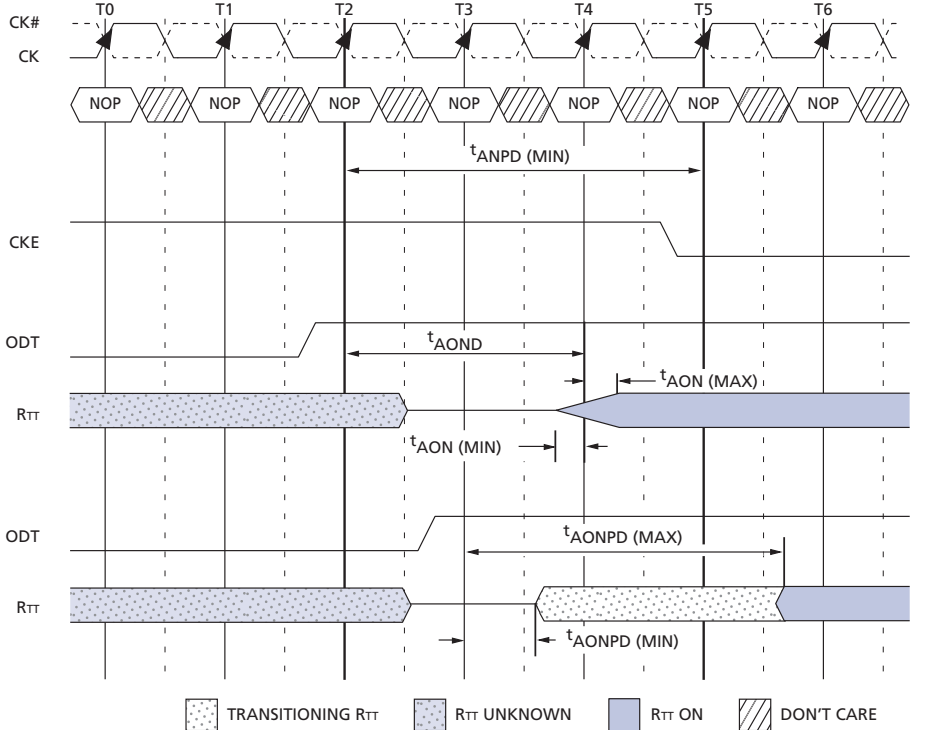


Figure 59: ODT Turn-On Timing When Entering Power-Down Mode





# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM ODT Timing

Figure 60: ODT Turn-Off Timing When Exiting Power-Down Mode

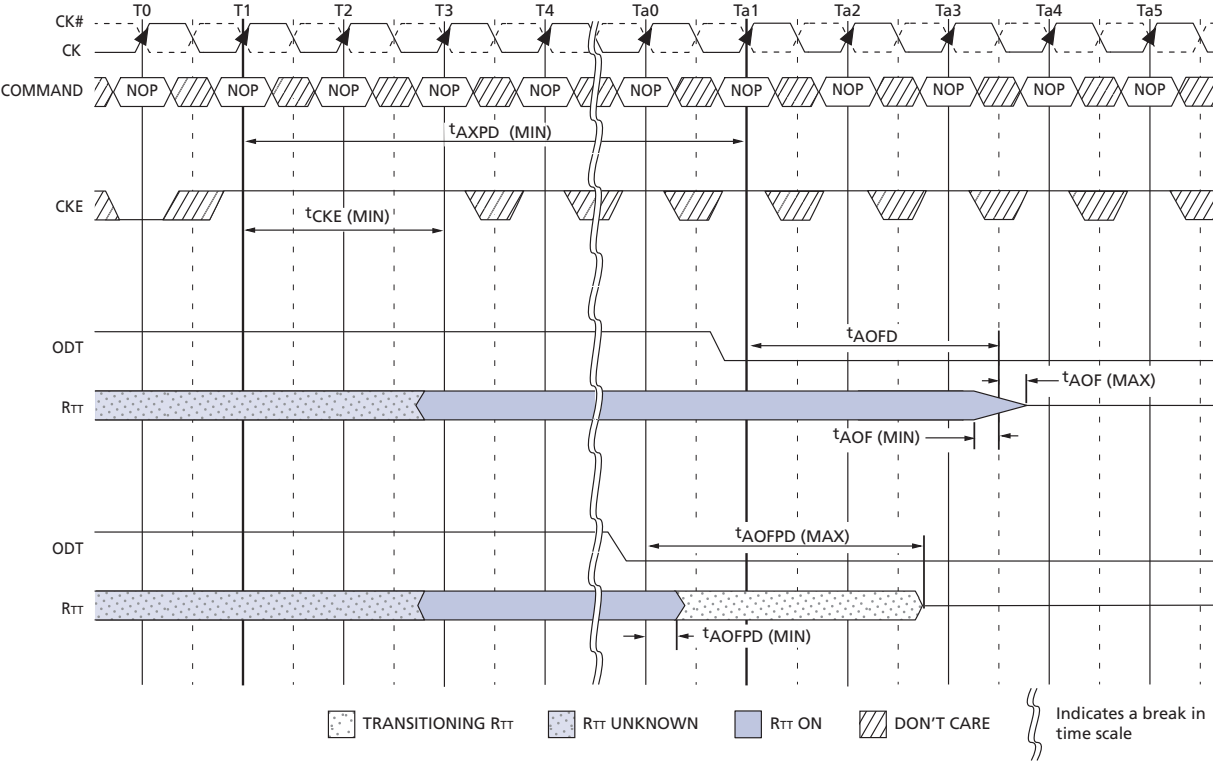
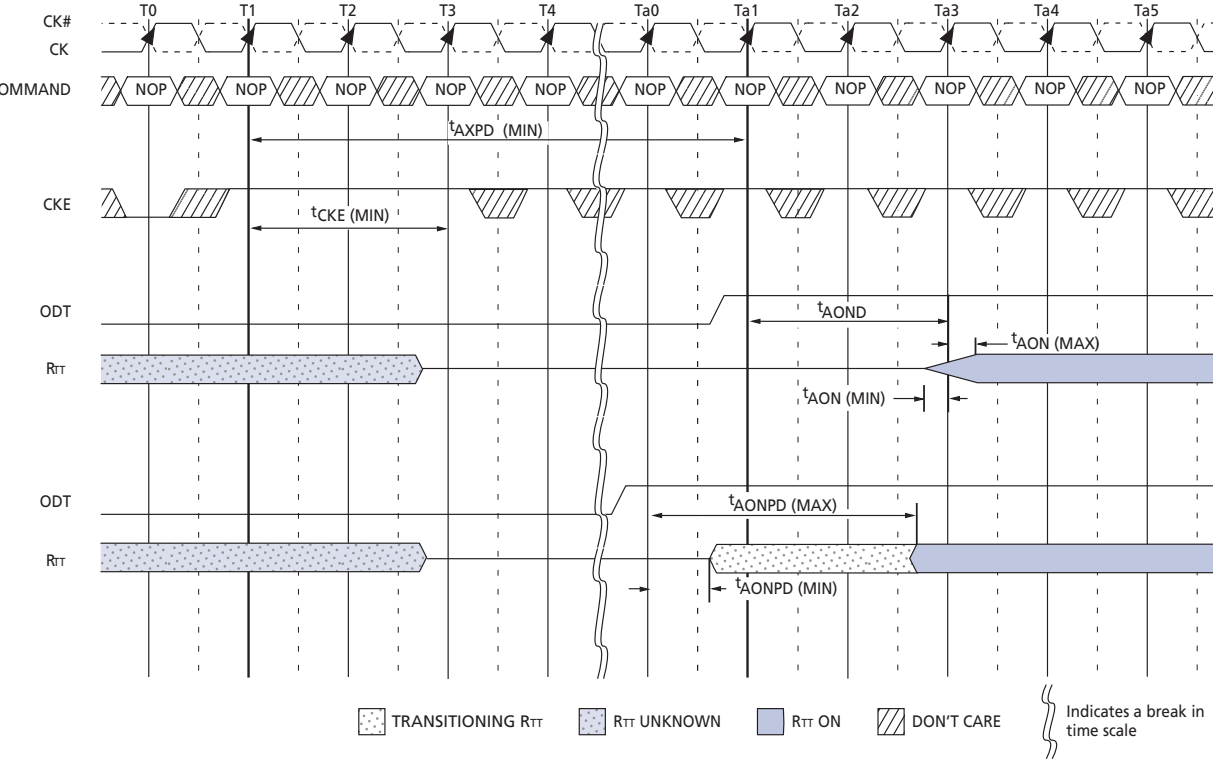


Figure 61: ODT Turn-On Timing When Exiting Power-Down Mode





## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 12: Absolute Maximum DC Ratings**

Parameter	Symbol	Min	Max	Units	Notes
VDD supply voltage relative to VSS	VDD	-1.0	1.8	V	1
VDDQ supply voltage relative to VSSQ	VDDQ	-0.5	1.8	V	1, 2
VDDL supply voltage relative to VSSL	VDDL	-0.5	1.8	V	1
Voltage on any ball relative to VSS	VIN, VOUT	-0.5	1.8	V	3
Input leakage current; any input $0V \leq V_{IN} \leq V_{DD}$ ; all other balls not under test = 0V	II	-5	5	$\mu A$	
Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$ ; DQ and ODT disabled	IOZ	-5	5	$\mu A$	
VREF leakage current; VREF = Valid VREF level	IVREF	-2	2	$\mu A$	

- Notes:
1. VDD, VDDQ, and VDDL must be within 300mV of each other at all times.
  2. VREF  $\leq 0.6 \times V_{DDQ}$ ; however, VREF may be  $\geq V_{DDQ}$  provided that VREF  $\leq 300mV$ .
  3. Voltage on any I/O may not exceed voltage on VDDQ.

## Temperature and Thermal Impedance

It is imperative that the temperature specifications, shown in Table 13 on page 80, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 14 on page 80 for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the thermal impedances listed below. For designs that are expected to last several years and require the flexibility to use several designs, consider using final target theta values, rather than existing values, to account for larger thermal impedances.

The safe junction temperature range can be maintained when the  $T_C$  specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Temperature and Thermal Impedance

**Table 13: Temperature Limits**

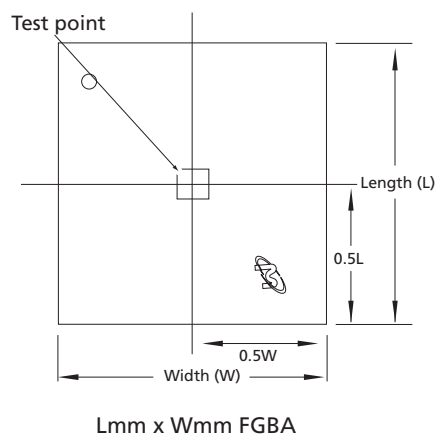
Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	$T_{STG}$	-55	150	°C	1
Operating temperature: commercial	$T_C$	0	95	°C	2, 3

- Notes:
1. The maximum storage case temperature is measured in the center of the package, as shown in Figure 62. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
  2. The maximum operating case temperature is measured in the center of the package, as shown in Figure 62.
  3. Device functionality is not guaranteed if the device exceeds maximum  $T_C$  during operation.

**Table 14: Thermal Impedance**

Die Revision	Package	Substrate	$\theta_{JA}$ (°C/W) Airflow = 0m/s	$\theta_{JA}$ (°C/W) Airflow = 1m/s	$\theta_{JA}$ (°C/W) Airflow = 2m/s	$\theta_{JB}$ (°C/W)	$\theta_{JC}$ (°C/W)
E <sup>1</sup>	60-ball	2-layer	56.7	42.1	36.8	22.7	2.5
		4-layer	40.2	32.8	29.9	22.1	
	84-ball	2-layer	52.9	41.3	35.7	21.6	2.5
		4-layer	38.4	32	28.9	21.5	
Last shrink target <sup>2</sup>	68-ball	2-layer	65	48	45	25	6.0
		4-layer	45	38	34	25	
	84-ball	2-layer	55	45	37	23	6.0
		4-layer	40	35	30	23	

- Notes:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.
  2. This is an estimate; simulated number and actual results could vary.

**Figure 62: Example Temperature Test Point Location**






## AC and DC Operating Conditions

**Table 15: Recommended DC Operating Conditions (SSTL\_18)**

All voltages referenced to Vss

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	VDD	1.425	1.5	1.625	V	1, 5
VDDL supply voltage	VDDL	1.425	1.5	1.625	V	4, 5
I/O supply voltage	VDDQ	1.425	1.5	1.625	V	4, 5
I/O reference voltage	VREF(DC)	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
I/O termination voltage (system)	VTT	VREF(DC) - 35	VREF(DC)	VREF(DC) + 35	mV	3

- Notes:
- VDD and VDDQ must track each other. VDDQ must be  $\leq$  VDD.
  - VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed  $\pm 1$  percent of the DC value. Peak-to-peak AC noise on VREF may not exceed  $\pm 2$  percent of VREF(DC). This measurement is to be taken at the nearest VREF bypass capacitor.
  - VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
  - VDDQ tracks with VDD; VDDL tracks with VDD.
  - VSSQ = VSSL = VSS.

**Table 16: ODT DC Electrical Characteristics**

All voltages referenced to Vss

Parameter	Symbol	Min	Nom	Max	Units	Notes
RTT effective impedance value for 75 $\Omega$ setting EMR (A6, A2) = 0, 1	RTT1(EFF)	60	80	98	$\Omega$	1
RTT effective impedance value for 150 $\Omega$ setting EMR (A6, A2) = 1, 0	RTT2(EFF)	120	160	195	$\Omega$	1
RTT effective impedance value for 50 $\Omega$ setting EMR (A6, A2) = 1, 1	RTT3(EFF)	40	55	65	$\Omega$	1
Deviation of VM with respect to VDDQ/2	$\Delta VM$	-6		6	%	2

- Notes:
- RTT1(EFF) and RTT2(EFF) are determined by separately applying  $V_{IH}(AC)$  and  $V_{IL}(AC)$  to the ball being tested, and then measuring current,  $I(V_{IH}(AC))$ , and  $I(V_{IL}(AC))$ , respectively.

(EQ 1)

$$RTT(EFF) = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

- Measure voltage (VM) at tested ball with no load.

(EQ 2)

$$\Delta VM = \left( \frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$



# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Electrical Characteristics and Operating Conditions

## Input Electrical Characteristics and Operating Conditions

**Table 17: Input DC Logic Levels**

All voltages referenced to  $V_{SS}$

Parameter	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage	$V_{IH}(DC)$	$V_{REF}(DC) + 125$	$V_{DDQ}^1$	mV
Input LOW (logic 0) voltage	$V_{IL}(DC)$	-300	$V_{REF}(DC) - 125$	mV

Notes: 1.  $V_{DDQ} + 250mV$  is permitted, provided that 1.8V is not exceeded.

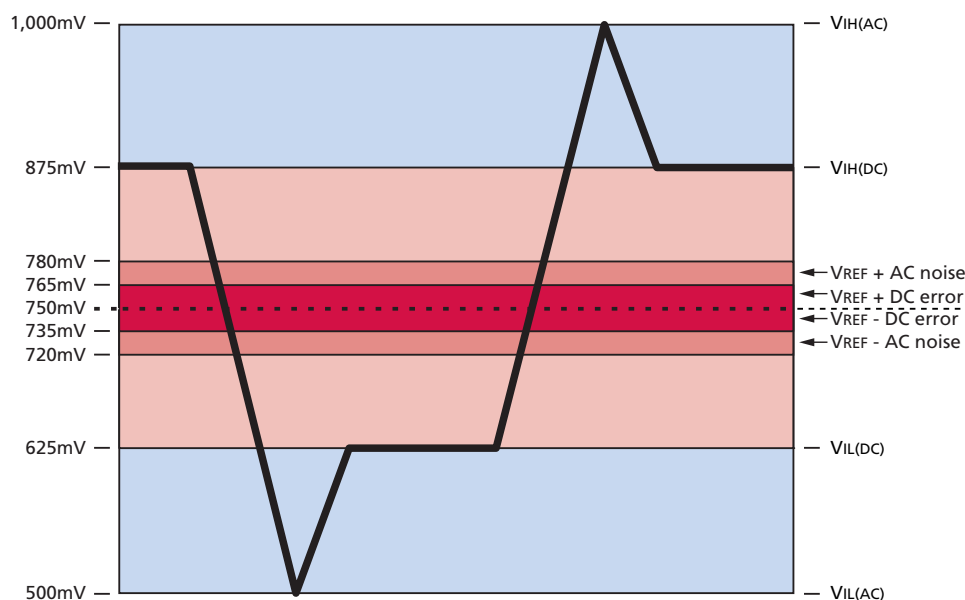
**Table 18: Input AC Logic Levels**

All voltages referenced to  $V_{SS}$

Parameter	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage (-5E/-37E)	$V_{IH}(AC)$	$V_{REF}(DC) + 250$	$V_{DDQ}^1$	mV
Input HIGH (logic 1) voltage (-3/-3E/-25/-25E/-187E)	$V_{IH}(AC)$	$V_{REF}(DC) + 200$	$V_{DDQ}^1$	mV
Input LOW (logic 0) voltage (-5E/-37E)	$V_{IL}(AC)$	-300	$V_{REF}(DC) - 250$	mV
Input LOW (logic 0) voltage (-3/-3E/-25/-25E/-187E)	$V_{IL}(AC)$	-300	$V_{REF}(DC) - 200$	mV

Notes: 1.  $V_{DDQ} + 250mV$  is permitted, provided that 1.8V is not exceeded.

**Figure 63: Single-Ended Input Signal Levels**



Notes: 1. Numbers in diagram reflect nominal 1.5V DDR2-400/DDR2-533 values.



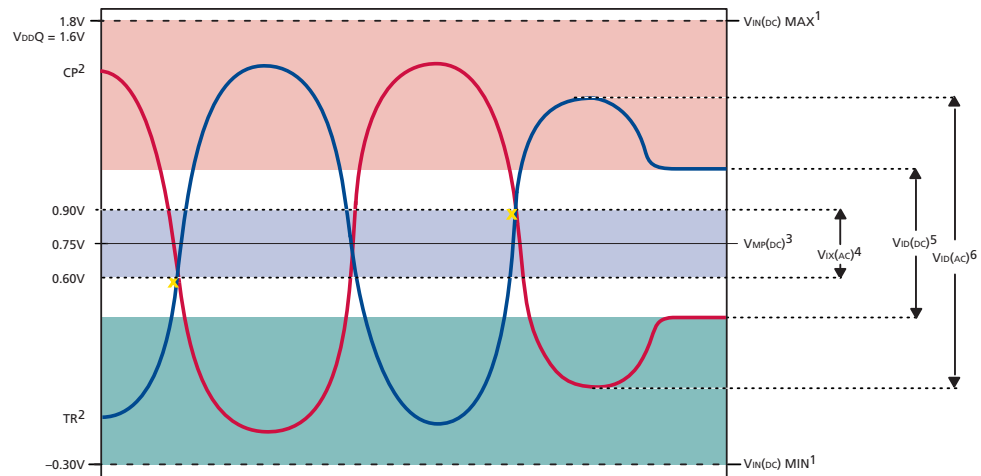
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Electrical Characteristics and Operating Conditions

**Table 19: Differential Input Logic Levels**

 All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Units	Notes
DC input signal voltage	V <sub>IN(DC)</sub>	-300	V <sub>DDQ</sub> <sup>6</sup>	mV	1
DC differential input voltage	V <sub>ID(DC)</sub>	250	V <sub>DDQ</sub> <sup>6</sup>	mV	2
AC differential input voltage	V <sub>ID(AC)</sub>	500	V <sub>DDQ</sub> <sup>6</sup>	mV	3
AC differential cross-point voltage	V <sub>IX(AC)</sub>	0.50 x V <sub>DDQ</sub> - 150	0.50 x V <sub>DDQ</sub> + 150	mV	4
Input midpoint voltage	V <sub>MP(DC)</sub>	V <sub>REF(DC)</sub> - 50	V <sub>REF(DC)</sub> + 65	mV	5

- Notes:
- V<sub>IN(DC)</sub> specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
  - V<sub>ID(DC)</sub> specifies the input differential voltage |V<sub>TR</sub> - V<sub>CP</sub>| required for switching, where V<sub>TR</sub> is the true input (such as CK, DQS, LDQS, UDQS) level and V<sub>CP</sub> is the complementary input (such as CK#, DQS#, LDQS#, UDQS#). The minimum value is equal to V<sub>IH(DC)</sub> - V<sub>IL(DC)</sub>. Differential input signal levels are shown in Figure 64.
  - V<sub>ID(AC)</sub> specifies the input differential voltage |V<sub>TR</sub> - V<sub>CP</sub>| required for switching, where V<sub>TR</sub> is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V<sub>CP</sub> is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to V<sub>IH(AC)</sub> - V<sub>IL(AC)</sub>, as shown in Table 18 on page 82.
  - The typical value of V<sub>IX(AC)</sub> is expected to be about 0.5 x V<sub>DDQ</sub> of the transmitting device and V<sub>IX(AC)</sub> is expected to track variations in V<sub>DDQ</sub>. V<sub>IX(AC)</sub> indicates the voltage at which differential input signals must cross, as shown in Figure 64.
  - V<sub>MP(DC)</sub> specifies the input differential common mode voltage (V<sub>TR</sub> + V<sub>CP</sub>)/2 where V<sub>TR</sub> is the true input (CK, DQS) level and V<sub>CP</sub> is the complementary input (CK#, DQS#). V<sub>MP(DC)</sub> is expected to be approximately 0.5 x V<sub>DDQ</sub>.
  - V<sub>DDQ</sub> + 250mV is permitted, provided that 1.8V is not exceeded.

**Figure 64: Differential Input Signal Levels**


- Notes:
- TR and CP may not be more positive than V<sub>DDQ</sub> + 0.250V (provided 1.8V is not exceeded) or more negative than V<sub>SS</sub> - 0.3V.
  - TR represents the CK, DQS, RDQS, LDQS, and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS#, and UDQS# signals.
  - This provides a minimum of 700mV to a maximum of 815mV and is expected to be V<sub>DDQ</sub>/2.
  - TR and CP must cross in this region.
  - TR and CP must meet at least V<sub>ID(DC)</sub> MIN when static and is centered around V<sub>MP(DC)</sub>.
  - TR and CP must have a minimum 500mV peak-to-peak swing.
  - Numbers in diagram reflect nominal values (V<sub>DDQ</sub> = 1.5V).



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Electrical Characteristics and Operating Conditions

**Table 20: AC Input Test Conditions**

Parameter	Symbol	Min	Max	Units	Notes
Input setup timing measurement reference level bank address pins, address pins, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	VRS	See Note 2			1, 2, 7, 8
Input hold timing measurement reference level bank address pins, address pins, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	VRH	See Note 3			1, 3, 7, 8
Input timing measurement reference level (single-ended) DQS for x4, x8; UDQS, LDQS for x16	VREF(DC)	VDDQ x 0.49	VDDQ x 0.51	V	1, 4, 7, 8
Input timing measurement reference level (differential) CK, CK# for x4, x8, x16; DQS, DQS# for x4, x8; RDQS, RDQS# for x8; UDQS, UDQS#, LDQS, LDQS# for x16	VRD	V <sub>IX</sub> (AC)		V	1, 5, 6, 7, 9

- Notes:
- All voltages referenced to V<sub>SS</sub>.
  - Input waveform setup timing ( $t_{ISb}$ ) is referenced from the input signal crossing at the V<sub>IH</sub>(AC) level for a rising signal and V<sub>IL</sub>(AC) for a falling signal applied to the device under test, as shown in Figure 73 on page 95.
  - Input waveform hold ( $t_{IHb}$ ) timing is referenced from the input signal crossing at the V<sub>IL</sub>(DC) level for a rising signal and V<sub>IH</sub>(DC) for a falling signal applied to the device under test, as shown in Figure 73 on page 95.
  - Input waveform setup timing ( $t_{DS}$ ) and hold timing ( $t_{DH}$ ) for single-ended data strobe is referenced from the crossing of DQS, UDQS, or LDQS through the VREF level applied to the device under test, as shown in Figure 75 on page 96.
  - Input waveform setup timing ( $t_{DS}$ ) and hold timing ( $t_{DH}$ ) when differential data strobe is enabled is referenced from the cross-point of DQS/DQS#, UDQS/UDQS#, or LDQS/LDQS#, as shown in Figure 74 on page 95.
  - Input waveform timing is referenced to the crossing point level (V<sub>IX</sub>) of two input signals (V<sub>TR</sub> and V<sub>CP</sub>) applied to the device under test, where V<sub>TR</sub> is the true input signal and V<sub>CP</sub> is the complementary input signal, as shown in Figure 76 on page 96.
  - See "Input Slew Rate Derating" on page 85.
  - The slew rate for single-ended inputs is measured from DC level to AC level, V<sub>IL</sub>(DC) to V<sub>IH</sub>(AC) on the rising edge and V<sub>IL</sub>(AC) to V<sub>IH</sub>(DC) on the falling edge. For signals referenced to VREF, the valid intersection is where the "tangent" line intersects VREF, as shown in Figures 66, 68, 70, and 72.
  - The slew rate for differentially ended inputs is measured from twice the DC level to twice the AC level: 2 x V<sub>IL</sub>(DC) to 2 x V<sub>IH</sub>(AC) on the rising edge and 2 x V<sub>IL</sub>(AC) to 2 x V<sub>IH</sub>(DC) on the falling edge. For example, the CK/CK# would be -250mV to +500mV for CK rising edge and would be +250mV to -500mV for CK falling edge.



## Input Slew Rate Derating

For all input signals, the total  $t_{IS}$  (setup time) and  $t_{IH}$  (hold time) required is calculated by adding the data sheet  $t_{IS}$  (base) and  $t_{IH}$  (base) value to the  $\Delta t_{IS}$  and  $\Delta t_{IH}$  derating value, respectively. Example:  $t_{IS}$  (total setup time) =  $t_{IS}$  (base) +  $\Delta t_{IS}$ .

$t_{IS}$ , the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of  $V_{REF(DC)}$  and the first crossing of  $V_{IH(AC)}$  MIN. Setup nominal slew rate ( $t_{IS}$ ) for a falling signal is defined as the slew rate between the last crossing of  $V_{REF(DC)}$  and the first crossing of  $V_{IL(AC)}$  MAX.

If the actual signal is always earlier than the nominal slew rate line between shaded “ $V_{REF(DC)}$  to AC region,” use nominal slew rate for derating value (Figure 65 on page 87).

If the actual signal is later than the nominal slew rate line anywhere between shaded “ $V_{REF(DC)}$  to AC region,” the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 66 on page 87).

$t_{IH}$ , the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of  $V_{IL(DC)}$  MAX and the first crossing of  $V_{REF(DC)}$ .  $t_{IH}$ , nominal slew rate for a falling signal, is defined as the slew rate between the last crossing of  $V_{IH(DC)}$  MIN and the first crossing of  $V_{REF(DC)}$ .

If the actual signal is always later than the nominal slew rate line between shaded “DC to  $V_{REF(DC)}$  region,” use nominal slew rate for derating value (Figure 67 on page 88).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded “DC to  $V_{REF(DC)}$  region,” the slew rate of a tangent line to the actual signal from the DC level to  $V_{REF(DC)}$  level is used for the derating value (Figure 68 on page 88).

Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached  $V_{IH(AC)}/V_{IL(AC)}$  at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach  $V_{IH(AC)}/V_{IL(AC)}$ .

For slew rates in between the values listed in Tables 21 and 22, the derating values may be obtained by linear interpolation.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Table 21: 1.5V DDR2-400/533 Setup and Hold Time Derating Values ( $t_{IS}$  and  $t_{IH}$ )**

Command/ Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	-11	-14	+19	+16	+49	+46	ps
0.8	-25	-31	+5	-1	+35	+29	ps
0.7	-43	-54	-13	-24	+17	+6	ps
0.6	-67	-83	-37	-53	-7	-23	ps
0.5	-110	-125	-80	-95	-50	-65	ps
0.4	-175	-188	-145	-158	-115	-128	ps
0.3	-285	-292	-255	-262	-225	-232	ps
0.25	-350	-375	-320	-345	-290	-315	ps
0.2	-525	-500	-495	-470	-465	-440	ps
0.15	-800	-708	-770	-678	-740	-648	ps
0.1	-1,450	-1,125	-1,420	-1,095	-1,390	-1,065	ps

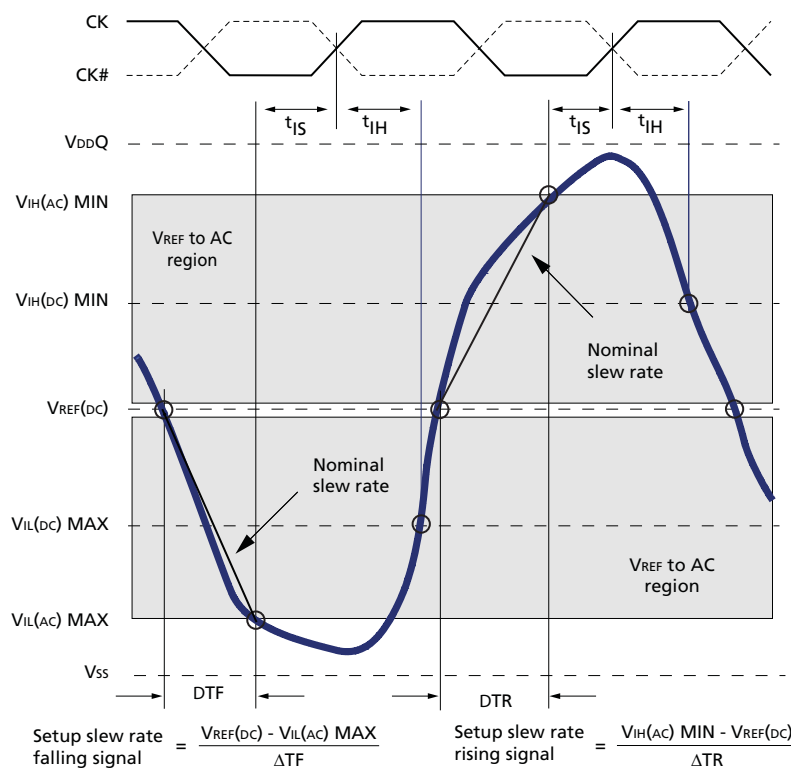
**Table 22: 1.5V DDR2-667/800/1066 Setup and Hold Time Derating Values ( $t_{IS}$  and  $t_{IH}$ )**

Command/ Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	
4.0	+150	+94	+180	+124	+210	+154	ps
3.5	+143	+89	+173	+119	+203	+149	ps
3.0	+133	+83	+163	+113	+193	+143	ps
2.5	+120	+75	+150	+105	+180	+135	ps
2.0	+100	+45	+160	+75	+160	+105	ps
1.5	+67	+21	+97	+51	+127	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	-5	-14	+25	+16	+55	+46	ps
0.8	-13	-31	+17	-1	+47	+29	ps
0.7	-22	-54	+8	-24	+38	+6	ps
0.6	-34	-83	-4	-53	+36	-23	ps
0.5	-60	-125	-30	-95	0	-65	ps
0.4	-100	-188	-70	-158	-40	-128	ps
0.3	-168	-292	-138	-262	-108	-232	ps
0.25	-200	-375	-170	-345	-140	-315	ps
0.2	-325	-500	-295	-470	-265	-440	ps
0.15	-517	-708	-487	-678	-457	-648	ps
0.1	-1,000	-1,125	-970	-1,095	-940	-1,065	ps

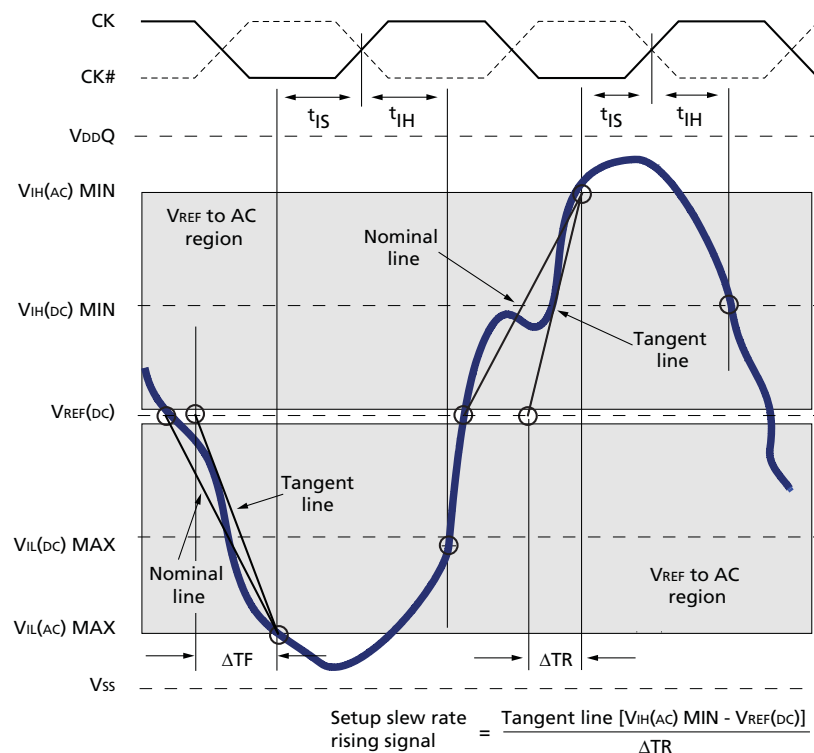


# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Figure 65: Nominal Slew Rate for  $t_{IS}$**



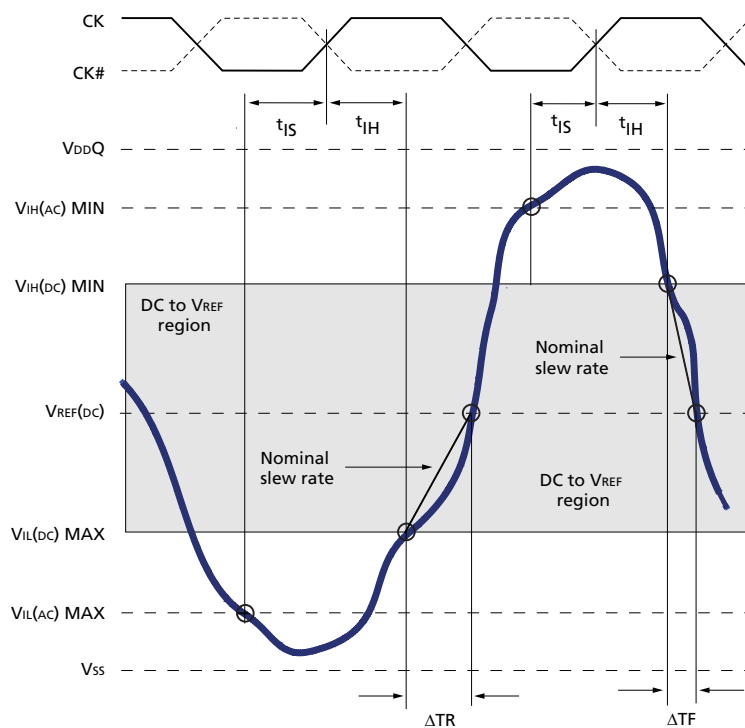
**Figure 66: Tangent Line for  $t_{IS}$**



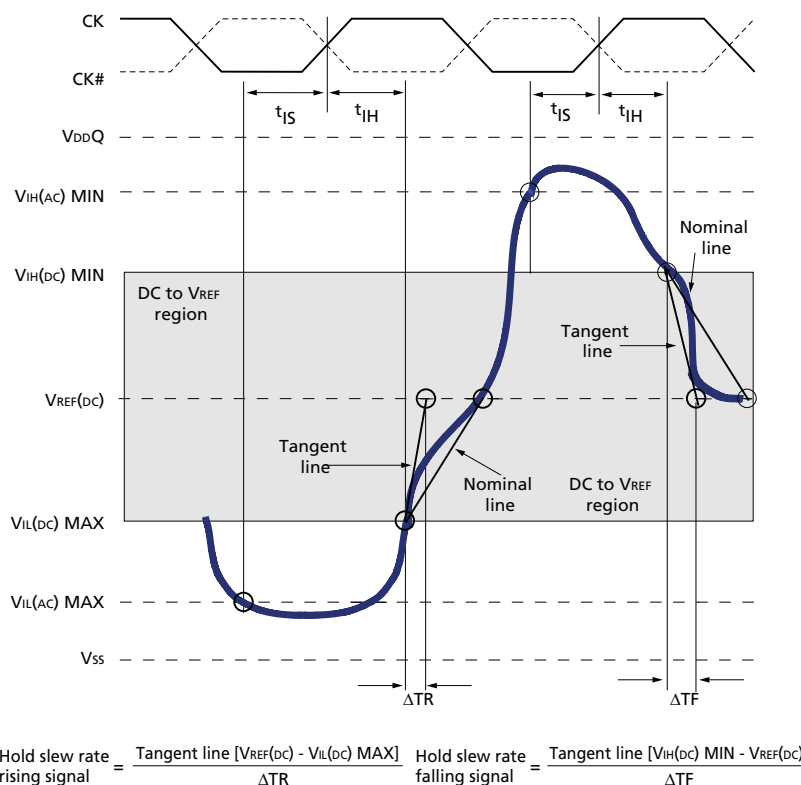


# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Figure 67: Nominal Slew Rate for  $t_{IH}$**



**Figure 68: Tangent Line for  $t_{IH}$**







## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Table 23: 1.5V DDR2-400/DDR2-533  $t_{DS}^{\Delta}$ ,  $t_{DH}^{\Delta}$  Derating Values with Differential Strobe**

All units are shown in ps

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$
2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

- Notes:
- For all input signals, the total  $t_{DS}^{\Delta}$  and  $t_{DH}^{\Delta}$  required is calculated by adding the data sheet value to the derating value listed in Table 23.
  - $t_{DS}^{\Delta}$  nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{REF}(DC)$  and the first crossing of  $V_{IH}(AC)$  MIN.  $t_{DS}^{\Delta}$  nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{REF}(DC)$  and the first crossing of  $V_{IL}(AC)$  MAX. If the actual signal is always earlier than the nominal slew rate line between shaded "VREF(DC) to AC region," use nominal slew rate for derating value (see Figure 69). If the actual signal is later than the nominal slew rate line anywhere between shaded "VREF(DC) to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 70).
  - $t_{DH}^{\Delta}$  nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL}(DC)$  MAX and the first crossing of  $V_{REF}(DC)$ .  $t_{DH}^{\Delta}$  nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH}(DC)$  MIN and the first crossing of  $V_{REF}(DC)$ . If the actual signal is always later than the nominal slew rate line between shaded "DC level to VREF(DC) region," use nominal slew rate for derating value (see Figure 71). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC) region," the slew rate of a tangent line to the actual signal from the DC level to  $V_{REF}(DC)$  level is used for derating value (see Figure 72).
  - Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached  $V_{IH}(AC)/V_{IL}(AC)$  at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach  $V_{IH}(AC)/V_{IL}(AC)$ .
  - For slew rates between the values listed in this table, the derating values may be obtained by linear interpolation.
  - These values are typically not subject to production test. They are verified by design and characterization.
  - Single-ended DQS requires special derating. The values in Table 25 are the DQS single-ended slew rate derating with DQS referenced at  $V_{REF}$  and DQ referenced at the logic levels  $t_{DS_b}^{\Delta}$  and  $t_{DH_b}^{\Delta}$ . Table 27 provides the  $V_{REF}$ -based fully derated values for the DQ ( $t_{DS_a}^{\Delta}$  and  $t_{DH_a}^{\Delta}$ ) for 1.5V DDR2-533. Table 28 provides the  $V_{REF}$ -based fully derated values for the DQ ( $t_{DS_a}^{\Delta}$  and  $t_{DH_a}^{\Delta}$ ) for 1.5V DDR2-400.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Table 24: 1.5V DDR2-667/DDR2-800/DDR2-1066  $t_{DS}$ ,  $t_{DH}$  Derating Values with Differential Strobe**  
All units are shown in ps

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$	$t_{DS}^{\Delta}$	$t_{DH}^{\Delta}$
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72
0.9	-5	-14	-5	-14	-5	-14	7	-2	19	10	31	22	43	34	55	46	67	58
0.8	-13	-31	-13	-31	-13	-31	-1	-19	11	-7	23	5	35	17	47	29	59	41
0.7	-22	-54	-22	-54	-22	-54	-10	-42	2	-30	14	-18	26	-6	38	6	50	18
0.6	-34	-83	-34	-83	-34	-83	-22	-71	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-60	-125	-60	-125	-60	-125	-48	-113	-36	-101	-24	-89	-12	-77	0	-65	12	-53
0.4	-100	-188	-100	-188	-100	-188	-88	-176	-76	-164	-64	-152	-52	-140	-40	-128	-28	-116

- Notes:
- For all input signals the total  $t_{DS}$  and  $t_{DH}$  required is calculated by adding the data sheet value to the derating value listed in Table 24.
  - $t_{DS}$  nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{REF}(DC)$  and the first crossing of  $V_{IH}(AC)$  MIN.  $t_{DS}$  nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{REF}(DC)$  and the first crossing of  $V_{IL}(AC)$  MAX. If the actual signal is always earlier than the nominal slew rate line between shaded "VREF(DC) to AC region," use nominal slew rate for derating value (see Figure 69). If the actual signal is later than the nominal slew rate line anywhere between shaded "VREF(DC) to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 70).
  - $t_{DH}$  nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL}(DC)$  MAX and the first crossing of  $V_{REF}(DC)$ .  $t_{DH}$  nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH}(DC)$  MIN and the first crossing of  $V_{REF}(DC)$ . If the actual signal is always later than the nominal slew rate line between shaded "DC level to VREF(DC) region," use nominal slew rate for derating value (see Figure 71). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC) region," the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for derating value (see Figure 72).
  - Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached  $V_{IH}(AC)/V_{IL}(AC)$  at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach  $V_{IH}(AC)/V_{IL}(AC)$ .
  - For slew rates between the values listed in this table, the derating values may be obtained by linear interpolation.
  - These values are typically not subject to production test. They are verified by design and characterization.
  - Single-ended DQS requires special derating. The values in Table 25 are the DQS single-ended slew rate derating with DQS referenced at  $V_{REF}$  and DQ referenced at the logic levels  $t_{DS_b}$  and  $t_{DH_b}$ . Table 26 provides the  $V_{REF}$ -based fully derated values for the DQ ( $t_{DS_a}$  and  $t_{DH_a}$ ) for 1.5V DDR2-667. It is not advised to operate 1.5V DDR2-800 and 1.5V DDR2-1066 devices with single-ended DQS; however Table 25 on page 91 would be used with the base values.



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Table 25: Single-Ended DQS Slew Rate Derating Values Using  $t_{DS_b}$  and  $t_{DH_b}$**

Reference points indicated in bold; Derating values, to be used with base  $t_{DS_b}$ - and  $t_{DH_b}$ -specified values

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$
2	130	53	130	53	130	53	130	53	130	53	145	48	155	45	165	41	175	38
1.5	97	32	97	32	97	32	97	32	97	32	112	27	122	24	132	20	142	17
1	30	-10	30	-10	30	-10	30	-10	30	-10	<b>45</b>	<b>-15</b>	55	-18	65	-22	75	-25
0.9	25	-24	25	-24	25	-24	25	-24	25	-24	40	-29	50	-32	60	-36	70	-39
0.8	17	-41	17	-41	17	-41	17	-41	17	-41	32	-46	42	-49	52	-53	61	-56
0.7	5	-64	5	-64	5	-64	5	-64	5	-64	20	-69	30	-72	40	-75	50	-79
0.6	-7	-93	-7	-93	-7	-93	-7	-93	-7	-93	8	-98	18	-102	28	-105	38	-108
0.5	-28	-135	-28	-135	-28	-135	-28	-135	-28	-135	-13	-140	-3	-143	7	-147	17	-150
0.4	-78	-198	-78	-198	-78	-198	-78	-198	-78	-198	-63	-203	-53	-206	-43	-210	-33	-213

**Table 26: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at 1.5V DDR2-667**

Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$	$t_{DS}$	$t_{DH}$
2	330	291	330	291	330	291	330	291	330	291	345	286	355	282	365	29	375	276
1.5	330	290	330	290	330	290	330	290	330	290	345	285	355	282	365	279	375	275
1	330	290	330	290	330	290	330	290	330	290	<b>345</b>	<b>285</b>	355	282	365	278	375	275
0.9	347	290	347	290	347	290	347	290	347	290	362	285	372	282	382	278	392	275
0.8	367	290	367	290	367	290	367	290	367	290	382	285	392	282	402	278	412	275
0.7	391	290	391	290	391	290	391	290	391	290	406	285	416	281	426	278	436	275
0.6	426	290	426	290	426	290	426	290	426	290	441	285	451	282	461	278	471	275
0.5	472	290	472	290	472	290	472	290	472	290	487	285	497	282	507	278	517	275
0.4	522	289	522	289	522	289	522	289	522	289	537	284	547	281	557	278	567	274



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Table 27: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at 1.5V DDR2-533**  
Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>
2	355	341	355	341	355	341	355	341	355	341	370	336	380	332	390	329	400	326
1.5	364	340	364	340	364	340	364	340	364	340	379	335	389	332	399	329	409	325
1	380	340	380	340	380	340	380	340	380	340	<b>395</b>	<b>335</b>	405	332	415	328	425	325
0.9	402	340	402	340	402	340	402	340	402	340	417	335	427	332	437	328	447	325
0.8	429	340	429	340	429	340	429	340	429	340	444	335	454	332	464	328	474	325
0.7	463	340	463	340	463	340	463	340	463	340	478	335	488	331	498	328	508	325
0.6	510	340	510	340	510	340	510	340	510	340	525	335	535	332	545	328	555	325
0.5	572	340	572	340	572	340	572	340	572	340	587	335	597	332	607	328	617	325
0.4	647	339	647	339	647	339	647	339	647	339	662	334	672	331	682	328	692	324

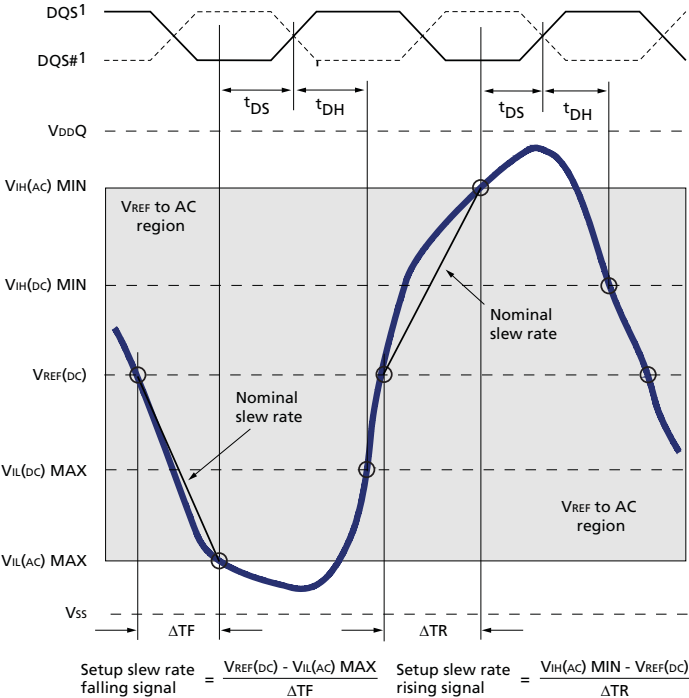
**Table 28: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at 1.5V DDR2-400**  
Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>	t <sub>DS</sub>	t <sub>DH</sub>
2	405	391	405	391	405	391	405	391	405	391	420	386	430	382	440	379	450	376
1.5	414	390	414	390	414	390	414	390	414	390	429	385	439	382	449	379	459	375
1	430	390	430	390	430	390	430	390	430	390	<b>445</b>	<b>385</b>	455	382	465	378	475	375
0.9	452	390	452	390	452	390	452	390	452	390	467	385	477	382	487	378	497	375
0.8	479	390	479	390	479	390	479	390	479	390	494	385	504	382	514	378	524	375
0.7	513	390	513	390	513	390	513	390	513	390	528	385	538	381	548	378	558	375
0.6	560	390	560	390	560	390	560	390	560	390	575	385	585	382	595	378	605	375
0.5	622	390	622	390	622	390	622	390	622	390	637	385	647	382	657	378	667	375
0.4	697	389	697	389	697	389	697	389	697	389	712	384	722	381	732	378	742	374



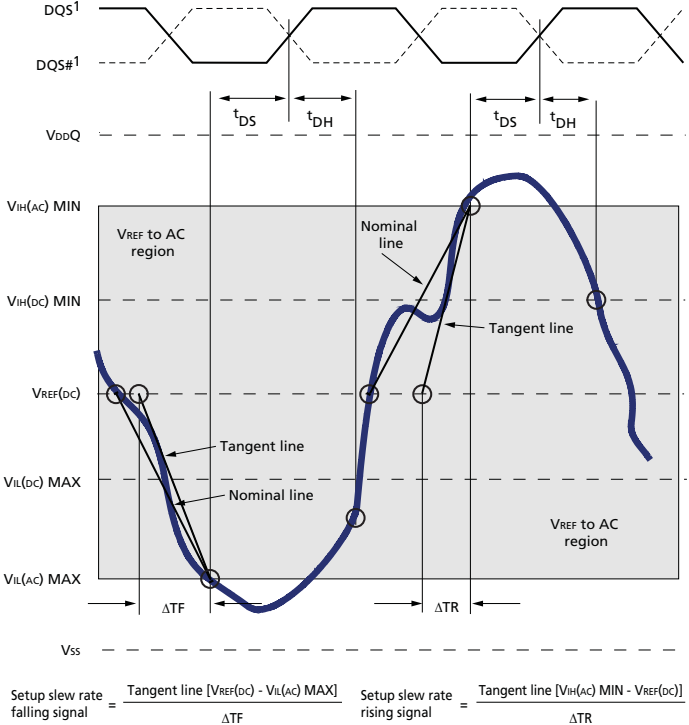
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

Figure 69: Nominal Slew Rate for t<sub>DS</sub>



Notes: 1. DQS, DQS# signals must be monotonic between V<sub>IL(DC)</sub> MAX and V<sub>IH(DC)</sub> MIN.

Figure 70: Tangent Line for t<sub>DS</sub>

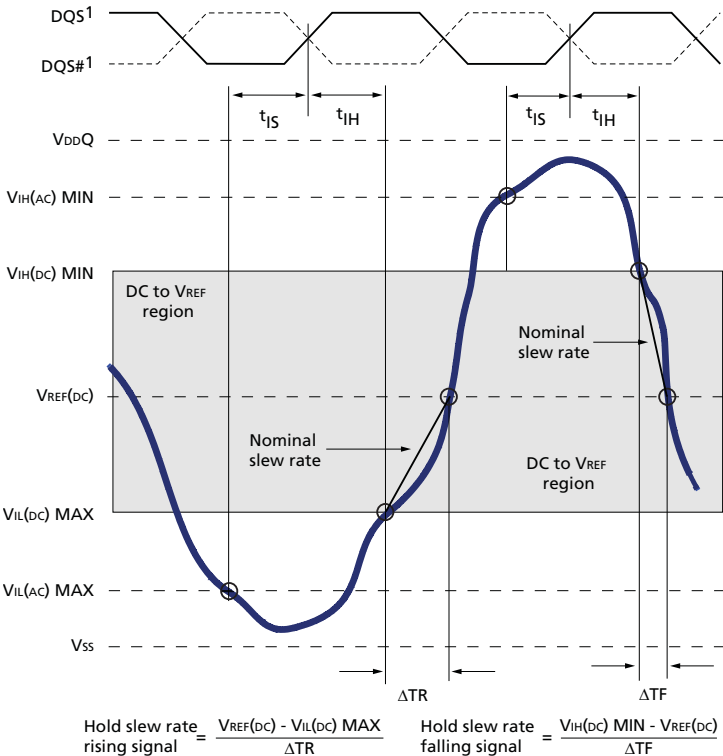


Notes: 1. DQS, DQS# signals must be monotonic between V<sub>IL(DC)</sub> MAX and V<sub>IH(DC)</sub> MIN.



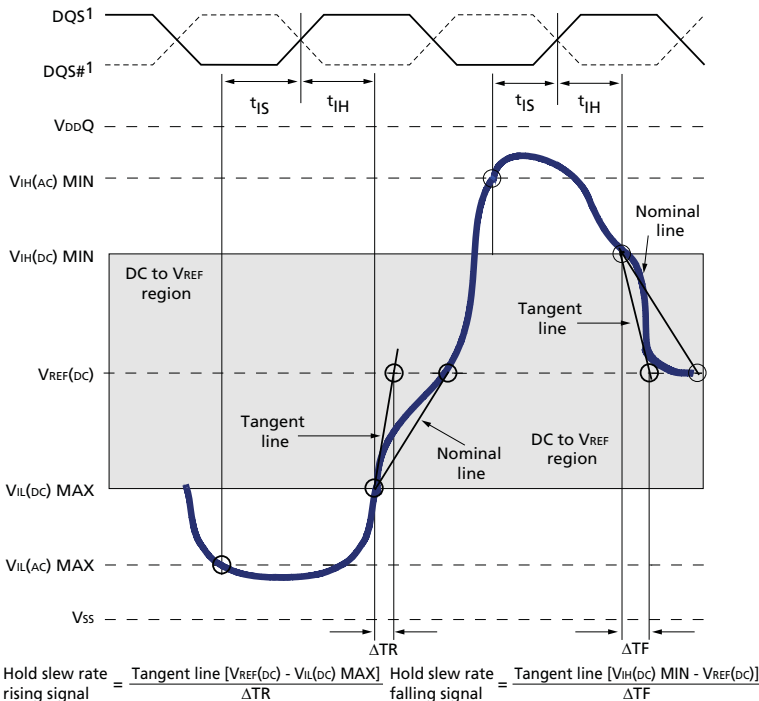
# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

Figure 71: Nominal Slew Rate for t<sub>DH</sub>



Notes: 1. DQS, DQS# signals must be monotonic between V<sub>IL(DC) MAX</sub> and V<sub>IH(DC) MIN</sub>.

Figure 72: Tangent Line for t<sub>DH</sub>

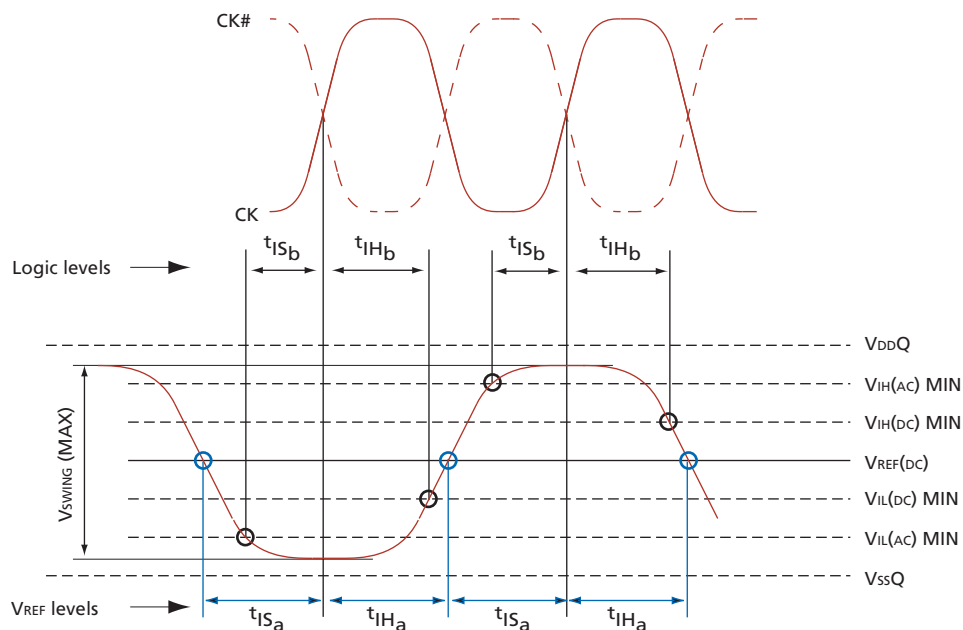


Notes: 1. DQS, DQS# signals must be monotonic between V<sub>IL(DC) MAX</sub> and V<sub>IH(DC) MIN</sub>.

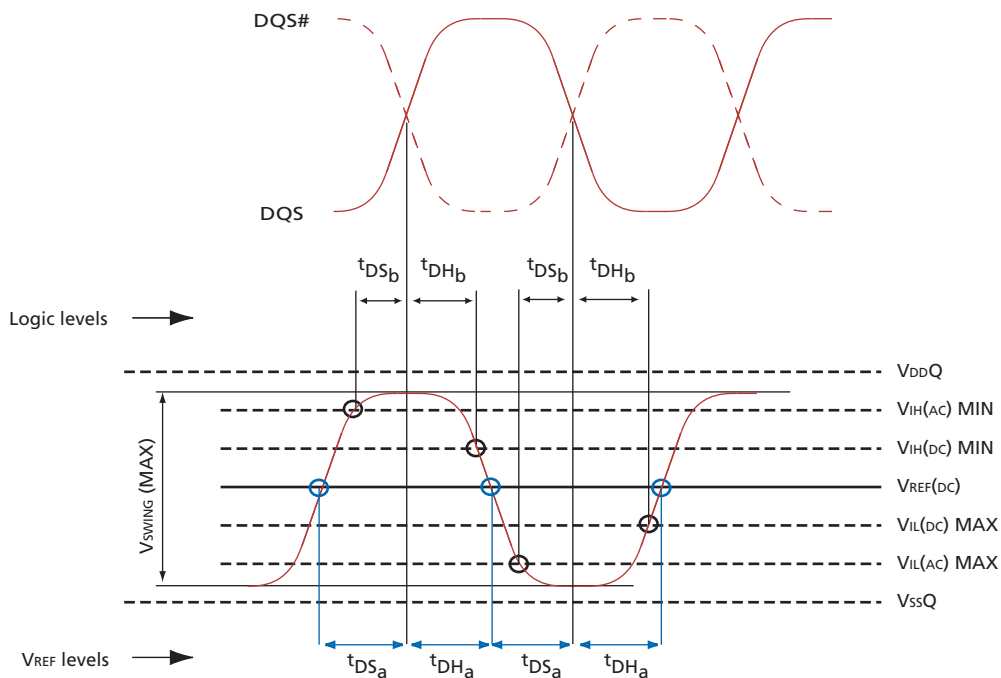


# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Input Slew Rate Derating

**Figure 73: AC Input Test Signal Waveform Command/Address Balls**



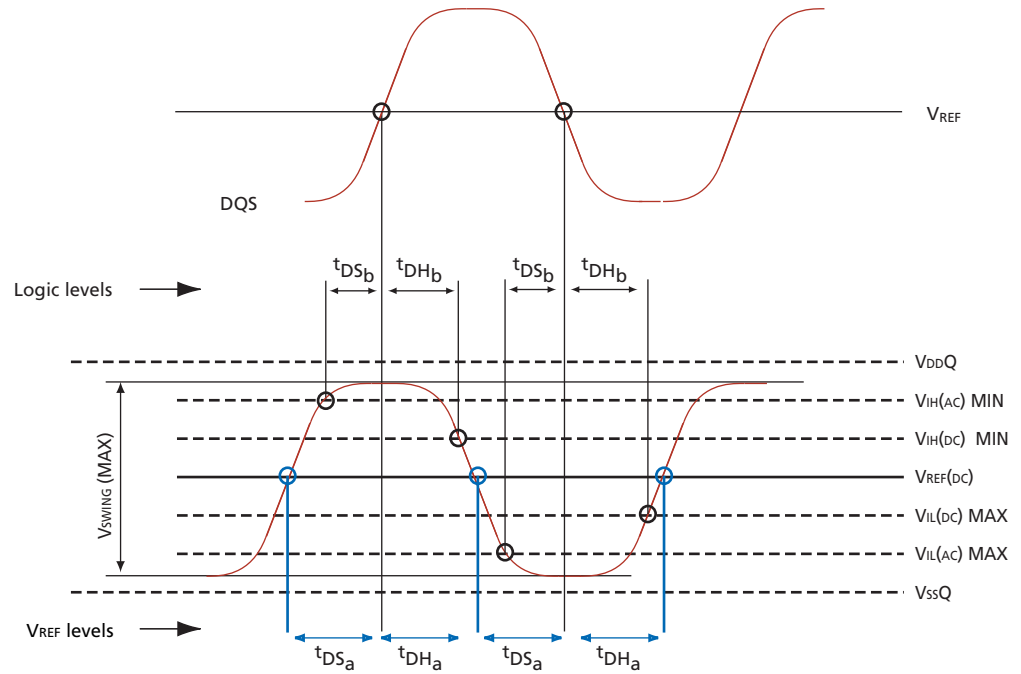
**Figure 74: AC Input Test Signal Waveform for Data with DQS, DQS# (Differential)**



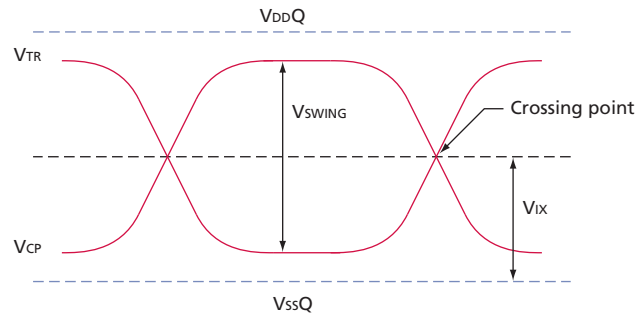


**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
Input Slew Rate Derating**

**Figure 75: AC Input Test Signal Waveform for Data with DQS (Single-Ended)**



**Figure 76: AC Input Test Signal Waveform (Differential)**







## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Power and Ground Clamp Characteristics

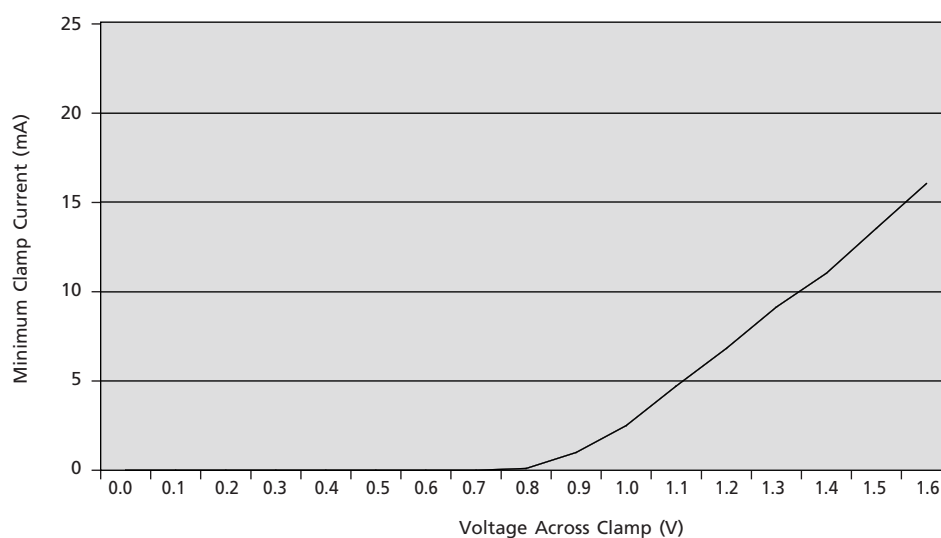
### Power and Ground Clamp Characteristics

Power and ground clamps are provided on the following input-only balls: Bank address pins, address pins, CS#, RAS#, CAS#, WE#, ODT, and CKE.

**Table 29: Input Clamp Characteristics**

Voltage Across Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0

**Figure 77: Input Clamp Characteristics**





**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
AC Overshoot/Undershoot Specification**

**AC Overshoot/Undershoot Specification**

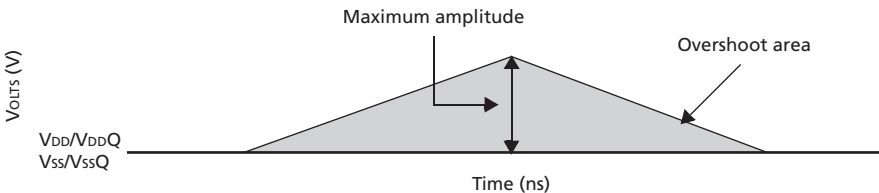
**Table 30: Address and Control Balls**  
Applies to bank address pins, address pins, CS#, RAS#, CAS#, WE#, CKE, ODT

Parameter	Specification				
	-5E	-37E	-3/-3E	-25/-25E	-187E
Maximum peak amplitude permitted for overshoot area (see Figure 78)	0.45V	0.45V	0.45V	0.45V	0.45V
Maximum peak amplitude permitted for undershoot area (see Figure 79)	0.45V	0.45V	0.45V	0.45V	0.45V
Maximum overshoot area above V <sub>DD</sub> (see Figure 78)	1.33 Vns	1.00 Vns	0.80 Vns	0.66 Vns	0.5 Vns
Maximum undershoot area below V <sub>SS</sub> (see Figure 79)	1.33 Vns	1.00 Vns	0.80 Vns	0.66 Vns	0.5 Vns

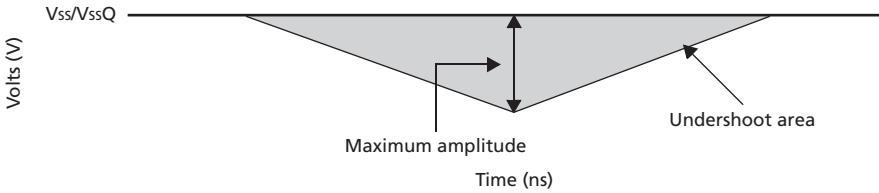
**Table 31: Clock, Data, Strobe, and Mask Balls**  
Applies to DQ, DQS, DQS#, RDQS, RDQS#, UDQS, UDQS#, LDQS, LDQS#, DM, UDM, LDM

Parameter	Specification				
	-5E	-37E	-3/-3E	-25/-25E	-187E
Maximum peak amplitude permitted for overshoot area (see Figure 78)	0.45V	0.45V	0.45V	0.45V	0.45V
Maximum peak amplitude permitted for undershoot area (see Figure 79)	0.45V	0.45V	0.45V	0.45V	0.45V
Maximum overshoot area above V <sub>DDQ</sub> (see Figure 78)	0.38 Vns	0.28 Vns	0.23 Vns	0.23 Vns	0.19 Vns
Maximum undershoot area below V <sub>SSQ</sub> (see Figure 79)	0.38 Vns	0.28 Vns	0.23 Vns	0.23 Vns	0.19 Vns

**Figure 78: Overshoot**



**Figure 79: Undershoot**



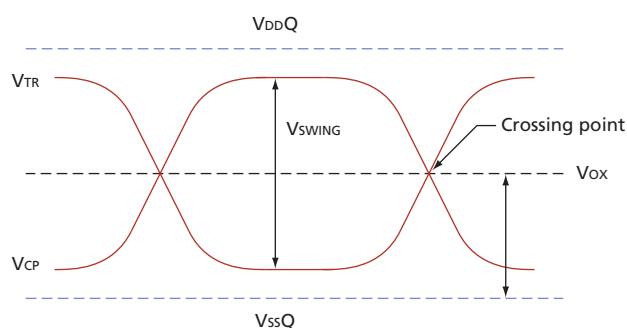


## Output Electrical Characteristics and Operating Conditions

**Table 32: Differential AC Output Parameters**

Parameter	Symbol	Min	Max	Units	Notes
AC differential cross-point voltage	$V_{OX(AC)}$	$0.50 \times V_{DDQ} - 105$	$0.50 \times V_{DDQ} + 105$	mV	1
AC differential voltage swing	$V_{SWING}$	1.0		mV	

Notes: 1. The typical value of  $V_{OX(AC)}$  is expected to be about  $0.5 \times V_{DDQ}$  of the transmitting device and  $V_{OX(AC)}$  is expected to track variations in  $V_{DDQ}$ .  $V_{OX(AC)}$  indicates the voltage at which differential output signals must cross.

**Figure 80: Differential Output Signal Levels**




## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Output Electrical Characteristics and Operating Conditions

**Table 33: Output DC Current Drive**

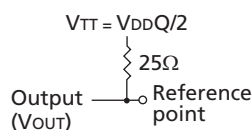
Parameter	Symbol	Value	Units	Notes
Output MIN source DC current	I <sub>OH</sub>	-13.4	mA	1, 2, 4
Output MIN sink DC current	I <sub>OL</sub>	13.4	mA	2, 3, 4

- Notes:
- For I<sub>OH</sub>(DC); V<sub>DDQ</sub> = 1.425V, V<sub>OUT</sub> = 1.145V. (V<sub>OUT</sub> - V<sub>DDQ</sub>)/I<sub>OH</sub> must be less than 21Ω for values of V<sub>OUT</sub> between V<sub>DDQ</sub> and V<sub>DDQ</sub> - 280mV.
  - For I<sub>OL</sub>(DC); V<sub>DDQ</sub> = 1.425V, V<sub>OUT</sub> = 280mV. V<sub>OUT</sub>/I<sub>OL</sub> must be less than 21Ω for values of V<sub>OUT</sub> between 0V and 280mV.
  - The DC value of V<sub>REF</sub> applied to the receiving device is set to V<sub>TT</sub>.
  - The values of I<sub>OH</sub>(DC) and I<sub>OL</sub>(DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V<sub>IH</sub> (MIN) plus a noise margin and V<sub>IL</sub> (MAX) minus a noise margin are delivered to an SSTL\_18 receiver. The actual current values are derived by shifting the desired driver operating point (see output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

**Table 34: Output Characteristics**

Parameter	Min	Nom	Max	Units	Notes
Output impedance	See "Full Strength Pull-Down Driver Characteristics" on page 101			Ω	1, 2
Pull-up and pull-down mismatch	0		4	Ω	1, 2, 3
Output slew rate	0.8		5	V/ns	1, 4, 5

- Notes:
- Absolute specifications: 0°C ≤ T<sub>C</sub> ≤ +95°C; V<sub>DDQ</sub> = +1.525V ±0.1V, V<sub>DD</sub> = +1.525V ±0.1V.
  - Impedance measurement conditions for output source DC current: V<sub>DDQ</sub> = 1.425V; V<sub>OUT</sub> = 1.145V; (V<sub>OUT</sub> - V<sub>DDQ</sub>)/I<sub>OH</sub> must be less than 23.4Ω for values of V<sub>OUT</sub> between V<sub>DDQ</sub> and V<sub>DDQ</sub> - 280mV. Impedance measurement condition for output sink DC current: V<sub>DDQ</sub> = 1.425V; V<sub>OUT</sub> = 280mV; V<sub>OUT</sub>/I<sub>OL</sub> must be less than 23.4Ω for values of V<sub>OUT</sub> between 0V and 280mV.
  - Mismatch is absolute value between pull-up and pull-down; both are measured at the same temperature and voltage.
  - Output slew rate for falling and rising edges is measured between V<sub>TT</sub> - 250mV and V<sub>TT</sub> + 250mV for single-ended signals. For differential signals (DQS, DQS#), output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
  - The absolute value of the slew rate as measured from V<sub>IL</sub>(DC) MAX to V<sub>IH</sub>(DC) MIN is equal to or greater than the slew rate as measured from V<sub>IL</sub>(AC) MAX to V<sub>IH</sub>(AC) MIN. This is guaranteed by design and characterization.

**Figure 81: Output Slew Rate Load**




## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Full Strength Pull-Down Driver Characteristics

### Full Strength Pull-Down Driver Characteristics

Figure 82: Full Strength Pull-Down Characteristics

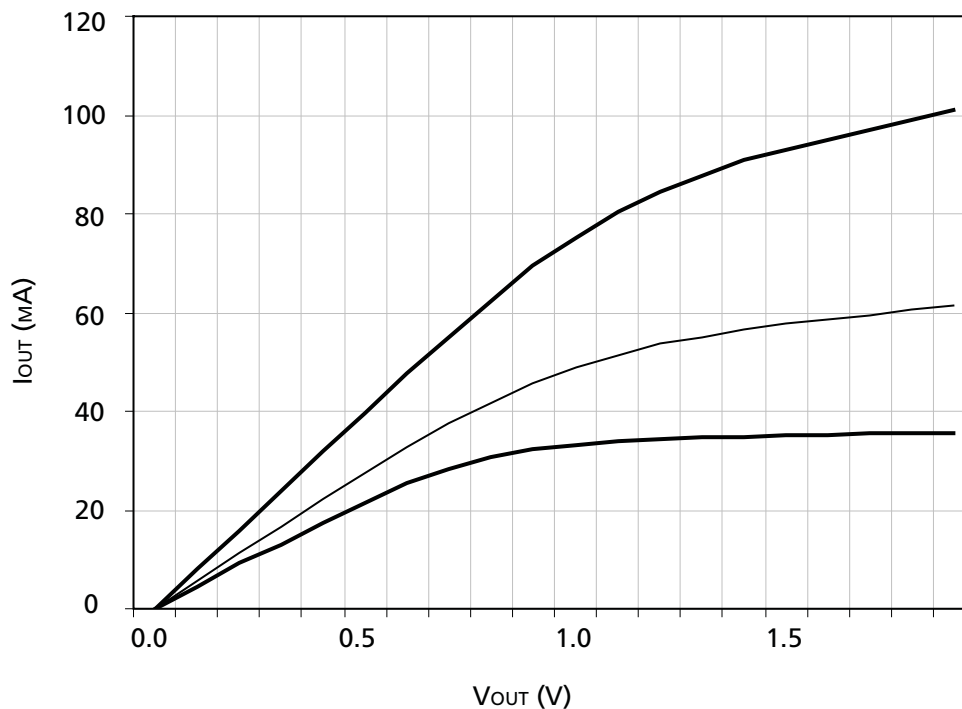


Table 35: Full Strength Pull-Down Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.0	0.00	0.00
0.1	3.9	5.63	7.95
0.2	7.7	11.3	15.90
0.3	11.6	16.52	23.85
0.4	15.2	22.19	31.80
0.5	18.4	27.59	39.75
0.6	21.0	32.39	47.70
0.7	22.9	36.45	55.55
0.8	24.1	40.38	62.95
0.9	24.9	44.01	69.55
1.0	25.5	47.01	75.35
1.1	26.1	49.63	80.35
1.2	26.5	51.71	84.55
1.3	26.9	53.32	87.95
1.4	27.3	54.9	90.70
1.5	27.6	56.03	93.00
1.6	27.9	57.07	95.05



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Full Strength Pull-Up Driver Characteristics

### Full Strength Pull-Up Driver Characteristics

Figure 83: Full Strength Pull-Up Characteristics

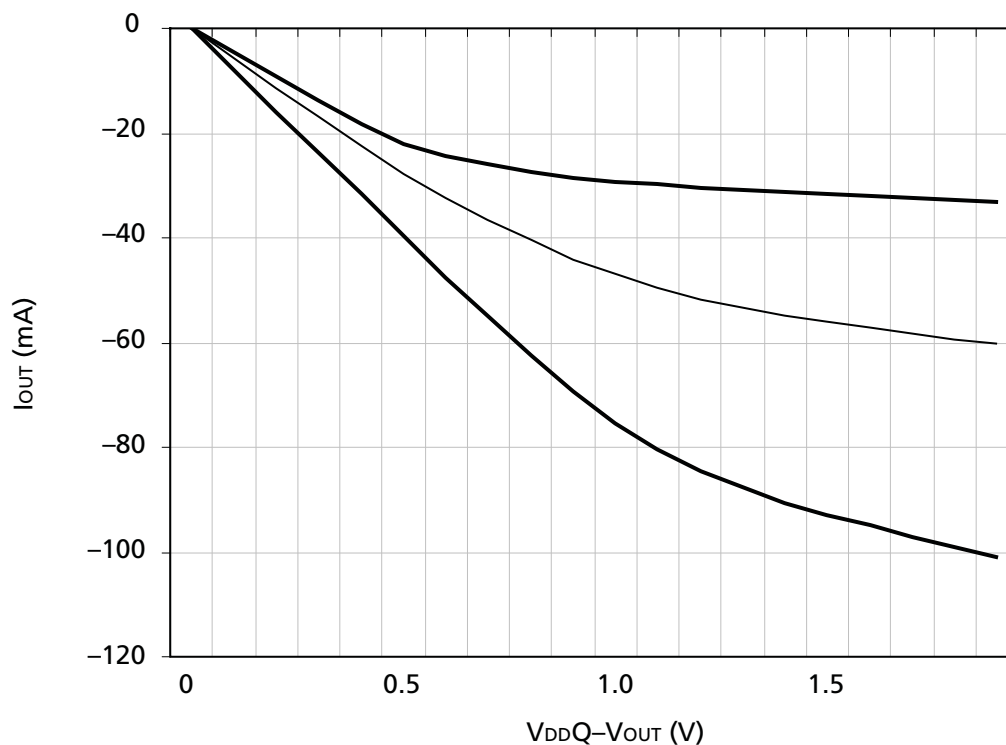


Table 36: Full Strength Pull-Up Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.0	0.00	0.00
0.1	-3.9	-5.63	-7.95
0.2	-7.7	-11.3	-15.90
0.3	-11.6	-16.52	-23.85
0.4	-15.2	-22.19	-31.80
0.5	-18.4	-27.59	-39.75
0.6	-21.0	-32.39	-47.70
0.7	-22.9	-36.45	-55.55
0.8	-24.1	-40.38	-62.95
0.9	-24.9	-44.01	-69.55
1.0	-25.5	-47.01	-75.35
1.1	-26.1	-49.63	-80.35
1.2	-26.5	-51.71	-84.55
1.3	-26.9	-53.32	-87.95
1.4	-27.3	-54.90	-90.70
1.5	-27.6	-56.03	-93.00
1.6	-27.9	-57.07	-95.05



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Reduced Strength Pull-Down Driver Characteristics

### Reduced Strength Pull-Down Driver Characteristics

Figure 84: Reduced Strength Pull-Down Characteristics

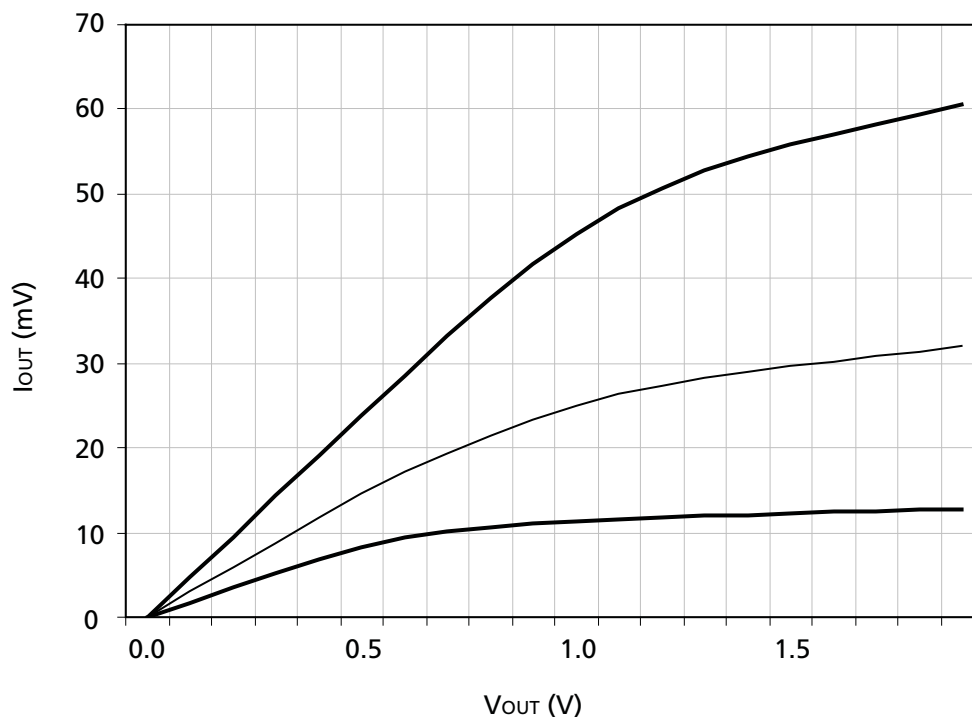


Table 37: Reduced Strength Pull-Down Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.0	0.00	0.00
0.1	1.5	2.98	4.77
0.2	3.1	5.99	9.54
0.3	4.6	8.75	14.31
0.4	6.1	11.76	19.08
0.5	7.3	14.62	23.85
0.6	8.4	17.17	28.62
0.7	9.2	19.32	33.33
0.8	9.6	21.40	37.77
0.9	10.0	23.32	41.73
1.0	10.2	24.92	45.21
1.1	10.4	26.30	48.21
1.2	10.6	27.41	50.73
1.3	10.8	28.26	52.77
1.4	10.9	29.10	54.42
1.5	11.0	29.70	55.80
1.6	11.2	30.25	57.03



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Reduced Strength Pull-Up Driver Characteristics

### Reduced Strength Pull-Up Driver Characteristics

Figure 85: Reduced Strength Pull-Up Characteristics

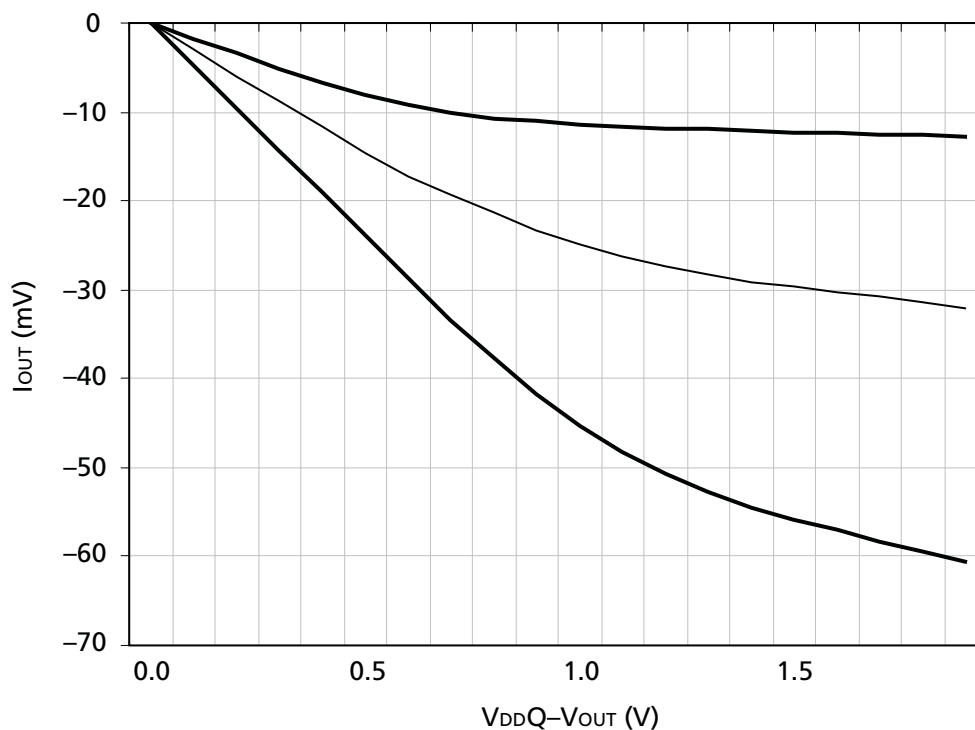


Table 38: Reduced Strength Pull-Up Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.0	0.00	0.00
0.1	-1.5	-2.98	-4.77
0.2	-3.1	-5.99	-9.54
0.3	-4.6	-8.75	-14.31
0.4	-6.1	-11.76	-19.08
0.5	-7.3	-14.62	-23.85
0.6	-8.4	-17.17	-28.62
0.7	-9.2	-19.32	-33.33
0.8	-9.6	-21.40	-37.77
0.9	-10.0	-23.32	-41.73
1.0	-10.2	-24.92	-45.21
1.1	-10.4	-26.30	-48.21
1.2	-10.6	-27.41	-50.73
1.3	-10.8	-28.26	-52.77
1.4	-10.9	-29.10	-54.42
1.5	-11.0	-29.69	-55.8
1.6	-11.2	-30.25	-57.03





## FBGA Package Capacitance

**Table 39: Input Capacitance**

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	CCK	1.0	2.0	pF	1
Delta input capacitance: CK, CK#	CDCK	–	0.25	pF	2, 6
Input capacitance: Bank address pins, address pins, CS#, RAS#, CAS#, WE#, CKE, ODT	CI	1.0	2.0	pF	1, 5
Delta input capacitance: Bank address pins, address pins, CS#, RAS#, CAS#, WE#, CKE, ODT	CDI	–	0.25	pF	2, 6
Input/output capacitance: DQ, DQS, DM, NF	CIO	2.5	4.0	pF	1, 4
Delta input/output capacitance: DQ, DQS, DM, NF	CDIO	–	0.5	pF	3, 6

- Notes:
1. This parameter is sampled.  $V_{DD} = V_{DDQ} = +1.425V$  to  $+1.625V$ ,  $V_{REF} = V_{SS}$ ,  $f = 100$  MHz,  $T_C = 25^\circ C$ ,  $V_{OUT(DC)} = V_{DDQ}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
  2. The input capacitance per ball group will not differ by more than this maximum amount for any given device.
  3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
  4. Reduce MAX limit by 0.5pF for -3, -3E, -25, -25E, -187E speed devices.
  5. Reduce MAX limit by 0.25pF for -25, -25E, -187E speed devices.
  6.  $\Delta C$  are not pass/fail parameters but rather targets.

**Table 40: Input Capacitance**

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	CCK	1.0	2.0	pF	1
Input capacitance: Bank address pins, address pins, CS#, RAS#, CAS#, WE#, CKE, ODT	CI	1.0	2.0	pF	1
Input/Output capacitance: DQs, DQS, DM, NF	CIO	2.5	4.0	pF	1, 2

- Notes:
1. This parameter is sampled.  $V_{DD} = V_{DDQ} = +1.425V$  to  $+1.625V$ ,  $V_{REF} = V_{SS}$ ,  $f = 100$  MHz,  $T_C = 25^\circ C$ ,  $V_{OUT(DC)} = V_{DDQ}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
  2. Reduce MAX limit by 0.5pF for -3, -3E, -25, -25E speed devices.
  3. Reduce MAX limit by 0.25pF for -3, -3E, -25, -25E speed devices.


**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
FBGA Package Capacitance**
**Table 41: 1.5V DDR2 IDD Specifications and Conditions (Die Revision E)**

Notes: 1–7 apply to the entire table; Notes appear on page 107

Parameter/Condition	Symbol	Configuration	-187E	-25E/ -25	-3E/ -3	-37E	-5E	Units
<b>Operating one bank active-precharge current:</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	x4, x8	95	75	70	60	60	mA
		x16	155	130	115	95	95	
<b>Operating one bank active-read-precharge current:</b> $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	x4, x8	110	95	85	80	75	mA
		x16	180	150	110	100	100	
<b>Precharge power-down current:</b> All banks idle; $t_{CK} = t_{CK} (IDD)$ ; CE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	x4, x8, x16	6	6	6	6	6	mA
<b>Precharge quiet standby current:</b> All banks idle; $t_{CK} = t_{CK} (IDD)$ ; CE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	x4, x8	50	45	35	35	30	mA
		x16	75	65	55	40	35	
<b>Precharge standby current:</b> All banks idle; $t_{CK} = t_{CK} (IDD)$ ; CE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	x4, x8	50	45	35	35	30	mA
		x16	80	70	60	45	35	
<b>Active power-down current:</b> All banks open; $t_{CK} = t_{CK} (IDD)$ ; CE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD3P	Fast exit MR12 = 0	40	35	25	25	25	mA
		Slow exit MR12 = 1	9	9	9	9	9	
<b>Active standby current:</b> All banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	x4, x8	60	50	45	40	35	mA
		x16	80	70	65	50	45	
<b>Operating burst write current:</b> All banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	x4	160	125	100	95	75	mA
		x8	180	135	115	105	90	
		x16	345	270	170	155	135	
<b>Operating burst read current:</b> All banks open, continuous burst reads, $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	x4	160	125	100	105	90	mA
		x8	180	135	115	95	75	
		x16	355	270	185	155	135	
<b>Burst refresh current:</b> $t_{CK} = t_{CK} (IDD)$ ; refresh command at every $t_{RFC} (IDD)$ interval; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	x4, x8	225	200	185	180	175	mA
		x16	255	240	230	215	205	



## 1Gb: x4, x8, x16 1.5V DDR2 SDRAM FBGA Package Capacitance

**Table 41: 1.5V DDR2 IDD Specifications and Conditions (Die Revision E) (continued)**

Notes: 1–7 apply to the entire table; Notes appear on page 107

Parameter/Condition	Symbol	Configuration	-187E	-25E/ -25	-3E/ -3	-37E	-5E	Units
<b>Self refresh current:</b> CK and CK# at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	x4, x8, x16	6	6	6	6	6	mA
<b>Operating bank interleave read current:</b> All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = $t_{RCD}$ (IDD) - 1 x $t_{CK}$ (IDD); $t_{CK} = t_{CK}$ (IDD), $t_{RC} = t_{RC}$ (IDD), $t_{RRD} = t_{RRD}$ (IDD), $t_{RCD} = t_{RCD}$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See "Idd7 Conditions" on page 108 for details	IDD7	x4, x8	360	285	240	230	220	mA
		x16	440	375	300	280	255	

- Notes:
- IDD specifications are tested after the device is properly initialized.  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ .  $V_{DD} = V_{DDQ} = V_{DDL} = +1.425$  to  $1.625\text{V}$ ,  $V_{REF} = V_{DDQ}/2$ .
  - Input slew rate is specified by AC parametric test conditions (Table 42 on page 108).
  - IDD parameters are specified with ODT disabled.
  - Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. IDD values must be met with all combinations of EMR bits 10 and 11.
  - Definitions for IDD conditions:
    - LOW**  $V_{IN} \leq V_{IL(AC)} \text{ MAX}$
    - HIGH**  $V_{IN} \geq V_{IH(AC)} \text{ MIN}$
    - Stable** Inputs stable at a HIGH or LOW level
    - Floating** Inputs at  $V_{REF} = V_{DDQ}/2$
    - Switching** Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
    - Switching** Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes
  - IDD1, IDD4R, and IDD7 require A12 in EMR1 to be enabled during testing.
  - The following Idds must be derated (IDD limits increase) when operated in the range  $85^{\circ}\text{C} \leq T_C \leq 95^{\circ}\text{C}$ :
    - When  $T_C \geq 85^{\circ}\text{C}$**  IDD0, IDD1, IDD2N, IDD2Q, IDD3N, IDD3P (fast), IDD4R, IDD4W, and IDD5W must be derated by 2 percent; IDD2P must be derated by 20 percent; IDD3Pslow must be derated by 30 percent; and IDD6 must be derated by 80 percent (IDD6 will increase by this amount if  $T_C < 85^{\circ}\text{C}$  and the 2X refresh option is still enabled)


**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
IDD7 Conditions**
**Table 42: General IDD Parameters**

IDD Parameters	-187E	-25E	-25	-3E	-3	-37E	-5E	Units
CL (IDD)	7	5	6	4	5	4	3	<sup>t</sup> CK
<sup>t</sup> RCD (IDD)	13.125	12.5	15	12	15	15	15	ns
<sup>t</sup> RC (IDD)	58.125	57.5	60	57	60	60	55	ns
<sup>t</sup> RRD (IDD) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns
<sup>t</sup> RRD (IDD) - x16 (2KB)	10	10	10	10	10	10	10	ns
<sup>t</sup> CK (IDD)	1.875	2.5	2.5	3	3	3.75	5	ns
<sup>t</sup> RAS MIN (IDD)	45	45	45	45	45	45	40	ns
<sup>t</sup> RAS MAX (IDD)	70,000	70,000	70,000	70,000	70,000	70,000	70,000	ns
<sup>t</sup> RP (IDD)	13.125	12.5	15	12	15	15	15	ns
<sup>t</sup> RFC (IDD - 256Mb)	75	75	75	75	75	75	75	ns
<sup>t</sup> RFC (IDD - 512Mb)	105	105	105	105	105	105	105	ns
<sup>t</sup> RFC (IDD - 1Gb)	127.5	127.5	127.5	127.5	127.5	127.5	127.5	ns
<sup>t</sup> RFC (IDD - 2Gb)	195	195	195	195	195	195	195	ns
<sup>t</sup> FAW (IDD) - x4/x8 (1KB)	35	75	75	75	75	75	75	ns
<sup>t</sup> FAW (IDD) - x16 (2KB)	45	45	45	50	50	50	50	ns

## IDD7 Conditions

The detailed timings are shown below for IDD7. Where general IDD parameters in Table 42 on page 108 conflict with pattern requirements of Table 43, then Table 43 requirements take precedence.

**Table 43: IDD7 Timing Patterns (8-Bank Interleave READ Operation)**

Speed Grade	IDD7 Timing Patterns
Timing patterns for 8-bank devices x4/x8	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 A4 RA4 A5 RA5 A6 RA6 A7 RA7
-37E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D
-3	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D
-3E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D
-25	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-25E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-175E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
Timing patterns for 8-bank devices x16	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-3	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D
-3E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D
-25	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
-175E	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D

- Notes:
1. A = active; RA = read auto precharge; D = deselect.
  2. All banks are being interleaved at <sup>t</sup>RC (IDD) without violating <sup>t</sup>RRD (IDD) using a BL = 4.
  3. Control and address bus inputs are STABLE during DESELECTs.

## AC Operating Specifications

**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 1 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;  
 Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics				-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Clock cycle time	CL = 7	$t_{CK}^{(AVG)}$	1.875	8.0	–	–	–	–	–	–	–	–	–	–	–	–	–	ns	16, 22, 36, 38	
	CL = 6	$t_{CK}^{(AVG)}$	2.5	8.0	–	–	2.5	8.0	–	–	–	–	–	–	–	–	–			
	CL = 5	$t_{CK}^{(AVG)}$	3.0	8.0	2.5	8.0	3.0	8.0	3.0	8.0	3.0	8.0	–	–	–	–	–			
	CL = 4	$t_{CK}^{(AVG)}$	–	–	3.75	8.0	3.75	8.0	3.0	8.0	3.75	8.0	3.75	8.0	5.0	8.0	–			–
	CL = 3	$t_{CK}^{(AVG)}$	–	–	–	–	–	–	–	–	5.0	8.0	5.0	8.0	5.0	8.0	–			–
Clock	CK high-level width	$t_{CH}^{(AVG)}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	$t_{CK}$	45
	CK low-level width	$t_{CL}^{(AVG)}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	$t_{CK}$	
	Half clock period	$t_{HP}$	MIN = lessor of $t_{CH}$ and $t_{CL}$ MAX = n/a														ps	46		
	Absolute $t_{CK}$	$t_{CK}^{(ABS)}$	MIN = $t_{CK}^{(AVG)} \text{ MIN} + t_{JITPER}^{(MIN)}$ MAX = $t_{CK}^{(AVG)} \text{ MAX} + t_{JITPER}^{(MAX)}$														ps			
	Absolute CK high-level width	$t_{CH}^{(ABS)}$	MIN = $t_{CK}^{(AVG)} \text{ MIN} \times t_{CH}^{(AVG)} \text{ MIN} + t_{JITDTY}^{(MIN)}$ MAX = $t_{CK}^{(AVG)} \text{ MAX} \times t_{CH}^{(AVG)} \text{ MAX} + t_{JITDTY}^{(MAX)}$														ps			
	Absolute CK low-level width	$t_{CL}^{(ABS)}$	MIN = $t_{CK}^{(AVG)} \text{ MIN} \times t_{CL}^{(AVG)} \text{ MIN} + t_{JITDTY}^{(MIN)}$ MAX = $t_{CK}^{(AVG)} \text{ MAX} \times t_{CL}^{(AVG)} \text{ MAX} + t_{JITDTY}^{(MAX)}$														ps			

**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 2 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;

Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics		-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Clock Jitter	Period jitter	$t_{JITPER}$	-90	90	-100	100	-100	100	-125	125	-125	125	-125	125	-125	125	ps	39
	Half period	$t_{JITDTY}$	-75	75	-100	100	-100	100	-125	125	-125	125	-125	125	-150	150	ps	40
	Cycle to cycle	$t_{JITCC}$	180		200		200		250		250		250		250		ps	41
	Cumulative error, 2 cycles	$t_{ERR_{2PER}}$	-132	132	-150	150	-150	150	-175	175	-175	175	-175	175	-175	175	ps	42
	Cumulative error, 3 cycles	$t_{ERR_{3PER}}$	-157	157	-175	175	-175	175	-225	225	-225	225	-225	225	-225	225	ps	42
	Cumulative error, 4 cycles	$t_{ERR_{4PER}}$	-175	175	-200	200	-200	200	-250	250	-250	250	-250	250	-250	250	ps	42
	Cumulative error, 5 cycles	$t_{ERR_{5PER}}$	-188	188	-200	200	-200	200	-250	250	-250	250	-250	250	-250	250	ps	42, 48
	Cumulative error, 6–10 cycles	$t_{ERR_{6-10PER}}$	-250	250	-300	300	-300	300	-350	350	-350	350	-350	350	-350	350	ps	42, 48
	Cumulative error, 11–50 cycles	$t_{ERR_{11-50PER}}$	-425	425	-450	450	-450	450	-450	450	-450	450	-450	450	-450	450	ps	42
Data Strobe-Out	DQS output access time from CK/CK#	$t_{DQSCK}$	-400	+400	-450	+450	-450	+450	-500	+500	-500	+500	-550	+550	-600	+600	ps	40
	DQS read preamble	$t_{RPRE}$	MIN = $0.9 \times t_{CK} - 100ps$ MAX = $1.1 \times t_{CK} + 100ps$													$t_{CK}$	33, 37, 43	
	DQS read postamble	$t_{RPST}$	MIN = $0.4 \times t_{CK} - 100ps$ MAX = $0.6 \times t_{CK} + 100ps$													$t_{CK}$	33, 34, 37, 43	
	CK/CK# to DQS low-impedance	$t_{LZ1}$	MIN = $t_{AC} (MIN)$ MAX = $t_{AC} (MAX)$													ps	8, 10, 43	

**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 3 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;

Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics		-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe-In	Positive DQS edge to associated clock edge	$t_{DQSS}$	MIN = $-0.25 \times t_{CK}$ MAX = $+0.25 \times t_{CK}$								$t_{CK}$	37					
	DQS input-high pulse width	$t_{DQSH}$	MIN = $0.35 \times t_{CK}$ MAX = n/a								$t_{CK}$	37					
	DQS input-low pulse width	$t_{DQSL}$	MIN = $0.35 \times t_{CK}$ MAX = n/a								$t_{CK}$	37					
	DQS falling to CK rising: setup time	$t_{DSS}$	MIN = $0.2 \times t_{CK}$ MAX = n/a								$t_{CK}$	37					
	DQS falling from CK rising: hold time	$t_{DSH}$	MIN = $0.2 \times t_{CK}$ MAX = n/a								$t_{CK}$	37					
	Write preamble setup time	$t_{WPRES}$	MIN = 0 MAX = n/a								ps	12, 13					
	DQS write preamble	$t_{WPRE}$	MIN = $0.35 \times t_{CK}$ MAX = n/a								$t_{CK}$	37					
	DQS write postamble	$t_{WPST}$	MIN = $0.4 \times t_{CK}$ MAX = $0.6 \times t_{CK}$								$t_{CK}$	11, 37					
	WRITE command to first DQS transition	–	MIN = WL - $t_{DQSS}$ MAX = WL + $t_{DQSS}$								$t_{CK}$						

**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 4 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;

Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics		-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Data-Out	DQ output access time from CK/CK#	$t_{AC}$	-450	+450	-500	+500	-500	+500	-550	+550	-550	+550	-600	+600	-700	+700	ps	43
	DQS–DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$	–	325	–	350	–	350	–	390	–	390	–	450	–	500	ps	15, 17
	DQ hold from next DQS strobe	$t_{QHS}$	–	350	–	400	–	400	–	440	–	440	–	500	–	550	ps	47
	DQ–DQS hold, DQS to first DQ not valid	$t_{QH}$	MIN = $t_{HP} - t_{QHS}$ MAX = n/a														ps	15, 17, 47
	CK/CK# to DQ, DQS high-impedance	$t_{HZ}$	MIN = n/a MAX = $t_{AC}$ (MAX)														ps	8, 9, 43
	CK/CK# to DQ low-impedance	$t_{LZ_2}$	MIN = $2 \times t_{AC}$ (MIN) MAX = $t_{AC}$ (MAX)														ps	8, 10, 43
	DQ and DM input setup time relative to DQS	$t_{DS}$	150		150		150		150		150		100		150		ps	7, 15, 19
	DQ and DM input hold time relative to DQS	$t_{DH}$	275		275		275		275		275		225		275		ps	7, 15, 19
	Data valid output window	DVW	MIN = $t_{QH} - t_{DQSQ}$ MAX = n/a														ns	15, 17
Data-In	DQ and DM input setup time to DQS	$t_{DS_b}$	0	–	50	–	50	–	100	–	100	–	100	–	150	–	ps	7, 15, 19
	DQ and DM input hold time to DQS	$t_{DH_b}$	75	–	125	–	125	–	175	–	175	–	225	–	275	–	ps	7, 15, 19
	DQ and DM input setup time to DQS	$t_{DS_a}$	200	–	250	–	250	–	300	–	300	–	350	–	400	–	ps	7, 15, 19
	DQ and DM input hold time to DQS	$t_{DH_a}$	200	–	250	–	250	–	300	–	300	–	350	–	400	–	ps	7, 15, 19
	DQ and DM input pulse width	$t_{DIPW}$	MIN = $0.35 \times t_{CK}$ MAX = n/a														$t_{CK}$	30, 37



**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 5 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;

Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics		-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Command and Address	Input setup time	$t_{IS_b}$	125	–	175	–	175	–	200	–	200	–	250	–	350	–	ps	6, 19	
	Input hold time	$t_{IH_b}$	200	–	250	–	250	–	275	–	275	–	375	–	475	–	ps	6, 19	
	Input setup time	$t_{IS_a}$	325	–	375	–	375	–	400	–	400	–	500	–	600	–	ps	6, 19	
	Input hold time	$t_{IH_a}$	325	–	375	–	375	–	400	–	400	–	500	–	600	–	ps	6, 19	
	Input pulse width	$t_{IPW}$	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	$t_{CK}$	30, 37	
	ACTIVE-to-ACTIVE delay, same bank	$t_{RC}$	54	–	55	–	55	–	54	–	55	–	55	–	55	–	ns	31, 37	
	ACTIVE-to READ or WRITE delay	$t_{RCD}$	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15	–	ns	37	
	ACTIVE-to-PRECHARGE delay	$t_{RAS}$	40	70K	45	70K	45	70K	40	70K	40	70K	40	70K	40	70K	ns	18, 31, 37	
	PRECHARGE period	$t_{RP}$	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15	–	ns	29, 37	
	PRECHARGE ALL period	<1Gb	$t_{RPA}$	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15	–	ns	29, 37
		$\geq$ 1Gb	$t_{RPA}$	15	–	15	–	17.5	–	15	–	18	–	18.75	–	20	–	ns	29, 37
	ACTIVE-to-ACTIVE delay different bank	x4, x8	$t_{RRD}$	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	ns	25, 37
		x16	$t_{RRD}$	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns	25, 37
	4-bank activate period	x4, x8	$t_{FAW}$	35	–	35	–	35	–	37.5	–	37.5	–	37.5	–	37.5	–	ns	28, 37
		x16	$t_{FAW}$	45	–	45	–	45	–	50	–	50	–	50	–	50	–	ns	28, 37
	Internal READ to PRECHARGE delay	$t_{RTP}$	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	ns	21, 25, 37	
	CAS#-to-CAS# delay	$t_{CCD}$	2	–	2	–	2	–	2	–	2	–	2	–	2	–	$t_{CK}$	37	
Write recovery time	$t_{WR}$	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns	25, 37		
Write AP recovery + precharge time	$t_{DAL}$	$t_{WR} + t_{RP}$	–	$t_{WR} + t_{RP}$	–	$t_{WR} + t_{RP}$	–	$t_{WR} + t_{RP}$	–	$t_{WR} + t_{RP}$	–	$t_{WR} + t_{RP}$	–	$t_{WR} + t_{RP}$	–	ns	20		
Internal WRITE-to-READ delay	$t_{WTR}$	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	10	–	ns	25, 37		
LOAD MODE cycle time	$t_{MRD}$	2	–	2	–	2	–	2	–	2	–	2	–	2	–	$t_{CK}$	37		

**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 6 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;

Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes	
Parameter	Symbol		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Refresh	REFRESH-to-ACTIVE or to-REFRESH interval	256Mb	$t_{RFC}$	75	70K	75	70K	75	70K	75	70K	75	70K	75	70K	75	70K	ns	14, 37
		512Mb		105	70K	105	70K	105	70K	105	70K	105	70K	105	70K	105	70K		
		1Gb		127.5	70K	127.5	70K	127.5	70K	127.5	70K	127.5	70K	127.5	70K	127.5	70K		
		2Gb		197.5	70K	197.5	70K	197.5	70K	197.5	70K	197.5	70K	197.5	70K	197.5	70K		
Refresh	Average periodic refresh (commercial)	$t_{REFI}$	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	$\mu$ s	14, 37	
	Average periodic refresh (industrial)	$t_{REFI_T}$	-	3.9	-	3.9	-	3.9	-	3.9	-	3.9	-	3.9	-	3.9	$\mu$ s	14, 37	
	CKE LOW to CK, CK# uncertainty	$t_{DELAY}$	MIN limit = $t_{IS} + t_{CK} + t_{IH}$ MAX limit = n/a														ns	26	
Self Refresh	Exit SELF REFRESH to nonREAD command	$t_{XSNR}$	MIN limit = $t_{RFC}(\text{MIN}) + 10$ MAX limit = n/a														ns		
	Exit SELF REFRESH to READ command	$t_{XSRD}$	MIN limit = 200 MAX limit = n/a														$t_{CK}$	37	
	Exit SELF REFRESH timing reference	$t_{ISXR}$	MIN limit = $t_{IS}$ MAX limit = n/a														ps	6, 27	
Power-Down	Exit active power-down to READ command	MR12 = 0	$t_{XARD}$	3	-	2	-	2	-	2	-	2	-	2	-	2	-	$t_{CK}$	37
		MR12 = 1		10 - AL	-	8 - AL	-	8 - AL	-	7 - AL	-	7 - AL	-	6 - AL	-	6 - AL	-	$t_{CK}$	37
	Exit precharge power-down to any non READ command	$t_{XP}$	3	-	2	-	2	-	2	-	2	-	2	-	2	-	$t_{CK}$	37	
	CKE MIN HIGH/LOW time	$t_{CKE}$	MIN = 3 MAX = n/a														$t_{CK}$	32, 37	

**Table 44: AC Operating Conditions for -187E, -25E, -3E, -3, -37E, and -5E Speeds (Sheet 7 of 7)**

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported;

Notes: 1–5 apply to the entire table; Notes appear on page 116; VDD = VDDQ = +1.425V to +1.625V

AC Characteristics		-187E		-25E		-25		-3E		-3		-37E		-5E		Units	Notes	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
ODT	ODT to power-down entry latency	$t_{ANPD}$	4	–	3	–	3	–	3	–	3	–	3	–	3	–	$t_{CK}$	37
	ODT power-down exit latency	$t_{AXPD}$	11	–	10	–	10	–	8	–	8	–	8	–	8	–	$t_{CK}$	37
	ODT turn-on delay	$t_{AOND}$	2													$t_{CK}$	37	
	ODT turn-off delay	$t_{AOFD}$	2.5													$t_{CK}$	35, 37	
	ODT turn-on	$t_{AON}$	$t_{AC}$ (MIN)	$t_{AC}$ (MAX) + 2,575	MIN = $t_{AC}$ (MIN) MAX = $t_{AC}$ (MAX) + 600				MIN = $t_{AC}$ (MIN) MAX = $t_{AC}$ (MAX) + 700				MIN = $t_{AC}$ (MIN) MAX = $t_{AC}$ (MAX) + 1,000				ps	23, 43
	ODT turn-off	$t_{AOF}$	MIN = $t_{AC}$ (MIN) MAX = $t_{AC}$ (MAX) + 600													ps	24, 44	
	ODT turn-on (power-down mode)	$t_{AONPD}$	$t_{AC}$ (MIN) + 2,000	2 x $t_{CK}$ + $t_{AC}$ (MAX) + 1,000	MIN = $t_{AC}$ (MIN) + 2,000 MAX = 2 x $t_{CK}$ + $t_{AC}$ (MAX) + 1,000												ps	50
	ODT turn-off (power-down mode)	$t_{AOFPD}$	MIN = $t_{AC}$ (MIN) + 2,000 MAX = 2.5 x $t_{CK}$ + $t_{AC}$ (MAX) + 1,000													ps		
ODT enable from MRS command	$t_{MOD}$	MIN = 12 MAX = n/a													ns	37, 49		



## Notes

- All voltages are referenced to Vss.
- Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
- Outputs measured with equivalent load (see Figure 81 on page 100).
- AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0 V/ns for signals in the range between VIL(AC) and VIH(AC). Slew rates other than 1.0 V/ns may require the timing parameters to be derated as specified.
- The AC and DC input level specifications are as defined in the SSTL\_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
- There are two sets of values listed for command/address:  $t_{IS_a}$ ,  $t_{IH_a}$  and  $t_{IS_b}$ ,  $t_{IH_b}$ . The  $t_{IS_a}$ ,  $t_{IH_a}$  values (for reference only) are equivalent to the baseline values of  $t_{IS_b}$ ,  $t_{IH_b}$  at VREF when the slew rate is 1 V/ns. The baseline values,  $t_{IS_b}$ ,  $t_{IH_b}$ , are the JEDEC-defined values, referenced from the logic trip points.  $t_{IS_b}$  is referenced from VIH(AC) for a rising signal and VIL(AC) for a falling signal, while  $t_{IH_b}$  is referenced from VIL(DC) for a rising signal and VIH(DC) for a falling signal. If the command/address slew rate is not equal to 1 V/ns, then the baseline values must be derated by adding the values from Tables 21 and 22 on page 86.
- The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew rate of 2 V/ns (1 V/ns for each signal). There are two sets of values listed:  $t_{DS_a}$ ,  $t_{DH_a}$  and  $t_{DS_b}$ ,  $t_{DH_b}$ . The  $t_{DS_a}$ ,  $t_{DH_a}$  values (for reference only) are equivalent to the baseline values of  $t_{DS_b}$ ,  $t_{DH_b}$  at VREF when the slew rate is 2 V/ns, differentially. The baseline values,  $t_{DS_b}$ ,  $t_{DH_b}$ , are the JEDEC-defined values, referenced from the logic trip points.  $t_{DS_b}$  is referenced from VIH(AC) for a rising signal and VIL(AC) for a falling signal, while  $t_{DH_b}$  is referenced from VIL(DC) for a rising signal and VIH(DC) for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated by adding the values from Tables 23 and 24 on pages 89–90. If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended, the baseline values are not applicable, and timing is not referenced to the logic trip points. Single-ended DQS data timing is referenced to DQS crossing VREF. The correct timing values for a single-ended DQS strobe are listed in Tables 25–28 on pages 91–92; listed values are already derated for slew rate variations and can be used directly from the table.
- $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving ( $t_{HZ}$ ) or begins driving ( $t_{LZ}$ ).
- This maximum value is derived from the referenced test load.  $t_{HZ}$  (MAX) will prevail over  $t_{DQSCK}$  (MAX) +  $t_{RPST}$  (MAX) condition.
- $t_{LZ}$  (MIN) will prevail over a  $t_{DQSCK}$  (MIN) +  $t_{RPRE}$  (MAX) condition.
- The intent of the “Don’t Care” state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above VIH[DC] MIN), then it must not transition LOW (below VIH[DC]) prior to  $t_{DQSH}$  (MIN).



12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on  $t_{DQSS}$ .
14. The refresh period is 64ms (commercial) or 32ms (industrial). This equates to an average refresh rate of 7.8125 $\mu$ s (commercial) or 3.9607 $\mu$ s (industrial). To ensure all rows of all banks are properly refreshed, 8,192 REFRESH commands must be issued every 64ms (commercial) or 32ms (industrial).
15. Referenced to each output group: x4 = DQS with DQ0–DQ3; x8 = DQS with DQ0–DQ7; x16 = LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
16. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications:  $t_{HP}$  ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. READs and WRITEs with auto precharge *are* allowed to be issued before  $t_{RAS}$  (MIN) is satisfied since  $t_{RAS}$  lockout feature is supported in 1.5V DDR2 SDRAM.
19.  $V_{IL}/V_{IH}$  1.5V DDR2 overshoot/undershoot. See “AC Overshoot/Undershoot Specification” on page 98.
20.  $t_{DAL} = (nWR) + (t_{RP}/t_{CK})$ . Each of these terms, if not already an integer, should be rounded up to the next integer.  $t_{CK}$  refers to the application clock period;  $nWR$  refers to the  $t_{WR}$  parameter stored in the MR9–MR11. For example, -37E at  $t_{CK} = 3.75$ ns with  $t_{WR}$  programmed to four clocks would have  $t_{DAL} = 4 + (15\text{ns}/3.75\text{ns})$  clocks = 4 + (4) clocks = 8 clocks.
21. The minimum internal READ-to-PRECHARGE time. This is the time from the last 4-bit prefetch begins to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when  $t_{RTP}/(2 \times t_{CK}) > 1$ , such as frequencies faster than 533 MHz when  $t_{RTP} = 7.5$ ns. If  $t_{RTP}/(2 \times t_{CK}) \leq 1$ , then equation AL + BL/2 applies.  $t_{RAS}$  (MIN) also has to be satisfied as well. The 1.5V DDR2 SDRAM will automatically delay the internal PRECHARGE command until  $t_{RAS}$  (MIN) has been satisfied.
22. Operating frequency is only permitted to change during self refresh mode (see Figure 52 on page 71), precharge power-down mode, or system reset condition (See “Reset Function” on page 72). SSC permits small deviations in operating frequency, provided the SSC guidelines are satisfied.
23. ODT turn-on time  $t_{AON}$  (MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time  $t_{AON}$  (MAX) is when the ODT resistance is fully on. Both are measured from  $t_{AOND}$ .
24. ODT turn-off time  $t_{AOF}$  (MIN) is when the device starts to turn off ODT resistance. ODT turn off time  $t_{AOF}$  (MAX) is when the bus is in High-Z. Both are measured from  $t_{AOFD}$ .
25. This parameter has a two clock minimum requirement at any  $t_{CK}$ .
26.  $t_{DELAY}$  is calculated from  $t_{IS} + t_{CK} + t_{IH}$  so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition. See “Reset Function” on page 72.
27.  $t_{ISXR}$  is equal to  $t_{IS}$  and is used for CKE setup time during self refresh exit, as shown in Figure 41 on page 62.



28. The  $t_{FAW}$  (MIN) parameter applies to all 8-bank 1.5V DDR2 devices. No more than four bank-ACTIVE commands may be issued in a given  $t_{FAW}$  (MIN) period.  $t_{RRD}$  (MIN) restriction still applies.
29. When a single-bank PRECHARGE command is issued,  $t_{RP}$  timing applies; and  $t_{RPA}$  timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks open. For 8-bank devices ( $\geq 1\text{Gb}$ ),  $t_{RPA}$  (MIN) =  $t_{RP}$  (MIN) +  $t_{CK}$  (AVG), table lists  $t_{RP}$  (MIN) +  $t_{CK}$  (AVG) MIN.
30. For each input signal not the group collectively.
31. This is applicable to READ cycles only. WRITE cycles generally require additional time due to  $t_{WR}$  during auto precharge.
32.  $t_{CKE}$  (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + 2 \times t_{CK} + t_{IH}$ .
33. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving ( $t_{RPST}$ ) or beginning to drive ( $t_{RPRE}$ ).
34. When DQS is used single-ended, the minimum limit is reduced by 100ps.
35. The half-clock of  $t_{AOFD}$ 's  $2.5 t_{CK}$  assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53,  $t_{AOFD}$  would actually be  $2.5 - 0.03$ , or 2.47, for  $t_{AOF}$  (MIN) and  $2.5 + 0.03$ , or 2.53, for  $t_{AOF}$  (MAX).
36. The clock's  $t_{CK}$  (AVG) is the average clock over any 200 consecutive clocks and  $t_{CK}$  (AVG) MIN is the smallest clock rate permitted, except a deviation due to permitted clock jitter. Input clock jitter is permitted, provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
37. The inputs to the DRAM must be aligned to the associated clock; that is, the actual clock that latches it in. However, the input timing (in ns) references to the  $t_{CK}$  (AVG) when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the  $t_{CK}$  (AVG) rather than  $t_{CK}$ :  $t_{IPW}$ ,  $t_{DIPW}$ ,  $t_{DQSS}$ ,  $t_{DQSH}$ ,  $t_{DQSL}$ ,  $t_{DSS}$ ,  $t_{DSH}$ ,  $t_{WPST}$ , and  $t_{WPRE}$ .
38. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range 20–60 KHz with additional one percent of  $t_{CK}$  (AVG); however, the spread spectrum may not use a clock rate below  $t_{CK}$  (AVG) MIN or above  $t_{CK}$  (AVG) MAX.
39. The period jitter ( $t_{JITPER}$ ) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked).
40. The half-period jitter ( $t_{JITDTY}$ ) applies to either the high pulse of clock or the low pulse of clock; however, the two cumulatively can not exceed  $t_{JITPER}$ .
41. The cycle-to-cycle jitter ( $t_{JITCC}$ ) is the amount the clock period can deviate from one cycle to the following cycle. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked).
42. The cumulative jitter error ( $t_{ERR}_{nPER}$ ), where  $n$  is 2, 3, 4, 5, 6–10, or 11–50, is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
43. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting  $t_{ERR}_{5PER}$  (MAX):  $t_{AC}$  (MIN),  $t_{DQSCK}$  (MIN),



$t_{LZDQS}$  (MIN),  $t_{LZDQ}$  (MIN),  $t_{AON}$  (MIN); while these following parameters are required to be derated by subtracting  $t_{ERR_{5PER}}$  (MIN):  $t_{AC}$  (MAX),  $t_{DQSCK}$  (MAX),  $t_{HZ}$  (MAX),  $t_{LZDQS}$  (MAX),  $t_{LZDQ}$  (MAX),  $t_{AON}$  (MAX). The parameter  $t_{RPRE}$  (MIN) is derated by subtracting  $t_{JITPER}$  (MAX), while  $t_{RPRE}$  (MAX), is derated by subtracting  $t_{JITPER}$  (MIN). The parameter  $t_{RPST}$  (MIN) is derated by subtracting  $t_{JITDTY}$  (MAX), while  $t_{RPST}$  (MAX), is derated by subtracting  $t_{JITDTY}$  (MIN).

44. Half-clock output parameters must be derated by the actual  $t_{ERR_{5PER}}$  and  $t_{JITDTY}$  when input clock jitter is present; this will result in each parameter becoming larger. The parameter  $t_{AOF}$  (MIN) is required to be derated by subtracting both  $t_{ERR_{5PER}}$  (MAX) and  $t_{JITDTY}$  (MAX). The parameter  $t_{AOF}$  (MAX) is required to be derated by subtracting both  $t_{ERR_{5PER}}$  (MIN) and  $t_{JITDTY}$  (MIN).
45. MIN ( $t_{CL}$ ,  $t_{CH}$ ) refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution;  $t_{CH}$  (AVG) and  $t_{CL}$  (AVG) must be met with or without clock jitter and with or without duty cycle jitter.  $t_{CH}$  (AVG) and  $t_{CL}$  (AVG) are the average of any 200 consecutive CK falling edges.
46.  $t_{HP}$  (MIN) is the lesser of  $t_{CL}$  and  $t_{CH}$  actually applied to the device CK and CK# inputs; thus,  $t_{HP}$  (MIN)  $\geq$  the lesser of  $t_{CL}$  (ABS) MIN and  $t_{CH}$  (ABS) MIN.
47.  $t_{QH} = t_{HP} - t_{QHS}$ ; the worst case  $t_{QH}$  would be the smaller of  $t_{CL}$  (ABS) MAX or  $t_{CH}$  (ABS) MAX times  $t_{CK}$  (ABS) MIN -  $t_{QHS}$ . Minimizing the amount of  $t_{CH}$  (AVG) offset and value of  $t_{JITDTY}$  will provide a larger  $t_{QH}$ , which in turn will provide a larger valid data out window.
48. JEDEC specifies using  $t_{ERR_{6-10PER}}$  when derating clock-related output timing (notes 43–44). Micron requires less derating by enabling  $t_{ERR_{5PER}}$  to be used.
49. Should use 8  $t_{CK}$  for backward compatibility.
50. The -187E maximum limit is  $2 \times t_{CK} + t_{AC}$  (MAX) + 1,000 but it will likely be  $3 \times t_{CK} + t_{AC}$  (MAX) + 1,000 in the future.

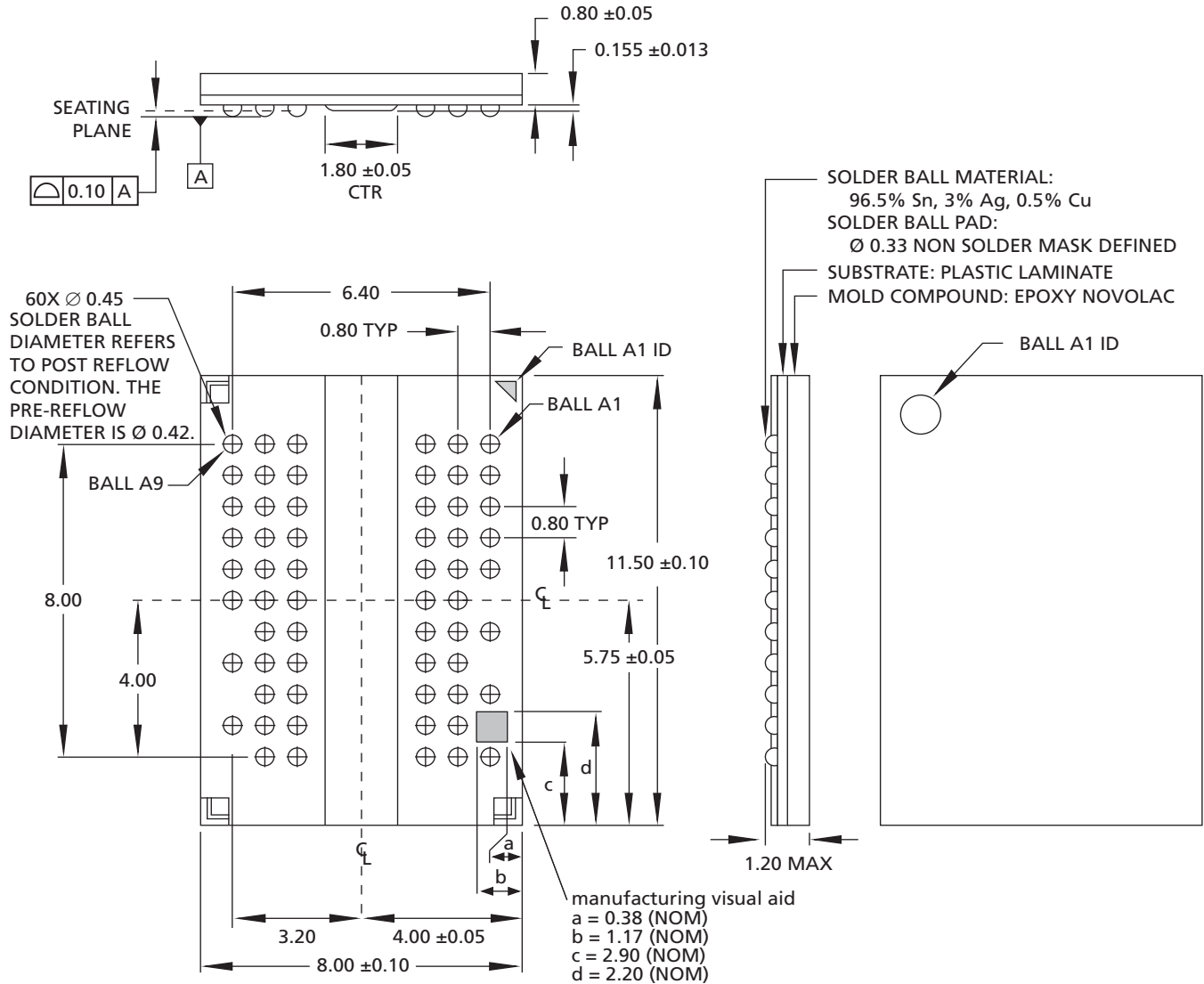




# 1Gb: x4, x8, x16 1.5V DDR2 SDRAM Package Dimensions

## Package Dimensions

Figure 86: 60-Ball FBGA Package – x4, x8



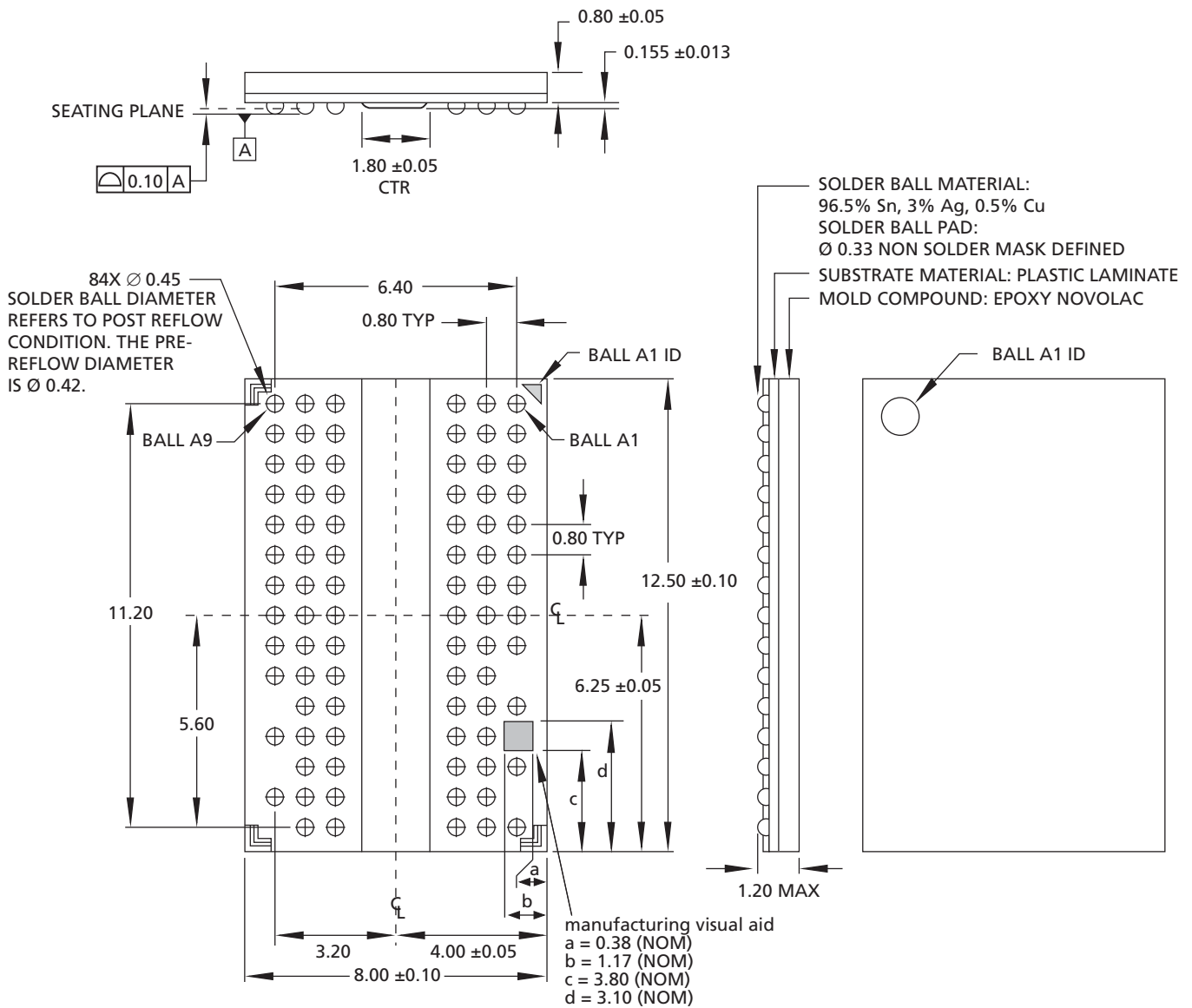
Notes: 1. All dimensions are in millimeters.





**1Gb: x4, x8, x16 1.5V DDR2 SDRAM  
Package Dimensions**

**Figure 87: 84-Ball FBGA Package – x16**



Notes: 1. All dimensions are in millimeters.



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