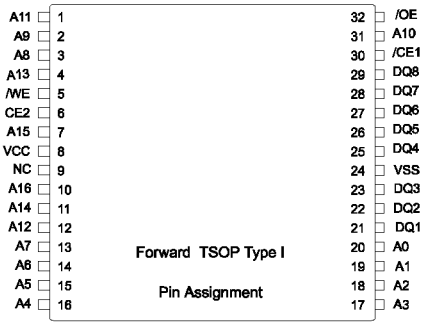
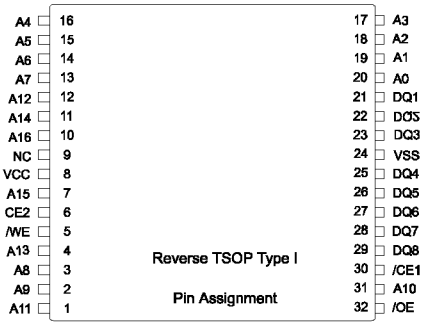
EK621024A

128K x 8 Bit CMOS SRAM



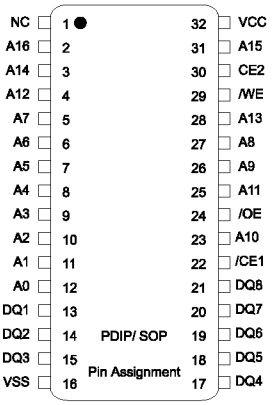


FEATURES

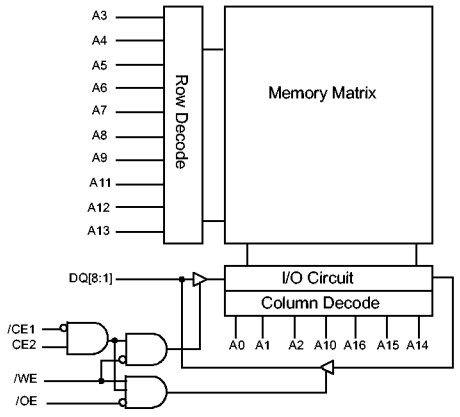
- Access Times
  35ns, 55ns, 70ns, 100ns
- Single 5V ±10% Power Supply
- Industry Standard Pin Assignment
- Package Options
  - 450 mil 32 pin SOP
  - 300 mil 32 pin PDIP (Skinny)
  - 32 pin Forward TSOP Type I (8x20mm)
  - 32 pin Reverse TSOP Type I (8x20mm)

DESCRIPTION

The EK621024A from Eureka is a one-megabit density static random access memory organized as 131,072 words by 8 bits. The device is offered in 450 mil SOP for surface mount applications and 300 mil DIP packages for thru-hole assembly. For low profile memory applications, TSOP is offered in forward and reverse pin assignments. The pin assignment complies with the JEDEC standard pin assignment. The device is fabricated using high performance CMOS technology.



BLOCK DIAGRAM



PIN ASSIGNMENT

Symbol	Description
A0-A16	Address Inputs
DQ1-DQ8	Data Inputs/Outputs
/CE1, CE2	Chip Enables
/WE	Write Enable
/OE	Output Enable
NC	No Connect
Vcc	Power Supply
Vss	Ground

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to Vcc + 0.5	V
Output Voltage	V_{OUT}	-0.5 to Vcc +0.5	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA

Stresses greater than those listed under Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

/CE1	CE2	/OE	/WE	Mode	DQ Pin	Supply Current
H	X	X	X	Not Selected	High - Z	I_{SB},I_{SB1}
X	L	X	X	Not Selected	High - Z	I_{SB},I_{SB1}
L	H	H	H	Output Disabled	High - Z	I_{CCA}
L	H	L	H	Read	Data Out	I_{CCA}
L		X	L	Write	Data In	I_{CCA}

Electrical Characteristics and DC Operating Conditions

(TA =0^0C to + 70^0C; VCC = +5V±10% unless otherwise noted; Note 1)

Description	Symbol	Conditions		Min	Max	Units
Power SupplyVoltage	V_{CC}			4.5	5.5	V
Input Low Voltage	V_{IL}			-0.5	0.8	V
Input High Voltage	V_{IH}			2.2	Vcc+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		-2	2	µA
Output Leakage Current	I_{LO}	V_{IN}=V_{SS} to V_{CC}; /CE1=V_{IH} or CE2 = V_{IL} or /OE=V_{IH} or /WE=V_{IL}		-2	2	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	V
Power Supply Operating Current	I_{CCA}	/CE1 = V_{IL}, CE2 = V_{IH} DQ=0mA, f=max	35ns 55ns 70ns 100ns	- - -	100 90 80 75	mA
Power Supply Standby Current	I_{SB}	/CE1 = V_{IH} OR CE2 = V_{IL}; f=max		-	5	mA
CMOS Standby	I_{SB1}	/CE1≥V_{CC}-0.2V or CE2≤V_{SS}+0.2V, f=0 MHz		-	500	µA

Capacitance

Parameter	Symbol	Max	Units
Input Capacitance	C_{IN}	6	pF
Input/Output Capacitance	$C_{I/O}$	8	pF

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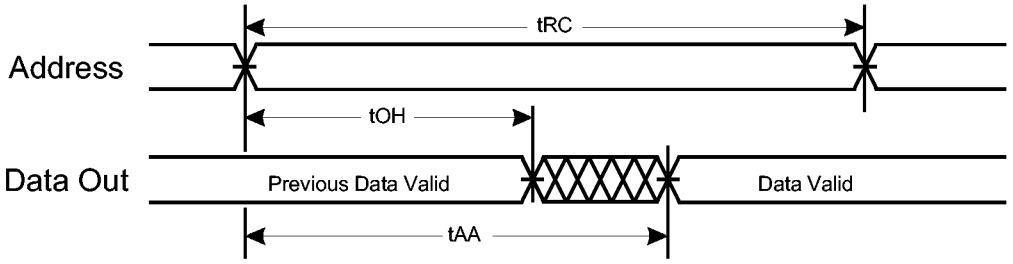
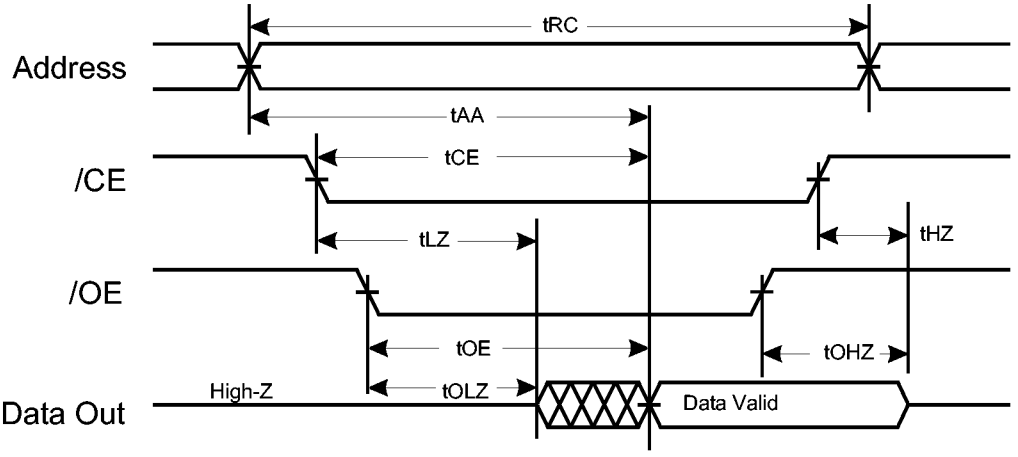
Read Timing (Address Access)



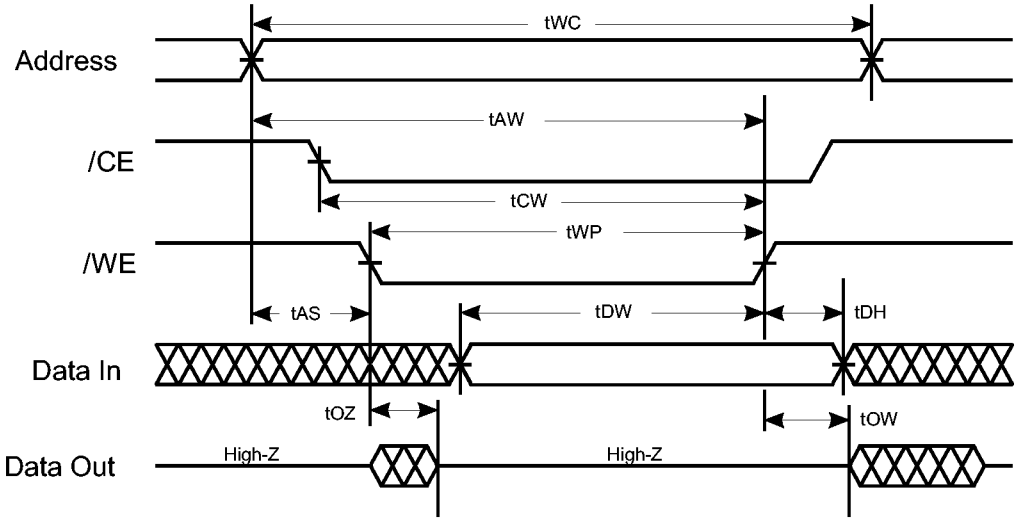
Read Timing (Chip Enable Access)



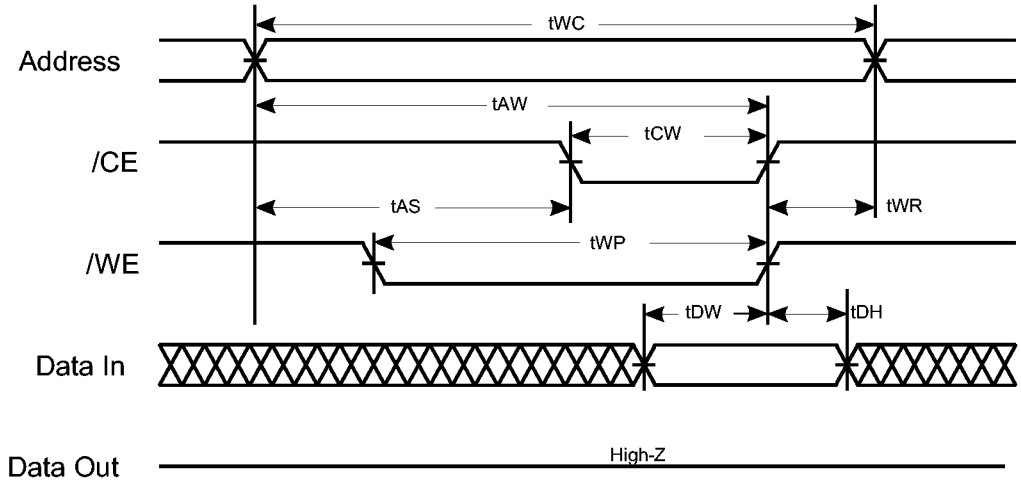
Read Cycle

DESCRIPTION		-35		-55		-70		-100			
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Read Cycle Time	tRC	35	-	55	-	70	-	100	-	ns	2,3,6
Address Access Time	tAA	-	35	-	55	-	70	-	100	ns	2,3
Chip Enable Access Time	tCE	-	35	-	55	-	70	-	100	ns	2,3
Output Enable Access Time	tOE	-	15	-	25	-	35	-	50	ns	
Output Hold from Address Change	tOH	5	-	5	-	5	-	5	-	ns	
Chip Enable Active to Low-Z	tLZ	5	-	5	-	5	-	5	-	ns	2,3
Output Enable to Low-Z	tOLZ	5	-	5	-	5	-	5	-	ns	2,3
Chip Disable to High-Z	tHZ	-	10	-	20	-	25	-	35	ns	2,3,5
Output Disable to High-Z	tOHZ	-	10	-	20	-	25	-	35	ns	2,3,5

Write Cycle (/WE Controlled)



Write Cycle (/CE Controlled)



Write Cycle

DESCRIPTION		-35		-55		-70		-100			
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Write Cycle Time	tRC	35	-	55	-	70	-	100	-	ns	2,4,6
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns	2,4
Address Valid to End of Write	tAW	20	-	45	-	60	-	80	-	ns	2,4
Write Pulse Width	tWP	20	-	40	-	50	-	60	-	ns	2,4
Chip Enable to End of Write	tCW	30	-	40	-	50	-	60	-	ns	2,4
Data Valid to End of Write	tDW	15	-	25	-	30	-	40	-	ns	2,4
Data Hold from End of Write	tDH	0	-	0	-	0	-	0	-	ns	2,4
Write Low to Output High-Z	tOZ	0	10	0	10	0	10	0	10	ns	2,4,5
Write High to Output Low-Z	tOW	5	-	5	-	5	-	5	-	ns	2,4
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns	2,4

AC Test Conditions

(T A = 0 to +70°C, VCC = 5V±10%)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	VIH	2.4	V
Input Pulse Low Level	VIL	0.8	V
Input Rise Time	TR	5.0	ns
Input Fall Time	TF	5.0	ns
Input and Output Timing Reference Level		1.5	V

AC Test Loads

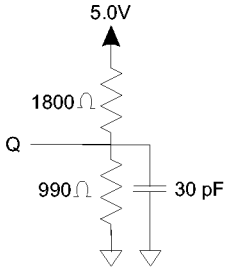


Figure 1A - AC Test Load

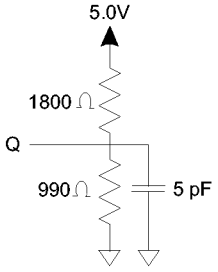


Figure 1B - Hi Z Test Load

Notes:

1. When /WE goes low, outputs are in a Hi-Z state and /OE is overridden.
2. /WE is high for a read cycle.
3. /CE1 and CE2 are represented by /CE in this data sheet. CE2 is of the opposite polarity of /CE in the timing diagrams.
4. A write occurs during the overlap of /CE and /WE.
5. Measured at ±500mv from steady state with the Hi-Z load.
6. Referenced from the last valid address to the first transitioning address pin.

Ordering Information

(Order by Complete Part Number)

EK 621024A X - Y

- Eureka Prefix
- Part Number
- Package Type
  - S = 450 mil SOP
  - K = 300 mil PDIP(Skinny)
  - TS = Forward TSOP Type I (8x20 mm)
  - TX = Reverse TSOP Type I(8x20 mm)
- 35=35ns, 55=55ns, 70=70ns, 100=100ns

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