

18-Bit Universal bus transceiver; 3-state**74ALVC16501****FEATURES**

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Universal bus transceiver with D-type latches and D-type Flip-flops capable of operating in transparent, latched or clocked mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85 °C
- 3-state non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16501 is an 18-bit universal bus transceiver.

Data flow in each direction is controlled by output enable (\overline{OE}_{AB} , \overline{OE}_{BA}), latch-enable (LE_{AB} , LE_{BA}) and clock inputs (CP_{AB} , CP_{BA}).

When LE_{AB} is HIGH, the A-B dataflow is transparent. When LE_{AB} is LOW, and CP_{AB} is held at LOW or HIGH, the A data is latched; on the LOW-to-HIGH transition of CP_{AB} the A-data is stored in the latch/flip-flop. The outputs are active when \overline{OE}_{AB} is HIGH. When \overline{OE}_{AB} is LOW the B-outputs are in 3-state.

Similarly, the LE_{BA} , \overline{OE}_{BA} and CP_{BA} control the B-to-A dataflow. Please note that both output enables are complementary: \overline{OE}_{AB} is active HIGH, \overline{OE}_{BA} is active LOW.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; LE_{AB} to A_n	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	3.0 3.2	ns
C_i	input capacitance		5.0	pF
$C_{i/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

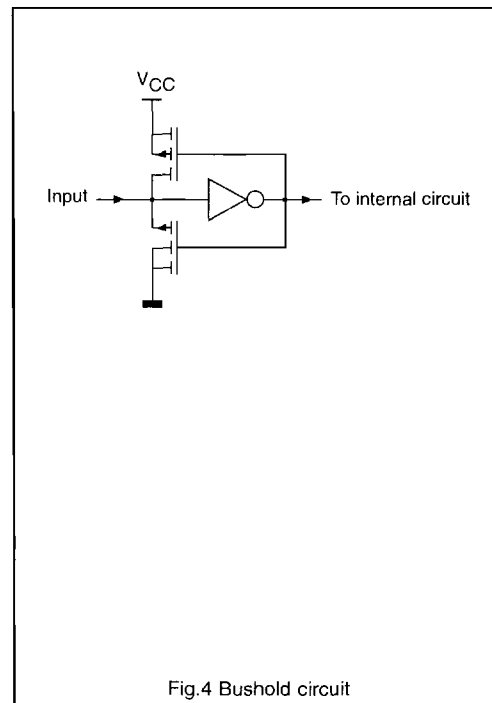
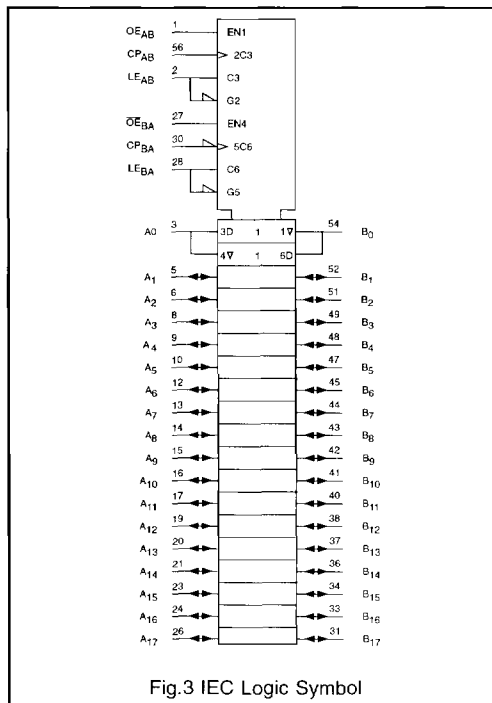
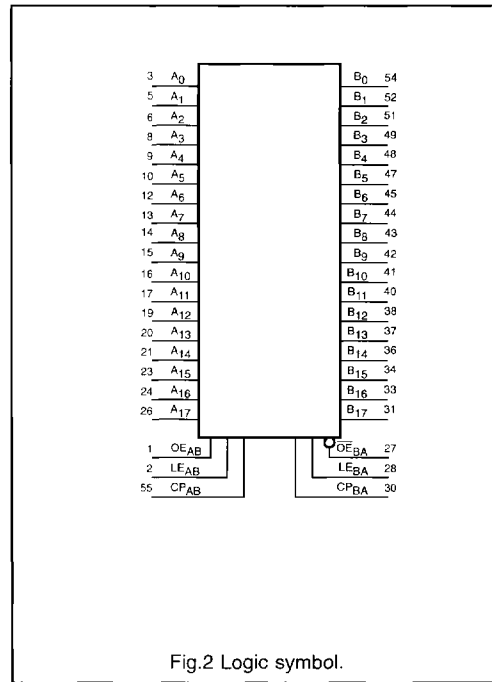
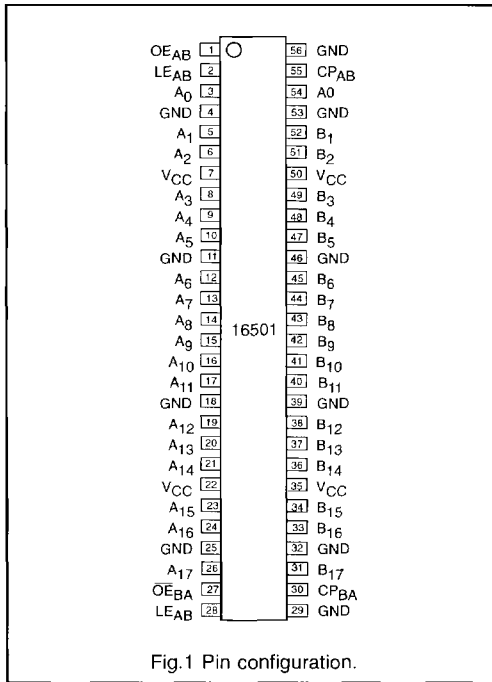
TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16501DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16501DGG	56	TSSOP56	plastic	TSSOP56/SOT364

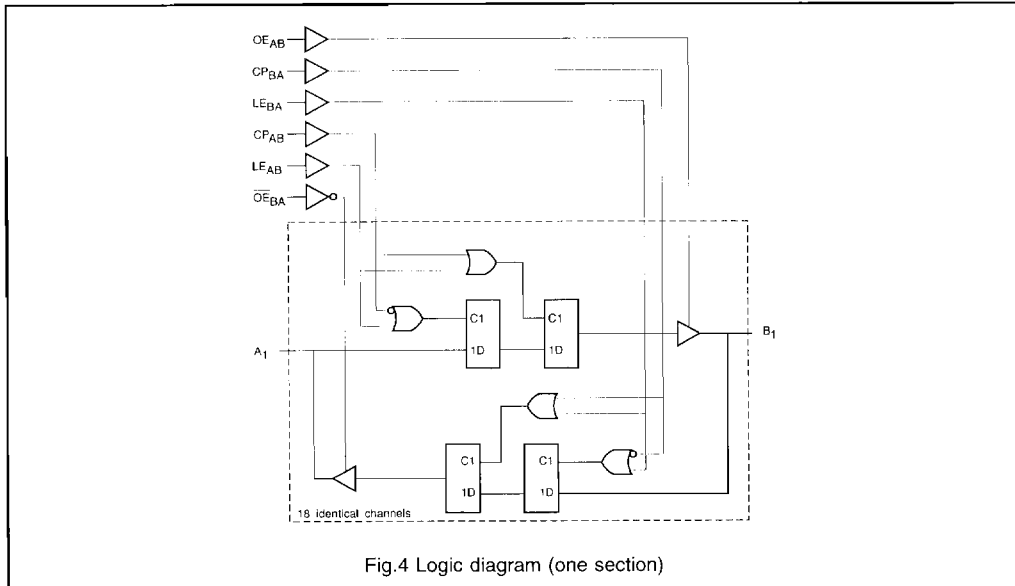
PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{OE}_{AB}	output enable A-to-B
2	LE_{AB}	latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A_0 to A_{17}	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
27	\overline{OE}_{BA}	output enable B-to-A
28	LE_{BA}	latch enable B-to-A
30	CP_{BA}	clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B_0 to B_{17}	'B' data inputs/outputs
55	CP_{AB}	clock input A-to-B, HIGH-to-LOW

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FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OE _{AB} ¹⁾	LE _{xx}	CP _{xx}	DATA		
L	X	X	X	Z	Disabled
H	H	X	H	H	Transparent
H	H	X	L	L	
L	L	↑	h	Z	Disabled + latch
L	L	↑	l	Z	
H	L	↑	h	H	Latch + display
H	L	↑	l	L	
H	L	L	X	NC	Hold
H	L	H	X	NC1	

XX = AB for A-to-B direction, BA for B-to-A direction

H = HIGH voltage level

L = LOW voltage level

h = High state must be present one setup time before the low-to-high transition of CP

l = Low state must be present one setup time before the low-to-high transition of CP

X = Don't care

↑ = LOW-to-HIGH level transition

NC = No change

NC1 = No change provided that CP was LOW before LE_{xx} went low

Z = High impedance "off" state

¹⁾ For the B-to-A direction $\overline{OE_{BA}}$ is the inverse of OE_{AB}

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DC CHARACTERISTICS FOR 74ALVC16501

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

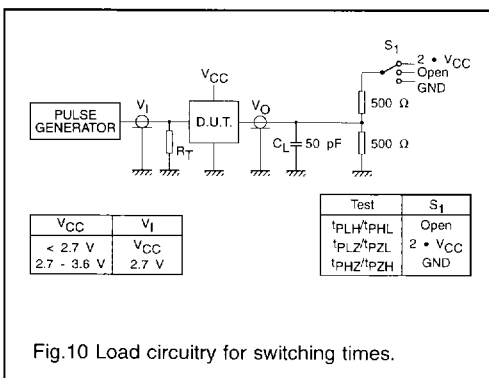
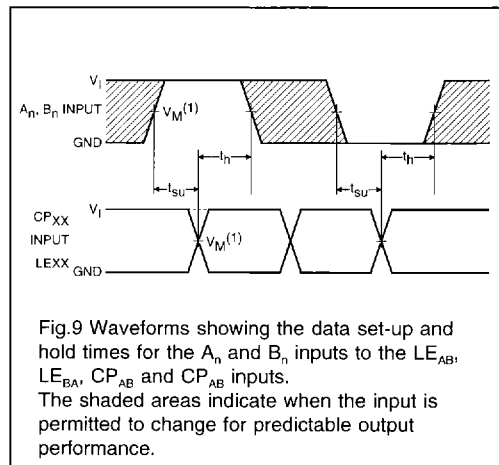
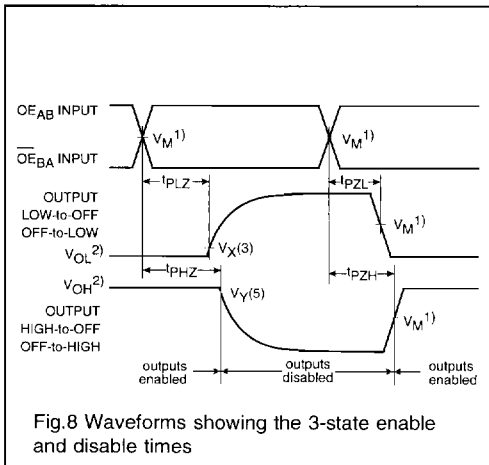
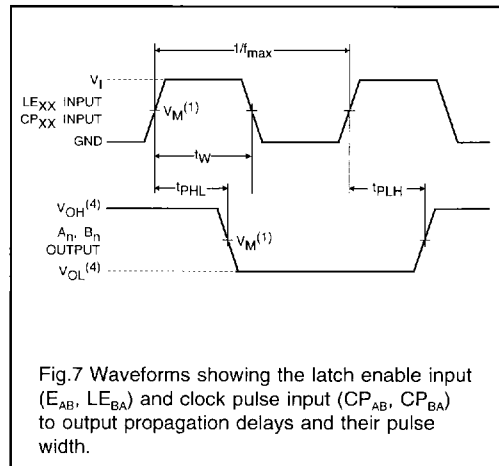
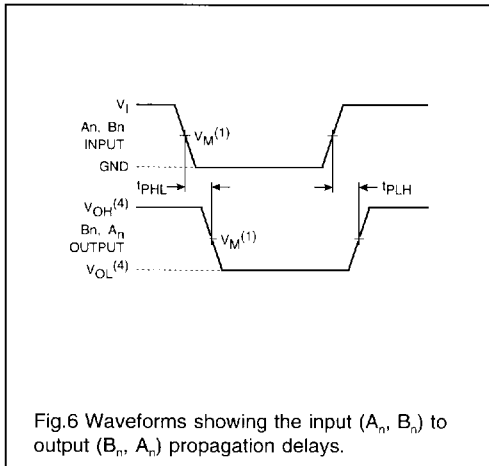
AC CHARACTERISTICS FOR 74ALVC16501GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n , B_n to A_n	-	-	-	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE_{BA} to A_n , LE_{AB} to B_n	-	-	-	ns	1.2 2.7 3.0 to 3.6	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP_{BA} to A_n , CP_{AB} to B_n	-	-	-	ns	1.2 2.7 3.0 to 3.6	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE}_{BA} to A_n , OE_{AB} to B_n	-	-	-	ns	1.2 2.7 3.0 to 3.6	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{BA} to A_n , OE_{AB} to B_n	-	-	-	ns	1.2 2.7 3.0 to 3.6	Fig. 8

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS		
		-40 to +85				V_{CC} (V)	WAVEFORMS	
		MIN.	TYP.	MAX.				
t_w	LE pulse width, LE_{AB} or LE_{BA} HIGH	-	-	-	ns	1.2 2.7 to 3.6	Fig.7	
	LE pulse width, CP_{AB} or CP_{BA} HIGH or LOW	2.5	-	-		1.2 2.7 to 3.6		
t_{su}	set-up time, A_n before $CP_{AB} \downarrow$	-	-	-	ns	1.2 2.7 to 3.6	Fig.9	
	set-up time, B_n before $CP_{AB} \downarrow$	3	-	-		1.2 2.7 to 3.6		
	set-up time, A_n before $LE_{AB} \downarrow$ or B_n before $LE_{AB} \downarrow$	CP high	1.5	-	-			1.2 2.7 to 3.6
		CP low	1.5	-	-			1.2 2.7 to 3.6
t_h	hold time, A_n after $CP_{AB} \downarrow$ or B_n before $CP_{AB} \downarrow$	-	-	-	ns	1.2 2.7 to 3.6		
	hold time, A_n after $LE_{AB} \downarrow$ or B_n before $LE_{BA} \downarrow$	0	-	-		1.2 2.7 to 3.6		

Notes: All typical values are measured at $T_{amb} = 25$ °C.* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS



- Notes:
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (3) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.