T-46-23-05

CY7C167

CYPRESS SEMICONDUCTOR

16,384 x 1 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  — 25 ns
- Low active power
  — 275 mW
- Low standby power
  — 83 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C167 is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C167 has an automatic power-down feature, reducing the power consumption by 67% when deselected.

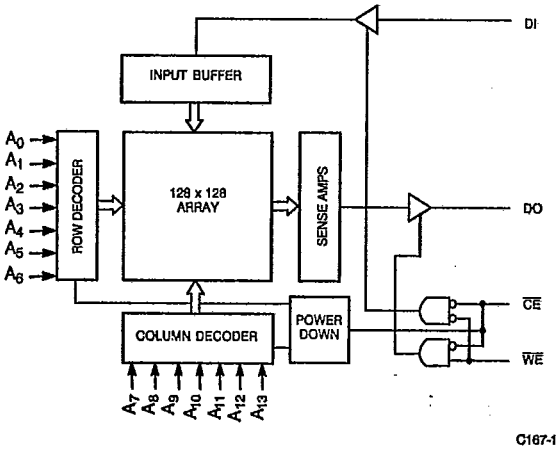
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C167 utilizes a die coat to insure alpha immunity.

Logic Block Diagram



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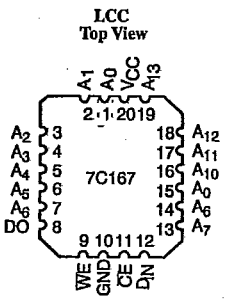
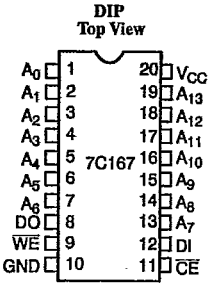
Pin Configurations



C167-2



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Selection Guide

		7C167–25	7C167–35	7C167–45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	60	60	50
	Military		60	50

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential (Pin 26 to Pin 10) ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Output Current into Outputs (Low) ..... 20 mA
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

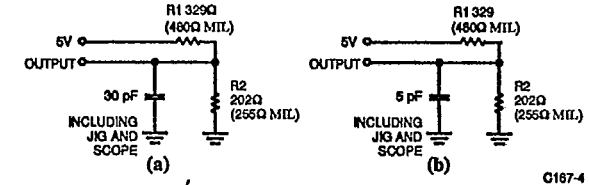
Parameters	Description	Test Conditions			7C167–25 Min.	7C167–25 Max.	7C167–35 Min.	7C167–35 Max.	7C167–45 Min.	7C167–45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA	Com'l		0.4		0.4		0.4	V
			I_{OL} = 8.0 mA	Mil		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND				−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		Com'l		60		60		50	mA
				Mil						50	
I_{SB}	Automatic CE[4] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		Com'l		20		20		15	mA
				Mil						20	

Capacitance[5]

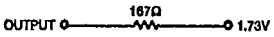
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF
C_{OUT}	Chip Enable Capacitance		5	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

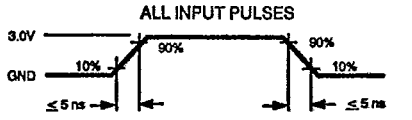
AC Test Loads and Waveforms

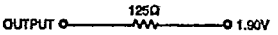


Equivalent to: THÉVENIN EQUIVALENT



Military





Commercial

Switching Characteristics Over the Operating Range[2, 6]

Parameters	Description		7C167–25 Min.	7C167–25 Max.	7C167–35 Min.	7C167–35 Max.	7C167–45 Min.	7C167–45 Max.	Units
READ CYCLE									
t_{RC}	Read Cycle Time	Com'l	25		30		40		ns
		Mil	25		35		40		ns
t_{AA}	Address to Data Valid	Com'l		25		30		40	ns
		Mil				35		40	ns
t_{OHA}	Output Hold from Address Change		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]			15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down			20		25		30	ns
WRITE CYCLE[9]									
t_{WC}	Write Cycle Time		25		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		25		30		40		ns
t_{AW}	Address Set-Up to Write End		25		30		40		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		15		20		20		ns
t_{SD}	Data Set-Up to Write End		15		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]			15		20		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		0		0		0		ns

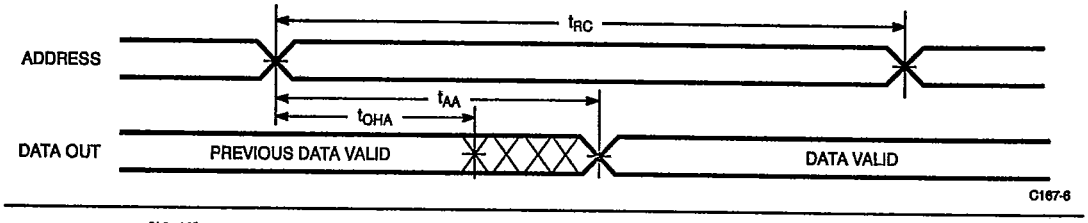
Notes:

6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

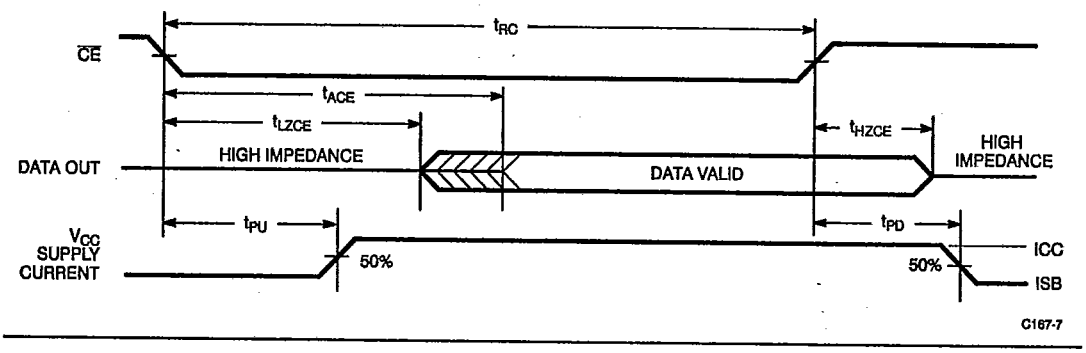
SRAMs

Switching Waveforms

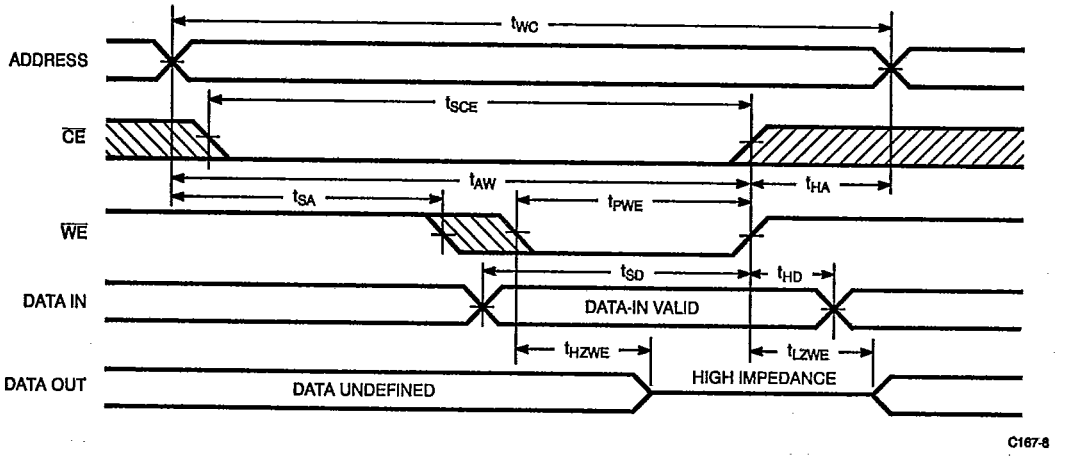
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]

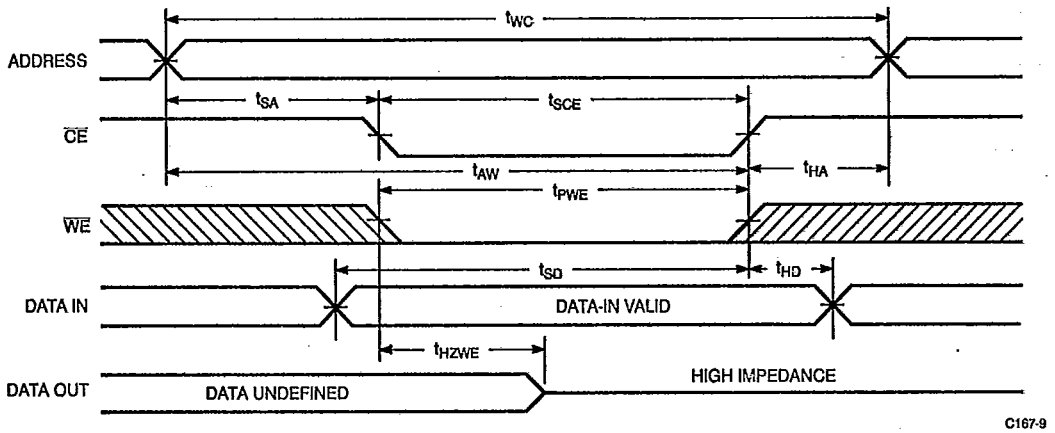


Write Cycle No. 1 ($\overline{WE}$ Controlled)[9]

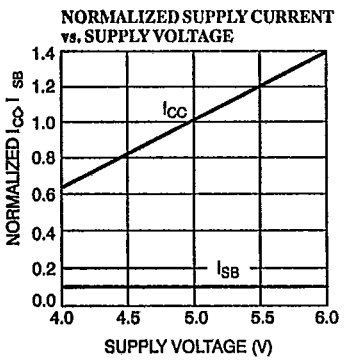


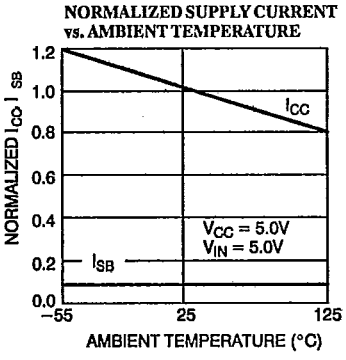
Switching Waveforms (continued)

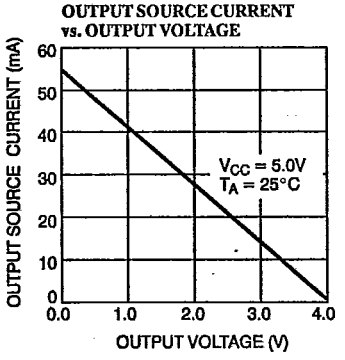
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13]

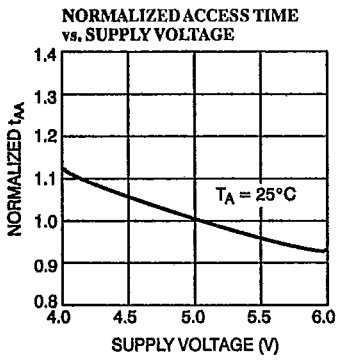


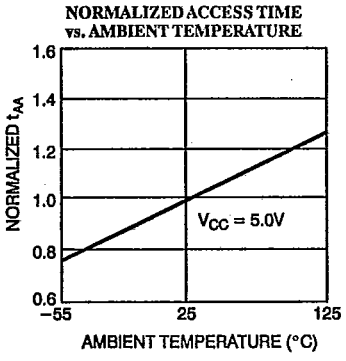
Typical DC and AC Characteristics

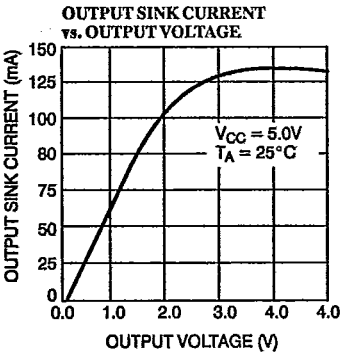






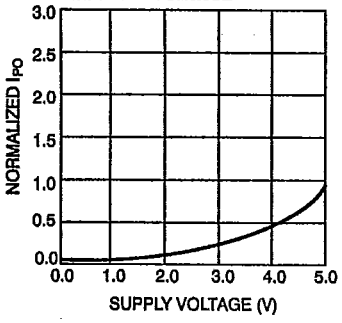




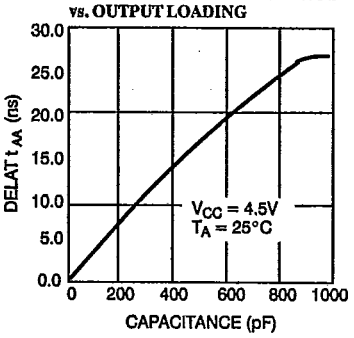


Typical DC and AC Characteristics (continued)

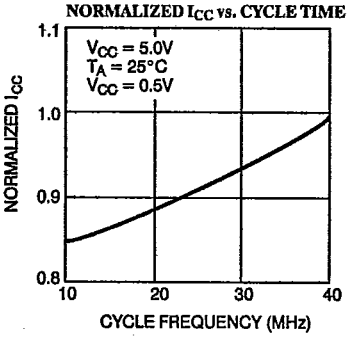
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
25	60	CY7C167-25PC	P5	Commercial
		CY7C167-25DC	D16	
		CY7C167-25LC	L51	
		CY7C167-25VC	V5	
35	60	CY7C167-35PC	P5	Commercial
		CY7C167-35DC	D6	
		CY7C167-35LC	L51	
		CY7C167-35VC	V5	
45	50	CY7C167-45PC	P5	Commercial
		CY7C167-45DC	D6	
		CY7C167-45LC	L51	
		CY7C167-45VC	V5	
		CY7C167-45DMB	D6	Military
		CY7C167-45LMB	L51	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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