

PROTECTION PRODUCTS - MicroClamp®

Description

The μ Clamp®2804L TVS diode is specifically designed to meet the performance requirements of Gigabit Ethernet interfaces. They are designed to protect sensitive PHY chips from damage or upset due to electrostatic discharge (ESD), lightning, electrical fast transients (EFT), and cable discharge events (CDE).

The μ Clamp2804L is constructed using Semtech's low voltage EPD process technology. The EPD process provides low operating voltages with significant reductions in leakage current and capacitance over silicon-avalanche diode processes. The device features low variation in capacitance over bias for stable operation on GbE lines. This means the μ Clamp2804L will introduce zero traffic frame errors on GbE interfaces up to a PHY temperature of 100°C (100M Cat 5/5e Cable). The μ Clamp2804L also features high surge capability and can be used to replace existing SLVU2.8-4 devices in applications where the device is placed on the PHY side of the magnetics. In this configuration, the device can withstand intra-building lightning surges per Telcordia GR-1089.

The μ Clamp2804L is in a 8-pin SOIC package. The leads are finished with lead-free matte tin. The combination of low clamping voltage, high surge capability, and low loading capacitance makes the uClamp2804L an ideal solution for protecting GbE systems to the lightning immunity requirements of GR-1089.

Features

- ◆ High ESD withstand Voltage: +/-**30kV** (Contact/Air) per **IEC 61000-4-2**
- ◆ Able to withstand over 1000 ESD strikes per IEC 61000-4-2 Level 4
- ◆ Flow-through design simplifies layout
- ◆ Protects two line pairs
- ◆ Low reverse current: 10nA typical (VR=2.8V)
- ◆ Low variation in capacitance vs. bias voltage: **1.3pF** Typical (VR = 0 to 2.8V)
- ◆ Working voltage: 2.8V
- ◆ Solid-state silicon-avalanche technology

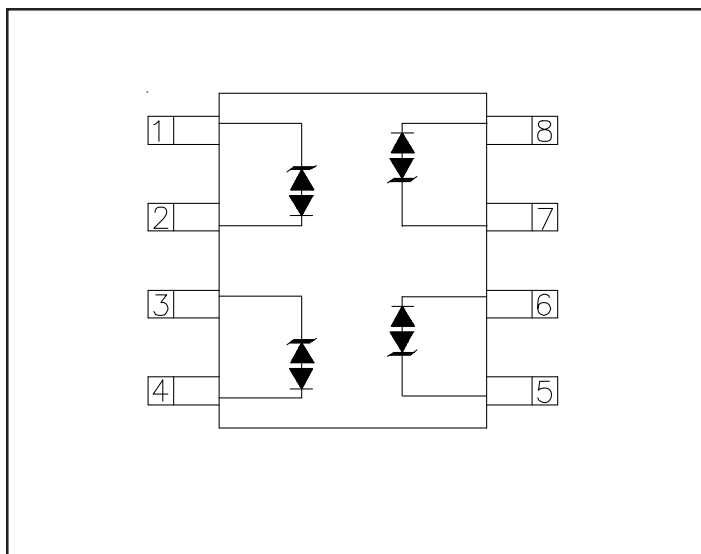
Mechanical Characteristics

- ◆ JEDEC SO-8 package
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Lead Finish: Matte tin
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Marking code, date code
- ◆ Packaging : Tape and Reel

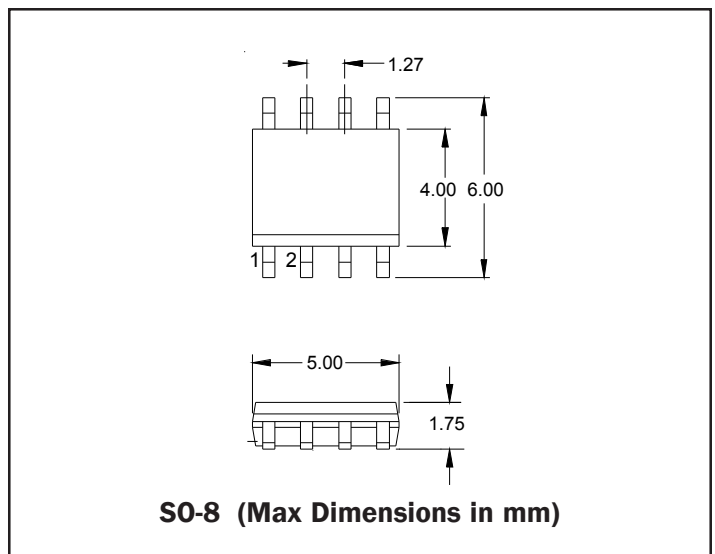
Applications

- ◆ 10/100/1000 Ethernet
- ◆ Integrated magnetics/RJ-45 connectors
- ◆ LAN/WAN Equipment
- ◆ Security Cameras
- ◆ Industrial Controls
- ◆ Notebooks & Desktop Computers

Functional Circuit Diagram



Package Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	100	Watts
Maximum Peak Pulse Current (tp = 8/20μs)	I_{pp}	10	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 30 +/- 30	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

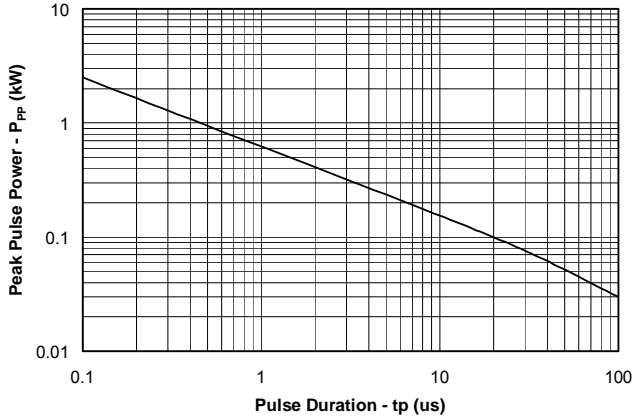
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				2.8	V
Punch-Through Voltage	V_{PT}	$I_{PT} = 2\mu A$	3.5	3.8	4.3	V
Snap-Back Voltage	V_{SB}	$I_{SB} = 50mA$	2.8			V
Reverse Leakage Current	I_R	$V_{RWM} = 2.8V$		0.01	0.05	μA
Clamping Voltage	V_C	$I_{pp} = 1A, tp = 8/20\mu s$			5.5	V
Clamping Voltage	V_C	$I_{pp} = 10A, tp = 8/20\mu s$			10	V
Variation in capacitance with reverse bias ¹		Pins 1, 8 to 2, 7 and pins 3, 6 to 4, 5 $V_R = 0$ to 2.8V $f = 1MHz$		1.3		pF
Junction Capacitance	C_J	Pins 1, 8 to 2, 7 and pins 3, 6 to 4, 5 $V_R = 2.8V, f = 1MHz$		4.5	6	pF

Notes:

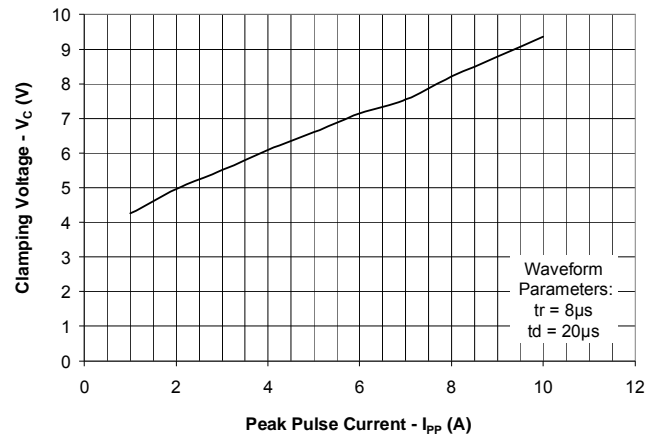
1) This parameter guaranteed by design and characterization and is not production tested

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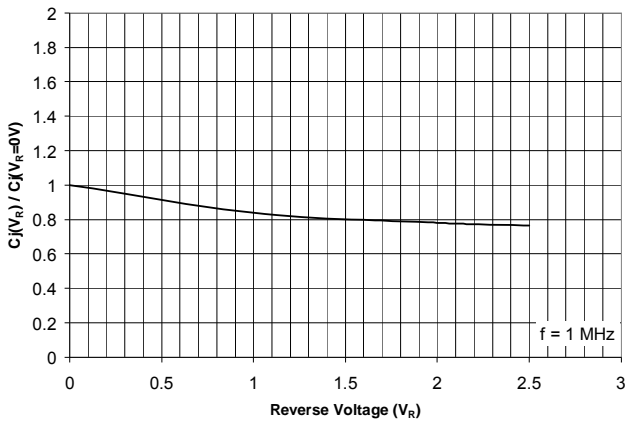
Non-Repetitive Peak Pulse Power vs. Pulse Time



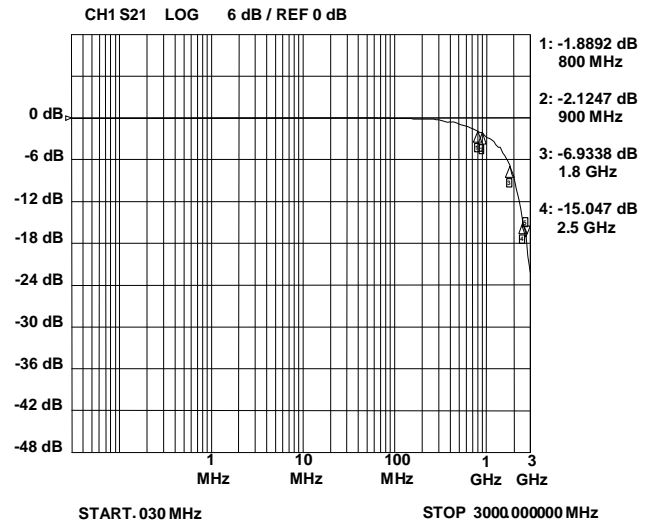
Clamping Voltage vs. Peak Pulse Current



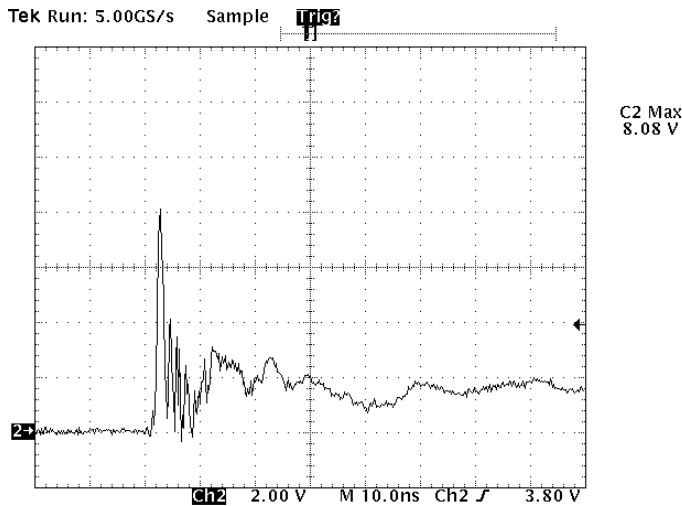
Normalized Junction Capacitance vs. Reverse Voltage



Typical Insertion Loss (S21)

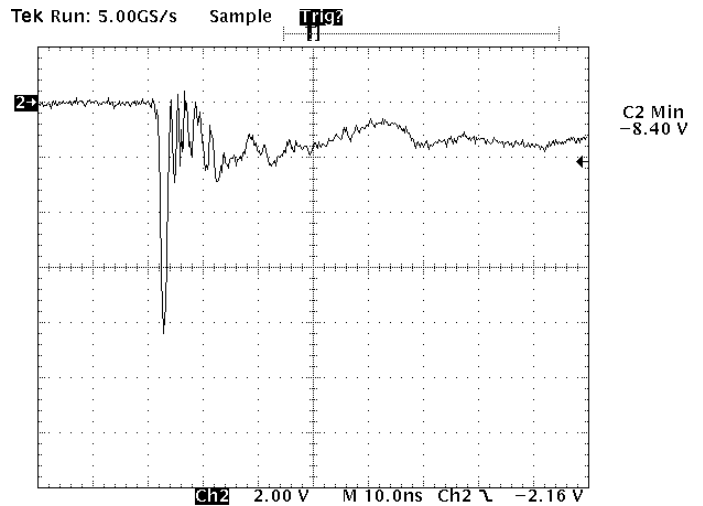


**ESD Clamping
(8kV Contact per IEC 61000-4-2)**



Note: Data is taken with a 10x attenuator

**ESD Clamping
(-8kV Contact per IEC 61000-4-2)**



Note: Data is taken with a 10x attenuator

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Device Connection Options for Protection of Four High-Speed Data Lines

The uClamp2804L is designed to protect four high-speed data lines (two differential pairs) from transient over-voltages which result from lightning and ESD. Data line inputs/outputs are connected at pins 1 and 8, 2 and 7, 3 and 6, and 4 and 5. The device is designed such that PCB traces must remain unbroken and routed through the device as shown in Figure 2.

Gigabit Ethernet Protection Solutions

When designing Ethernet protection, the entire system must be considered. An Ethernet port includes interface magnetics in the form of transformers and common mode chokes. Transformers and chokes can be discrete components, but integrated solutions that include the RJ-45 connector, resistors, capacitors, and protection are also available. In either case, the transformer will provide a high level of common mode isolation to external voltages, but no protection for metallic (line-to-line) surges. During a metallic transient event, current will flow into one line, through the transformer and back to the source. As the current flows, it charges the windings of the transformer on the line side. Once the surge is removed, the windings on the line side will stop charging and will transfer its stored energy to the IC side where the Ethernet transceiver or PHY IC is located. The magnitude and duration of the surge is attenuated by the inductance of the magnetics. The amount of attenuation will vary by vendor and configuration of the magnetics. It is this transferred energy that must be clamped by the protection circuitry.

A typical protection scheme which utilizes the uClamp2804L is shown in Figure 3. One device is placed across two line pairs and is located on the PHY side of the transformer as close to the magnetics as possible. This is done to minimize parasitic inductance and improve clamping performance. In this design, the isolation voltage of the transformer is relied upon to suppress common mode lightning surges. The need for a common mode protection device depends upon the magnitude of the surge and the isolation rating of the transformer. Most transformers are rated for at least 1500V of common mode isolation. It is also

Figure 1 - Circuit Diagram

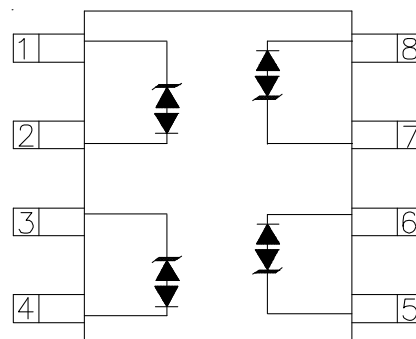
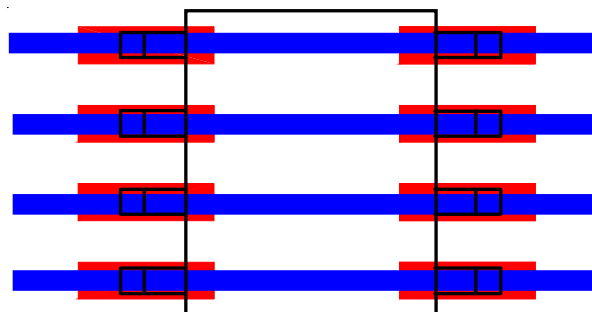


Figure 2 - Connection for Protection of Two Differential Line pairs



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important to make sure the resistor/capacitor termination networks are rated accordingly. Metallic surges will be transferred in some form to the PHY side and clamped by the uClamp2804L. The amount of energy will vary depending on the transformer, but will be well within the surge handling capability of the uClamp2804L. The uClamp2804L will turn on when the voltage across it exceeds the punch-through voltage of the device. Low voltage turn on is important since many PHY chips have integrated ESD protection structures. These structures are for protection of the device during manufacture and are not designed to handle large amounts of energy. Should they turn on before the external protection, they can be damaged resulting in failure of the PHY chip. As always, the final design should be verified with testing.

Replacing SLVU2.8-4 in Existing Designs

The uClamp2804L can be used to replace SLVU2.8-4 in existing designs where the device is placed on the PHY side of the transformer. This is true even though the uClamp2804L is rated for a lower peak pulse current than the SLVU2.8-4. The reason is that the duration and magnitude of the input surge waveform will be attenuated by the magnetics such that the amount of energy that is delivered to the uClamp2804L will be well within the capability of the device.

Lightning Surge Test Results

During the metallic (line-to-line) surge test, the line being stressed is tied to the surge generator with the remaining lines tied together and connected to the generator ground. Current will flow through the line transformer transferring energy to the PHY side of the transformer. Figure 4 shows the test set-up for measuring the clamping voltage of the device. This set up is designed to simulate the surge in an actual gigabit Ethernet (GbE) circuit. A 100 Ohm resistor is used to simulate the differential load of the PHY. Figure 5 shows the clamping voltage of the uClamp2804L for a metallic mode 4000V (100A) 10/700 μ s surge. The clamping voltage, measured at less than 11 volts, provides sufficient clamping margin to minimize electrical stress and is well below the failure voltage range of typical GbE PHY chips that have been tested by Semtech. The graph in Figure 6 shows the typical clamping voltage of the uClamp2804L compared to the clamping voltage of the SLVU2.8-4. An integrated magnetics module was used for the line side magnetics/RJ-45. As shown, the clamping voltage of both devices is nearly identical across the voltage test range.

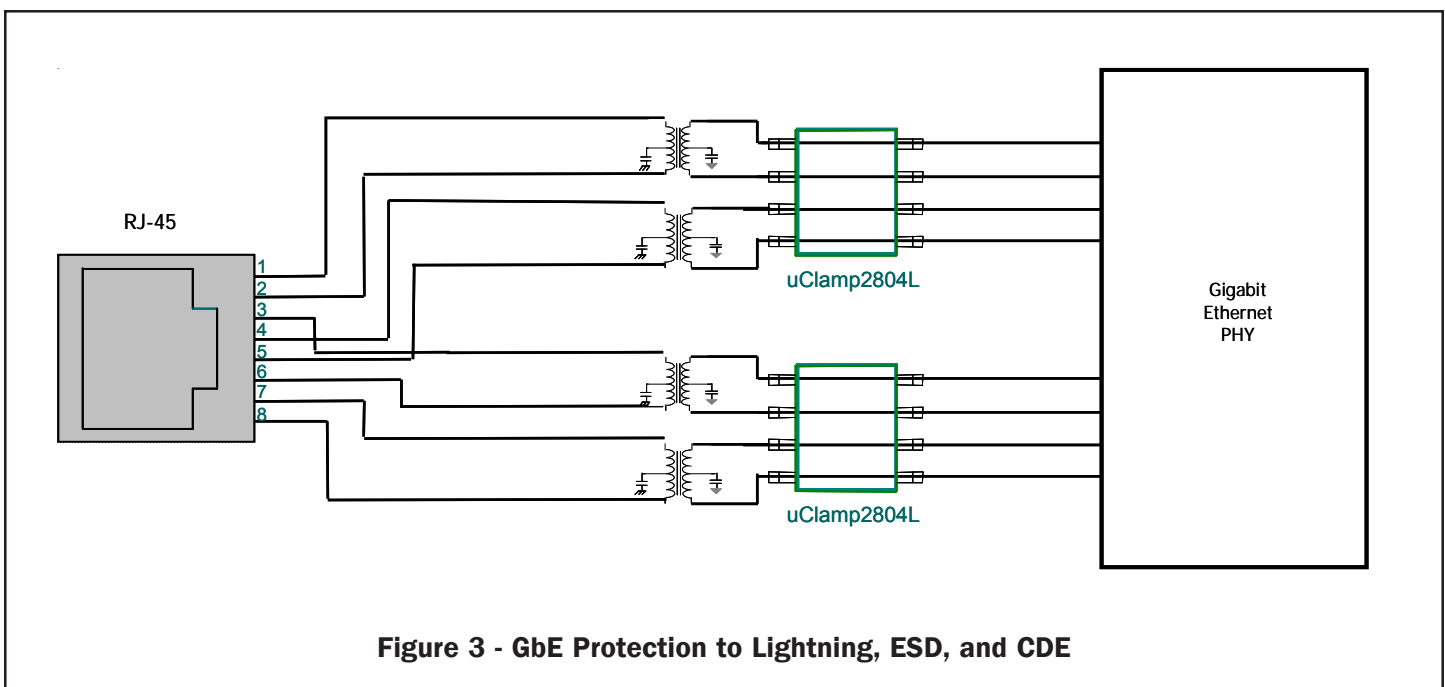


Figure 3 - GbE Protection to Lightning, ESD, and CDE

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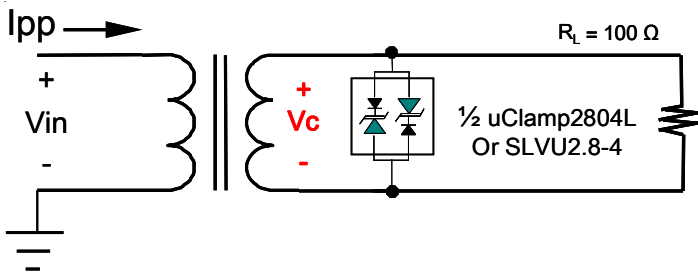
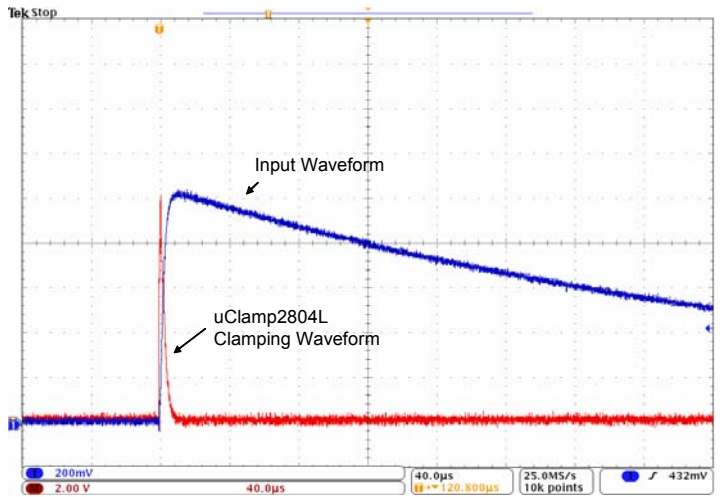


Figure 4 - Clamping Voltage Test Set-Up



Channel 1:
Input surge:
4000V, 100A, 10x700us

Channel M:
Typical clamping voltage
of uClamp2804L (test set-up
per Figure 4).

Figure 5 - Typical uClamp2804L Clamping Response

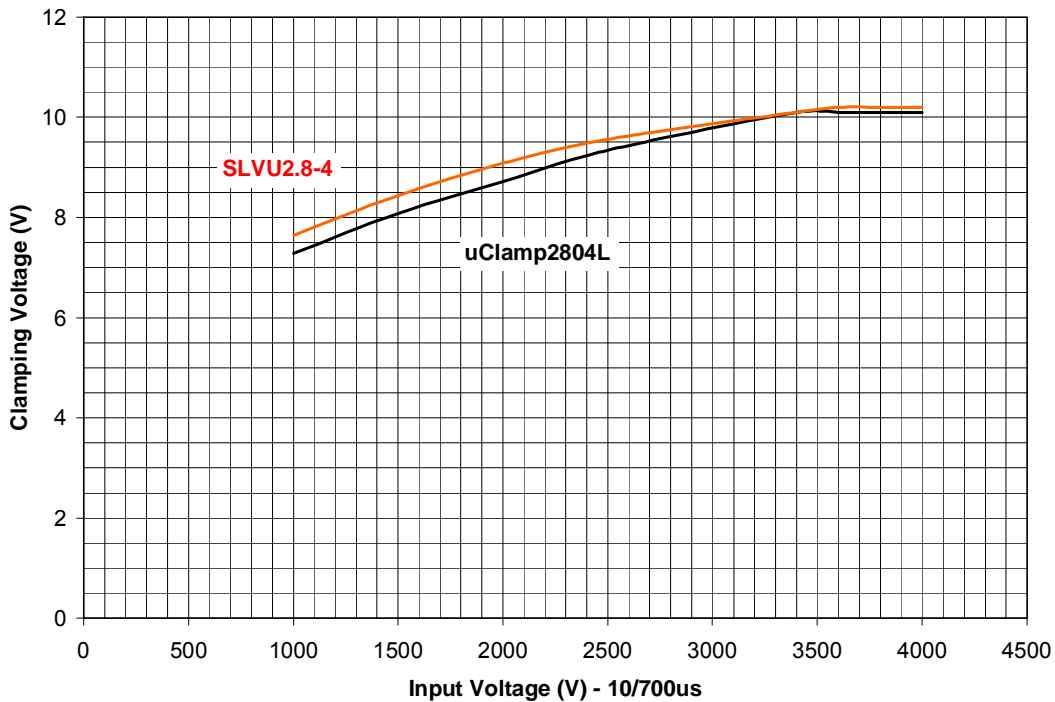
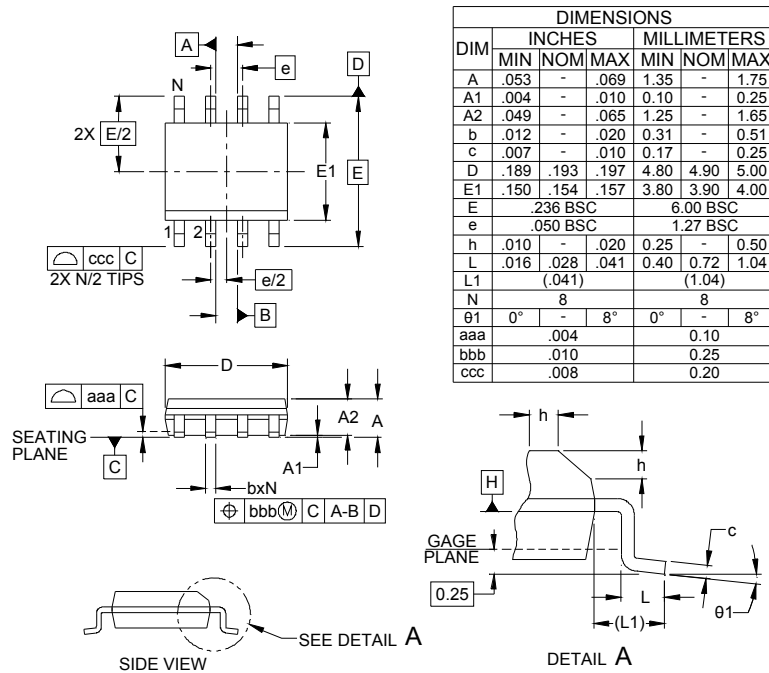


Figure 6 - uClamp2804L vs. SLVU2.8-4
Typical Clamping Voltage (PHY Side of Magnetics) vs. Vin (Line Side of magnetics)

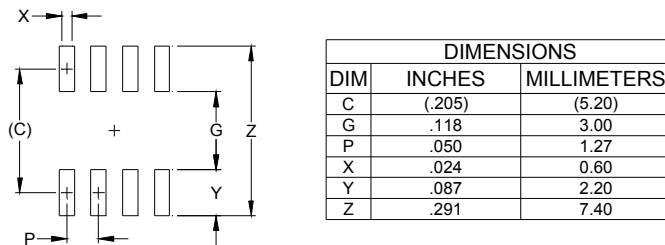
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Outline Drawing - SOIC-8



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SOIC-8



- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
 2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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Marking Code



YYWW = Date Code

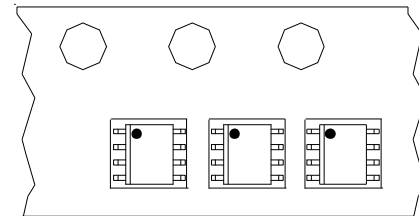
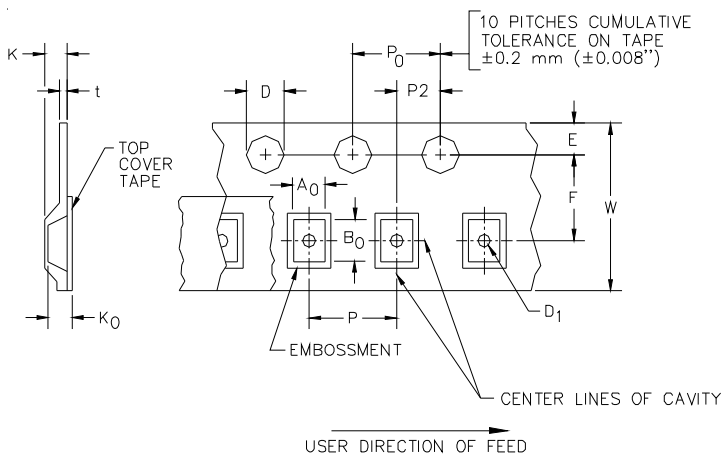
Ordering Information

Part Number	Working Voltage	Qty per Reel	Reel Size
uClamp2804L.TCT	2.8 Volts	3000	13 Inch

Notes:

1) MicroClamp, uClamp and μ Clamp are trademarks of Semtech Corporation

Tape and Reel Specification



User Direction of feed

Device Orientation in Tape

A0	B0	K0
6.45 +/-0.10 mm	5.37 +/-0.10 mm	2.10 +/-0.10 mm

Tape Width	D	D1	E	F	K	P	P0	P2	T(MAX)	W
12 mm	1.5 + 0.1 mm - 0.0 mm	1.5 +0.25 mm	1.75±.10 mm	5.5±0.05 mm	2.1 ±0.1 mm	8.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.25 ±0.02 mm	12 mm + 0.3 mm - 0.1 mm

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