

September 1997 - Revised May 2000

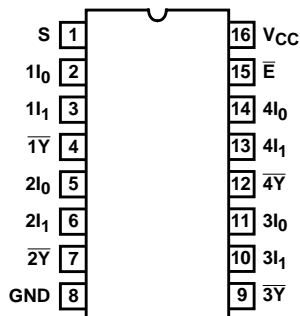
High Speed CMOS Logic Quad 2-Input Multiplexers

Features

- Common Select Inputs
- Separate Enable Inputs
- Buffered inputs and Outputs
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Pinout

CD54HC157, CD54HCT157, CD54HC158, CD54HCT158
 (CERDIP)
 CD74HC157, CD74HCT157, CD74HC158, CD74HCT158
 (PDIP, SOIC)
 TOP VIEW



Description

The 'HC157, 'HCT157, 'HC158, and 'HCT158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active Low. When (\bar{E}) is High, all of the outputs in the 158, the inverting type, ($\overline{1Y-4Y}$) are forced High and in the 157, the non-inverting type, all of the outputs ($\overline{1Y-4Y}$) are forced Low, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

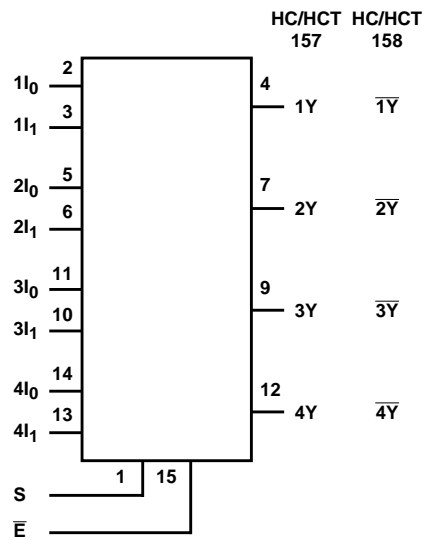
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC157F	-55 to 125	16 Ld CERDIP
CD54HC157F3A	-55 to 125	16 Ld CERDIP
CD74HC157E	-55 to 125	16 Ld PDIP
CD74HC157M	-55 to 125	16 Ld SOIC
CD54HCT157F3A	-55 to 125	16 Ld CERDIP
CD74HCT157E	-55 to 125	16 Ld PDIP
CD74HCT157M	-55 to 125	16 Ld SOIC
CD54HC158F3A	-55 to 125	16 Ld CERDIP
CD74HC158E	-55 to 125	16 Ld PDIP
CD74HC158M	-55 to 125	16 Ld SOIC
CD54HCT158F3A	-55 to 125	16 Ld CERDIP
CD74HCT158E	-55 to 125	16 Ld PDIP

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Functional Diagram



TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT	
				157	158
\bar{E}	S	I0	I1	Y	\bar{Y}
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	115
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS	
	HCT157	HCT158
I (All)	0.95	0.4
\bar{E}	0.6	0.6
S	3	2.8

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC/HCT157 TYPES											
Propagation Delay (Figure 1) Data to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	125	-	155	-	190	ns
			4.5	-	-	25	-	31	-	38	ns
HC157		C _L = 15pF	5	-	10	-	-	-	-	-	ns
			-	-	12	-	-	-	-	-	ns
HCT157		C _L = 50pF	6	-	-	21	-	26	-	32	ns
-			-	-	-	-	-	-	-	-	-

CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
HC157		C _L = 15pF	5	-	11	-	-	-	-	-	ns
			HCT157	-	12	-	-	-	-	-	ns
Select to Output		C _L = 50pF	6	-	-	23	-	29	-	35	ns
			C _L = 50pF	2	-	-	145	-	180	-	220
HC157	C _L = 15pF	5	-	12	-	-	-	-	-	ns	
		HCT157	-	15	-	-	-	-	-	ns	
C _L = 50pF	6	-	-	25	-	31	-	38	ns		
	C _L = 50pF	6	-	-	25	-	31	-	38	ns	
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	-	-	-	-	-	-	
HC157				-	62	-	-	-	-	-	pF
HCT157				-	70	-	-	-	-	-	pF
HC/HCT158 TYPES											
Data to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	
HC158		C _L = 15pF	5	-	11	-	-	-	-	-	ns
			HCT158	-	13	-	-	-	-	-	ns
Enable to Output		C _L = 50pF	6	-	-	24	-	30	-	36	ns
			C _L = 50pF	2	-	-	160	-	200	-	240
HC158	C _L = 15pF	5	-	13	-	-	-	-	-	ns	
		HCT158	-	15	-	-	-	-	-	ns	
C _L = 50pF	6	-	-	27	-	34	-	41	ns		
	C _L = 50pF	2	-	-	150	-	190	-	225	ns	
Select to Output	C _L = 50pF	4.5	-	-	30	-	38	-	45	ns	
		HC158	C _L = 15pF	5	-	12	-	-	-	-	ns
HCT158	C _L = 15pF	5	-	12	-	-	-	-	-	ns	
		HCT158	-	14	-	-	-	-	-	ns	
C _L = 50pF	6	-	-	26	-	33	-	38	ns		
	C _L = 50pF	2	-	-	75	-	95	-	110	ns	
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance (Notes 4, 5)			C _{PD}	-	5	-	-	-	-	-	-
HC158	-	35				-	-	-	-	pF	
HCT158	-	35				-	-	-	-	pF	
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per multiplexer.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

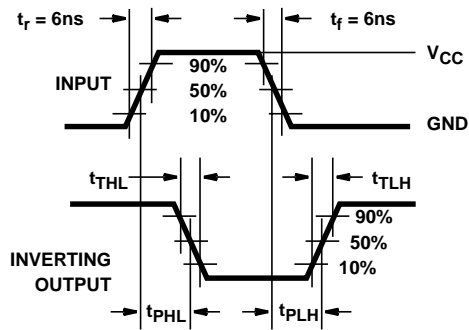


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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PRODUCT SUPPORT: [TRAINING](#)

CD54HCT157, High Speed CMOS Logic Quad 2-Input Multiplexers

DEVICE STATUS: ACTIVE

PARAMETER NAME	CD54HCT157
Voltage Nodes (V)	5

FEATURES

[▲Back to Top](#)

- Common Select Inputs
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DESCRIPTION

[▲Back to Top](#)

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TECHNICAL DOCUMENTS

[▲Back to Top](#)

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DATASHEET

[▲Back to Top](#)

Full datasheet in Acrobat PDF: [cd54hct157.pdf](#) (34 KB,Rev.A) (Updated: 05/19/2000)

APPLICATION NOTES

[▲Back to Top](#)

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- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)

- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

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[▲Back to Top](#)

- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

[▲Back to Top](#)

- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

PRICING/AVAILABILITY/PKG

[▲Back to Top](#)

DEVICE INFORMATION							
Updated Daily							
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY
5962-9070201MEA	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 3.83	1
CD54HCT157F3A	ACTIVE	CDIP (J) 16	-55 TO 125	5962-9070201MEA	View Contents	1KU 3.82	1

TI INVENTORY STATUS		
As Of 08:00 AM GMT, 17 Apr 2003		
IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
118*	>10k 20 May	8 WKS
22*	276 06 May	8 WKS
	>10k 20 May	

REPORTED DISTRIBUTOR INVENTORY		
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CD54HC157, High Speed CMOS Logic Quad 2-Input Multiplexers

DEVICE STATUS: **ACTIVE**

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Voltage Nodes (V)	6, 5, 2

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[▲Back to Top](#)

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[▲Back to Top](#)

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[▲Back to Top](#)

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[▲Back to Top](#)

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)

- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [Selecting the Right Texas Instruments Signal Switch](#) (SZZA030 - Updated: 09/07/2001)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
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[▲Back to Top](#)

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- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

[▲Back to Top](#)

- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

PRICING/AVAILABILITY/PKG

[▲Back to Top](#)

DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 08:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 08:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
5962-8606101EA	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 2.16	1	542*	>10k 20 May	8 WKS	EBV Elektronik Europe	64	BUY NOW
CD54HC157F	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 1.40	1	1004*	>10k 20 May	8 WKS	None Reported View Distributors		
CD54HC157F3A	ACTIVE	CDIP (J) 16	-55 TO 125	5962-8606101EA	View Contents	1KU 2.16	1	441*	>10k 20 May	8 WKS	None Reported View Distributors		

Table Data Updated on: 4/17/2003