SN65HVD01 3.3V RS-485 with Flexible I/O Supply and Selectable Speed

1 Features

- Exceeds Requirements of TIA-485 Standard
- 1.65-V to 3.6-V Supply for Data and Enable Signals
- 3-V to 3.6-V Supply for Bus Signals
- SLR Pin Selectable Data Rates: 250 kbps or 20 Mbps
- 1/8th Unit Load to Support up to 256 Nodes on a Bus
- Small 3 mm x 3 mm SON Package
- Failsafe Receiver (Bus Open, Bus Shorted, Bus Idle)
- Operating Temperature Range: –40°C to 125°C
- Bus-Pin Protection More Than:
  - ± 15kV HBM Protection
  - ± 16kV IEC61000-4-2 Contact Discharge
  - ± 16kV IEC61000-4-2 Air Discharge
  - 4kV IEC61000-4-4 Fast Transient Burst

2 Applications

- Telecom Infrastructure
- High-Speed Data Links
- Low-Voltage µC Communication

3 Description

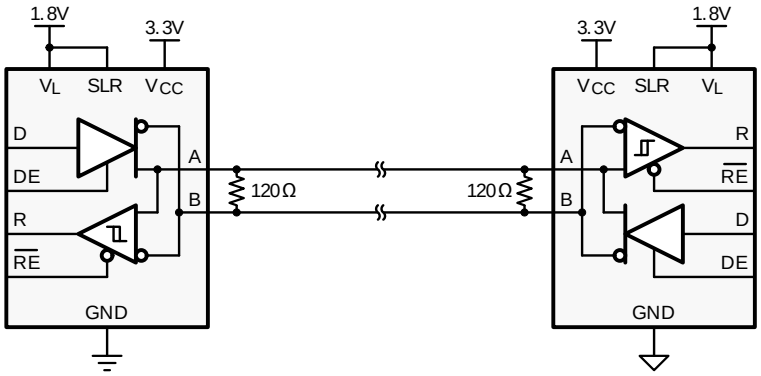
The SN65HVD01 is a low-power, 250 kbps or 20 Mbps data rate selectable RS-485 transceiver, utilizing a 1.65-V to 3.6-V supply for data and enable signals, and a 3.3 V ± 10% supply for bus signals. The device is designed for applications requiring synchronous (parallel transceiver) signal timing. On-chip transient suppression protects the device against destructive IEC 61000 ESD and EFT transients.

The device combines a differential driver and a differential receiver, connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making it suitable for multi-point applications over long cable runs. The SN65HVD01 is available in a tiny, 3 mm x 3 mm, SON package with operation characterized from -40°C to 125°C.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SN65HVD01DRC	SON (10)	3mm x 3mm

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2013) to Revision E	Page
• Changed the data sheet to the new TI standard layout	1
• Added the Device Information Table	1
• Added the Handling Ratings table	5
• Added the Detailed Description section	15
• Changed Figure 17	17
• Added the Applications and Implementation section	18
• Deleted the Application Information section	18
• Added the Power Supply Recommendations	21
• Added the Layout section	21

Changes from Revision C (November 2013) to Revision D **Page**

- Changed Feature From: Small 3 mm x 3 mm VQFN Package To: Small 3 mm x 3 mm SON Package 1
- Changed Feature From: Bus-Pin Protection: To: Bus-Pin Protection More Than: 1
- Changed Feature From: ≤ 15kV To: ±15 kV HBM Protection 1
- Changed Feature From: ≤ 15kV To: ±16 kV Contact Discharge 1
- Changed Feature From: ≤ 15kV To: ±16 kV Air Discharge 1
- Changed DESCRIPTION text From: 3 mm x 3 mm, VQFN package To: 3 mm x 3 mm, SON package 1
- Changed the ABSOLUTE MAXIMUM RATINGS for IEC 61000-4-2 ESD (Air-Gap Discharge) From MAX = ±15 To: MAX = ±16 5
- Changed the ABSOLUTE MAXIMUM RATINGS for IEC 61000-4-2 ESD (Contact Discharge) From MAX = ±15 To: MAX = ±16 5
- Changed the Thermal Information table package From VQFN (DRC) To; SON (DRC) 6

Changes from Revision B (October 2013) to Revision C **Page**

- Changed from Product Preview to Production Data 1

Changes from Revision A (October 2013) to Revision B **Page**

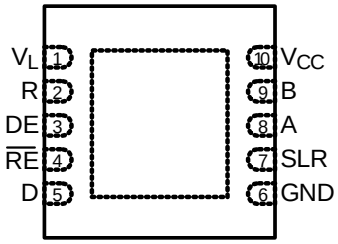
- Added 8 Typical Characteristics curves 9

Changes from Original (July 2013) to Revision A **Page**

- Changed Feature From: 1.8-V to 3.3-V Supply for Data and Enable Signals To: 1.65-V to 3.6-V Supply for Data and Enable Signals 1
- Changed Feature From: 3.3 V Supply for Bus Signals To: 3-V to 3.6-V Supply for Bus Signals 1
- Changed Feature From: Selectable Data Rates: 250 kbps or 20 Mbps To: SLR Pin Selectable Data Rates: 250 kbps or 20 Mbps 1
- Changed the list of APPLICATIONS 1
- Changed the DESCRIPTION 1
- Changed From: 100 Ω resistors To: 120 Ω resistors in the Typical Application circuit 1
- Changed the ELECTRICAL CHARACTERISTICS table values 7
- Changed the SWITCHING CHARACTERISTICS table values 8
- Changed V_{CC} and 3 V to V_L in Figure 9 through Figure 16 11
- Changed Figure 17 17

5 Terminal Configuration and Functions

DRC 10 TERMINAL
(TOP VIEW)



Terminal Functions

NAME	NO.	I/O	DESCRIPTION
V_L	1	Logic Supply	1.65 V to 3.6 V supply for logic I/O signals R, $\overline{RE}$, D, DE, and SLR)
R	2	Digital Output	Receive data output
DE	3	Digital Input	Driver enable input
$\overline{RE}$	4	Digital Input	Receiver enable input
D	5	Digital Input	Transmission data input
GND	6	Reference Potential	Local device ground
SLR	7	Digital Input	Slew rate select: Low = 20 Mbps, High = 250 kbps. Defaults to 20 Mbps if SLR is left floating
A	8	Bus I/O	Digital bus I/O, A
B	9	Bus I/O	Digital bus I/O, B
V_{CC}	10	Bus Supply	3 V to 3.6 V supply for A and B bus lines

6 Specifications

6.1 Absolute Maximum Ratings(1)

	VALUE		UNIT
	MIN	MAX	
Control supply voltage, V_L	–0.5	4	V
Bus supply voltage, V_{CC}	–0.5	5.5	V
Voltage range at A or B Inputs	–13	16.5	V
Input voltage range at any logic terminal	–0.3	5.7	V
Voltage input range, transient pulse, A and B, through 100Ω	–100	100	V
Receiver output current	–12	12	mA
Junction temperature, T_J		170	°C
Continuous total power dissipation	See the Thermal Information table		

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	150	°C
V_{ESD}	IEC 60749-26 ESD (Human Body Model), bus terminals and GND		±15	kV
	IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND (1)		±16	kV
	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND		±16	kV
	IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND		±4	kV
	JEDEC Standard 22, Test Method A114 (Human Body Model), all terminals		±8	kV
	JEDEC Standard 22, Test Method C101 (Charged Device Model), all terminals		±1.5	kV

(1) As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_L	Control supply voltage		1.65		3.6	V
V_{CC}	Bus supply voltage		3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode) (1)		–7		12	V
V_{IH}	High-level input voltage (Driver, driver enable, receiver enable inputs, and slew rate select)		0.7×V_L		V_L	V
V_{IL}	Low-level input voltage (Driver, driver enable, receiver enable inputs, and slew rate select)		0		0.3×V_L	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current	Driver	–80		80	mA
		Receiver	–2		2	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	SLR = '0'			20	Mbps
		SLR = '1'			250	kbps
T_A (2)	Operating free-air temperature Thermal Information		–40		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

6.4 Thermal Information

PARAMETER[1]		SON (DRC)	UNIT
Θ_{JA}	Junction-to-Ambient Thermal Resistance	41.4	°C/ W
$\Theta_{JC(top)}$	Junction-to-Case(top) Thermal Resistance	48.7	
Θ_{JB}	Junction-to-Board Thermal Resistance	18.8	
Ψ_{JT}	Junction-to-Top characterization parameter	0.6	
Ψ_{JB}	Junction-to-Board characterization parameter	19	
$\Theta_{JC(bottom)}$	Junction-to-Case(bottom) Thermal Resistance	3.7	
T_{TSD}	Thermal Shut-down junction temperature	170	°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953

6.5 Dissipation Ratings

PARAMETER			TEST CONDITIONS		VALUE	UNIT
PD	Power Dissipation driver and receiver enabled, $V_{CC} = V_L = 3.6$ V, $T_J = 150$°C, 50% duty cycle square-wave signal at signaling rate	Unterminated	$R_L = 300\ \Omega$, $C_L = 50$ pF (driver)	250 kbps	125	mW
				20 Mbps	175	
		RS-422 load	$R_L = 100\ \Omega$, $C_L = 50$ pF (driver)	250 kbps	165	mW
				20 Mbps	215	
		RS-485 load	$R_L = 54\ \Omega$, $C_L = 50$ pF (driver)	250 kbps	200	mW
				20 Mbps	250	

6.6 Electrical Characteristics

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V		See Figure 9	1.5	2		V
		R_L = 54 Ω (RS-485)		See Figure 10	1.5	2		V
		R_L = 100 Ω (RS-422) $T_J \geq 0°C$, $V_{CC} \geq 3.2V$			2			V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF			–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors			1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage					500		mV
C_{OD}	Differential output capacitance					15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				See (1)	–60	–20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold				–200	–130	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$)				40	70		mV
V_{OH}	Receiver high-level output voltage	V_L = 1.65 V, I_{OH} = -2 mA			1.3	1.45		V
		V_L = 3 V, I_{OH} = -2 mA			2.8	2.9		
V_{OL}	Receiver low-level output voltage	V_L = 1.65 V, I_{OL} = 2 mA				0.2	0.35	V
		V_L = 3 V, I_{OL} = 2 mA				0.1	0.2	
I_I	Driver input, driver enable, and receiver enable input current				–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_L, $\overline{RE}$ at V_L			–1		1	µA
I_{OS}	Driver short-circuit output current				–150		150	mA
I_I	Bus input current (disabled driver)	V_L = 1.8 V, V_{CC} = 3.3 V, DE at 0 V	V_I = 12 V			85	125	µA
			V_I = –7 V		–100	–60		µA
I_{CC}	Supply current (quiescent)	Driver and Receiver enabled	DE=V_L, RE = GND, No load			750	1100	µA
				$T_J \leq 85°C$			1000	µA
		Driver enabled, receiver disabled	DE=V_{CC}, $\overline{RE}$ = V_L, No load			350	650	µA
		Driver disabled, receiver enabled	DE=GND, $\overline{RE}$ = GND, No load			650	800	µA
		Driver and receiver disabled	DE=GND, $\overline{RE}$ = V_L, No load			0.1	5	µA
	Supply current (dynamic)	See the Typical Characteristics section						

(1) Under any specific conditions, V_{IT+} is specified to be at least V_{HYS} higher than V_{IT-}.

6.7 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER, SLR = '1', 250 kbps, bit time ≥ 4 µs							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 11	0.4	0.8	1.2	µs
t_{PHL}, t_{PLH}	Driver propagation delay			0.4	0.8	1.2	µs
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0.2	µs
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 12 and Figure 13		0.025	0.1	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.6	1	µs
		Receiver disabled			3.5	8	µs
DRIVER, SLR = '0', 20 Mbps, bit time ≥ 50 ns							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 11	5	10	15	ns
t_{PHL}, t_{PLH}	Driver propagation delay			6	15	25	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					4	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 12 and Figure 13		20	35	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			14	30	ns
		Receiver disabled			3	7	µs
RECEIVER, SLR = 'X'							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF	See Figure 14		5	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			30	60	90	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				10	20	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 15		15	80	ns
		Driver disabled	See Figure 16		3	8	µs

6.8 Typical Characteristics

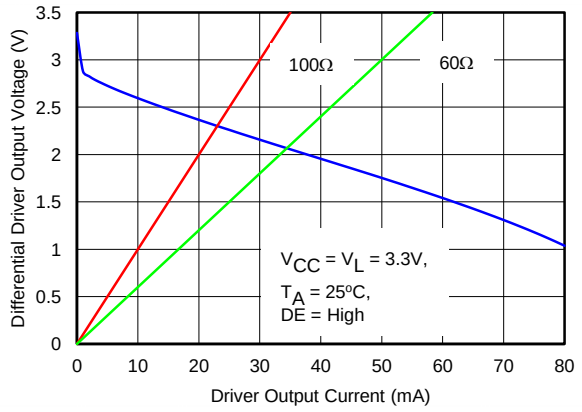


Figure 1. Differential Driver Output Voltage vs Driver Output Current

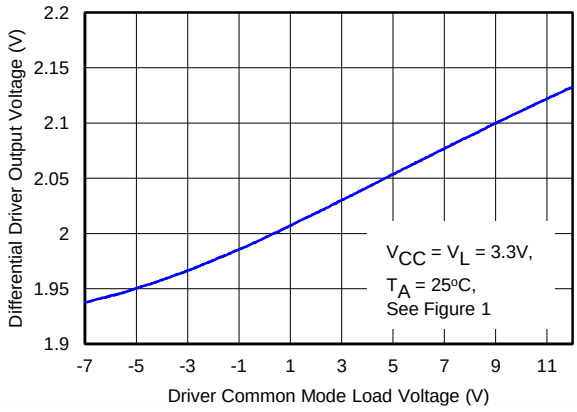


Figure 2. Differential Driver Output Voltage vs Driver Common Mode Load Voltage

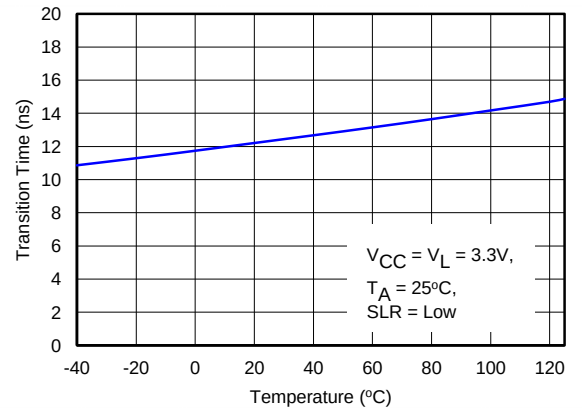


Figure 3. Transition Time vs Temperature

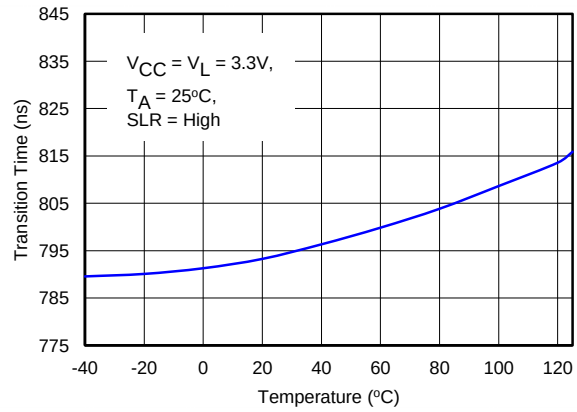


Figure 4. Transition Time vs Temperature

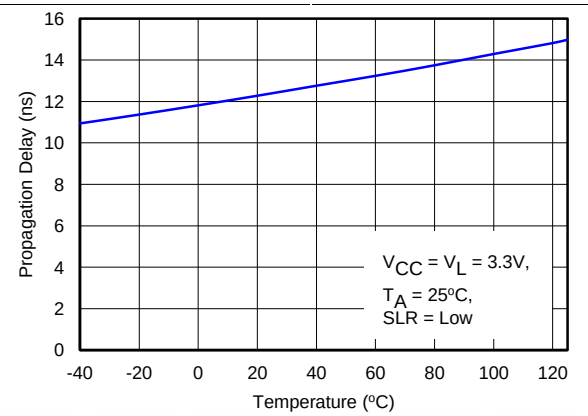


Figure 5. Propagation Delay vs Temperature

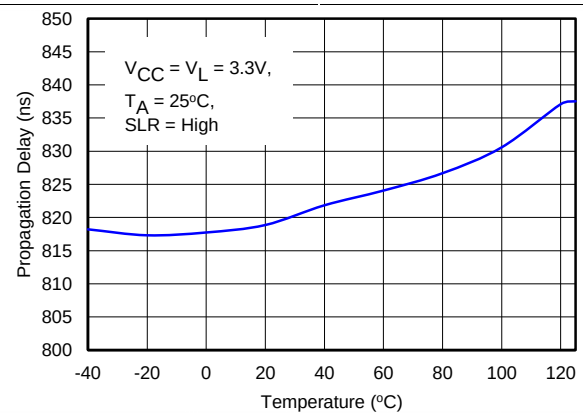


Figure 6. Propagation Delay vs Temperature

Typical Characteristics (continued)

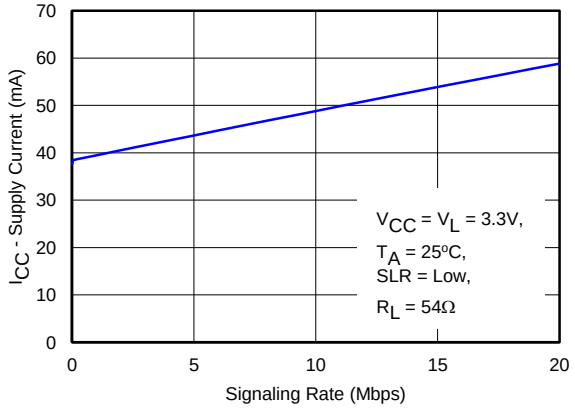


Figure 7. Supply Current vs Signaling Rate

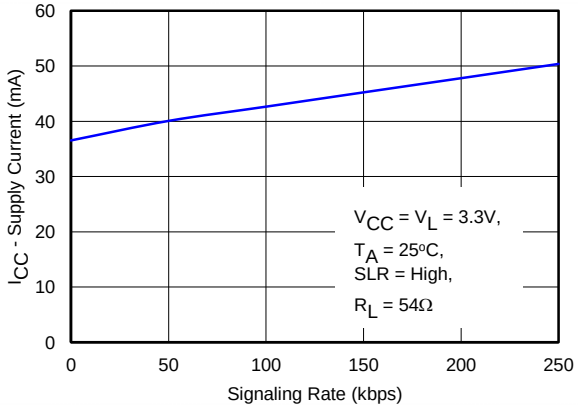


Figure 8. Supply Current vs Signaling Rate

7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec.

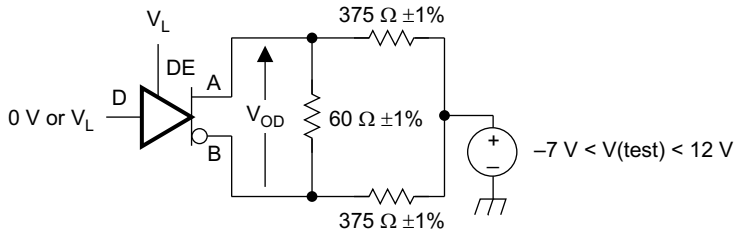


Figure 9. Measurement of Driver Differential Output Voltage with Common-Mode Load

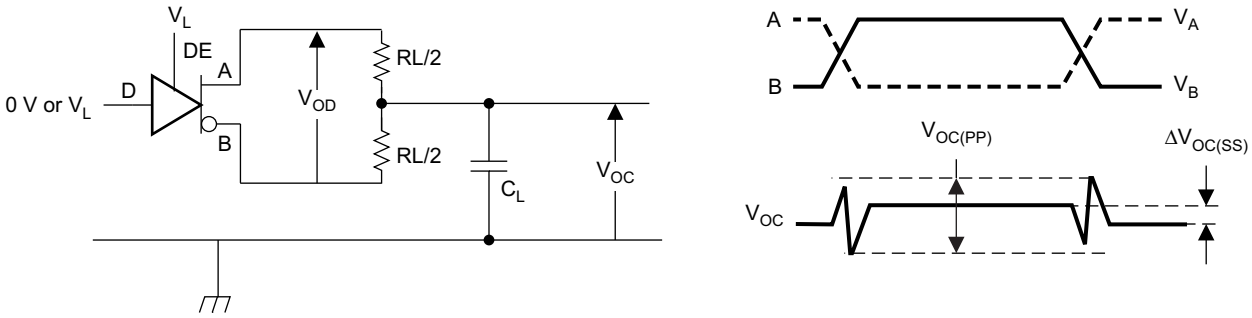


Figure 10. Measurement of Driver Differential and Common-Mode Output with RS-485 Load

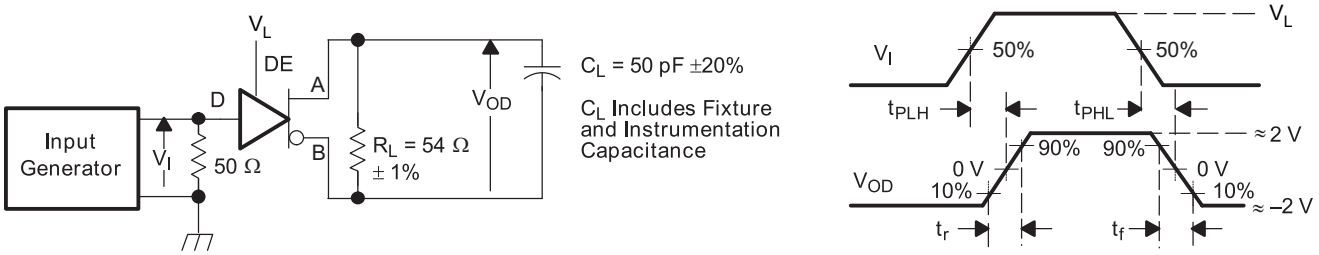
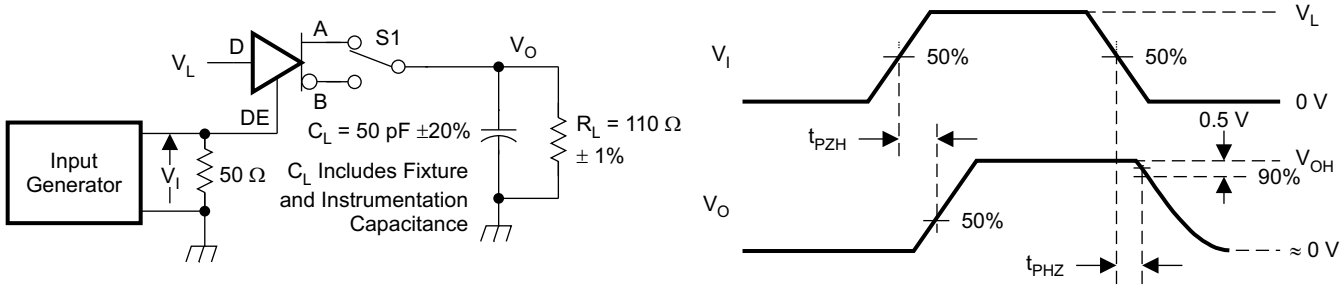


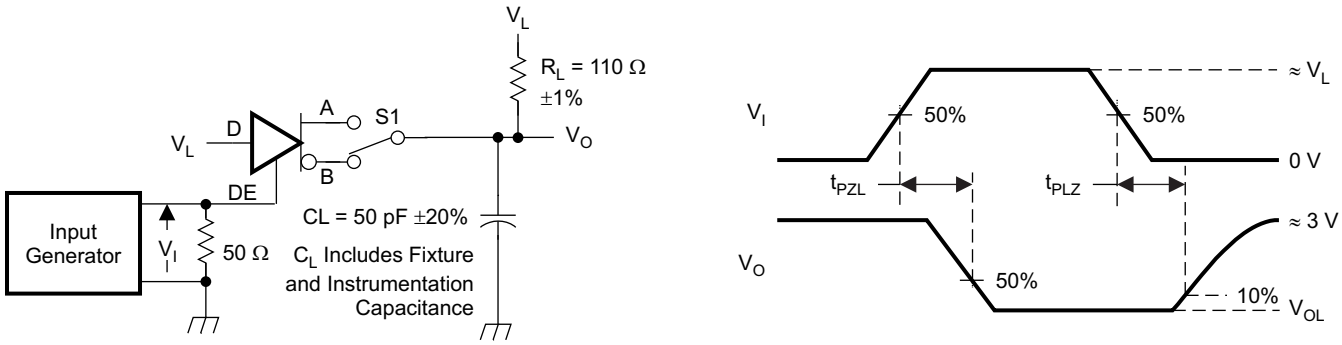
Figure 11. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at V_L to test non-inverting output, D at 0 V to test inverting output.

Figure 12. Measurement of Driver Enable and Disable Times with Active High Output and Pull-Down Load

Parameter Measurement Information (continued)



D at 0V to test non-inverting output, D at V_L to test inverting output.

Figure 13. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-Up Load

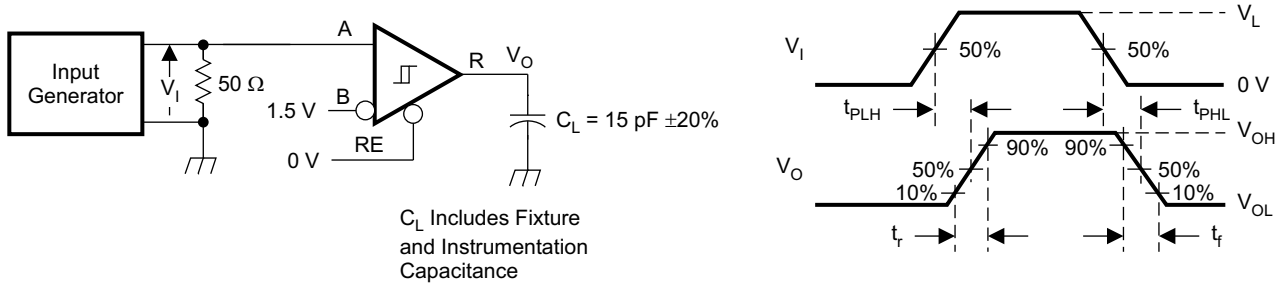


Figure 14. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)

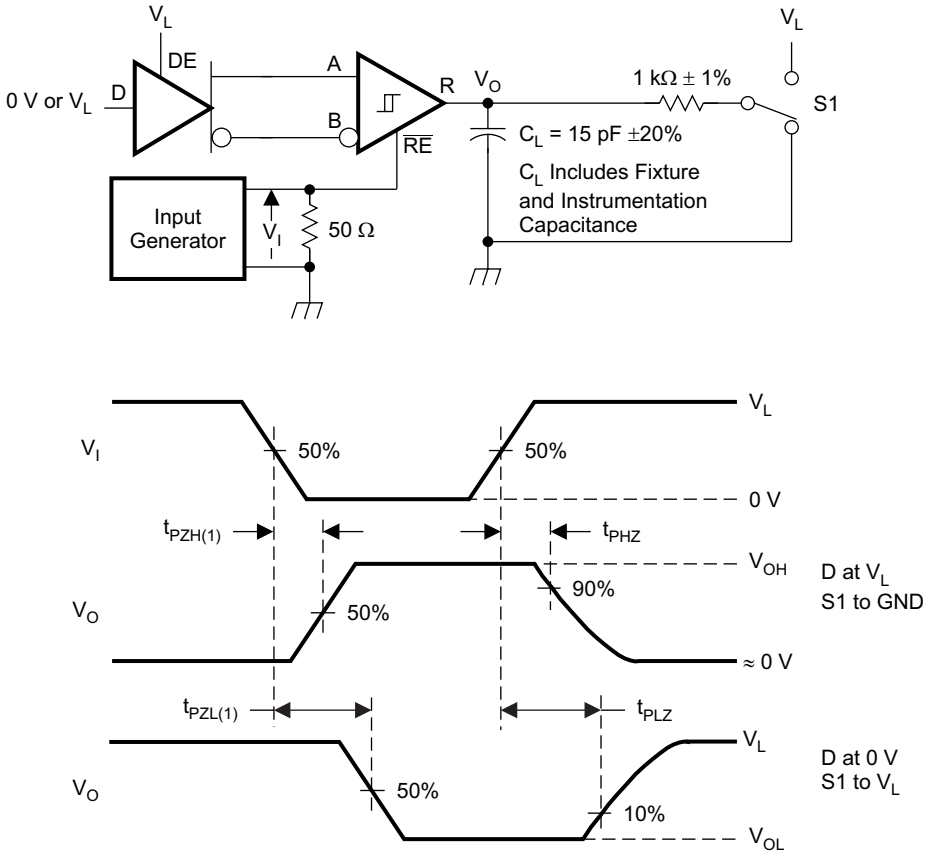


Figure 15. Measurement of Receiver Enable/Disable Times with Driver Enabled

Parameter Measurement Information (continued)

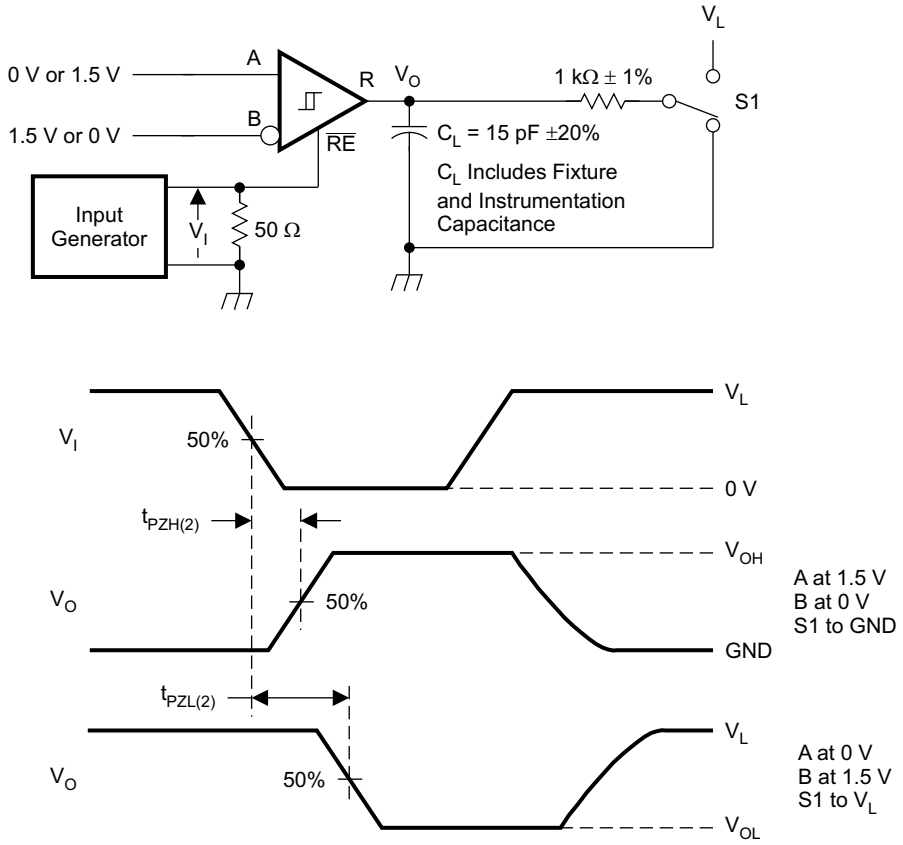


Figure 16. Measurement of Receiver Enable Times with Driver Disabled

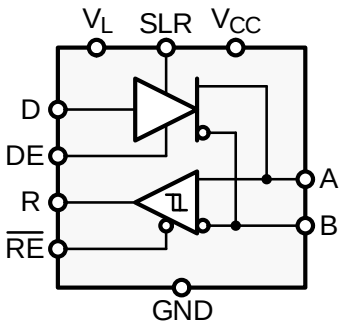
8 Detailed Description

8.1 Overview

The SN65HVD01 is a low-power, half-duplex RS-485 transceiver whose maximum data rate can be set to either 250 kbps or 20 Mbps via a selection terminal, SLR.

The device possesses two power supply inputs, one for logic control functions, V_L, and the other for the bus supply, V_{CC}. V_L can range from 1.65 V minimum up to 3.6 V maximum and allows for the direct interface to low-voltage FPGAs and micro controllers. V_{CC} requires a supply between 3 V to 3.6 V to assure sufficient output drive capability across a wide common-mode range.

8.2 Functional Block Diagram



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic discharges (ESD) according to IEC61000-4-2 of up to ±16 kV, and against electrical fast transients (EFT) according to IEC61000-4-4 of up to ±4 kV.

The SN65HVD01 provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –60 mV and an input hysteresis of VHYS = 70 mV, the receiver output remains logic high even in the presence of 130 mV_{PK} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide temperature range from –40°C to 125°C.

8.4 Device Functional Modes

When driver enable terminal, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE terminal has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D terminal has an internal pull-up resistor to V_L, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

When the receiver enable terminal, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Connecting SLR to V_L limits the maximum data rate to 250 kbps and increases the driver rise and fall times to 800 ns. Connecting SLR to GND increases the upper data rate limit to 20 Mbps and reduces the driver rise and fall times to 10 ns.

Table 3. SLR-Terminal Configuration

SLR-INPUT	DATA RATE	TYP tr / tf
V_L	250 kbps	800 ns
GND or OPEN	20 Mbps	10 ns

8.4.1 Equivalent Input and Output Schematic Diagrams

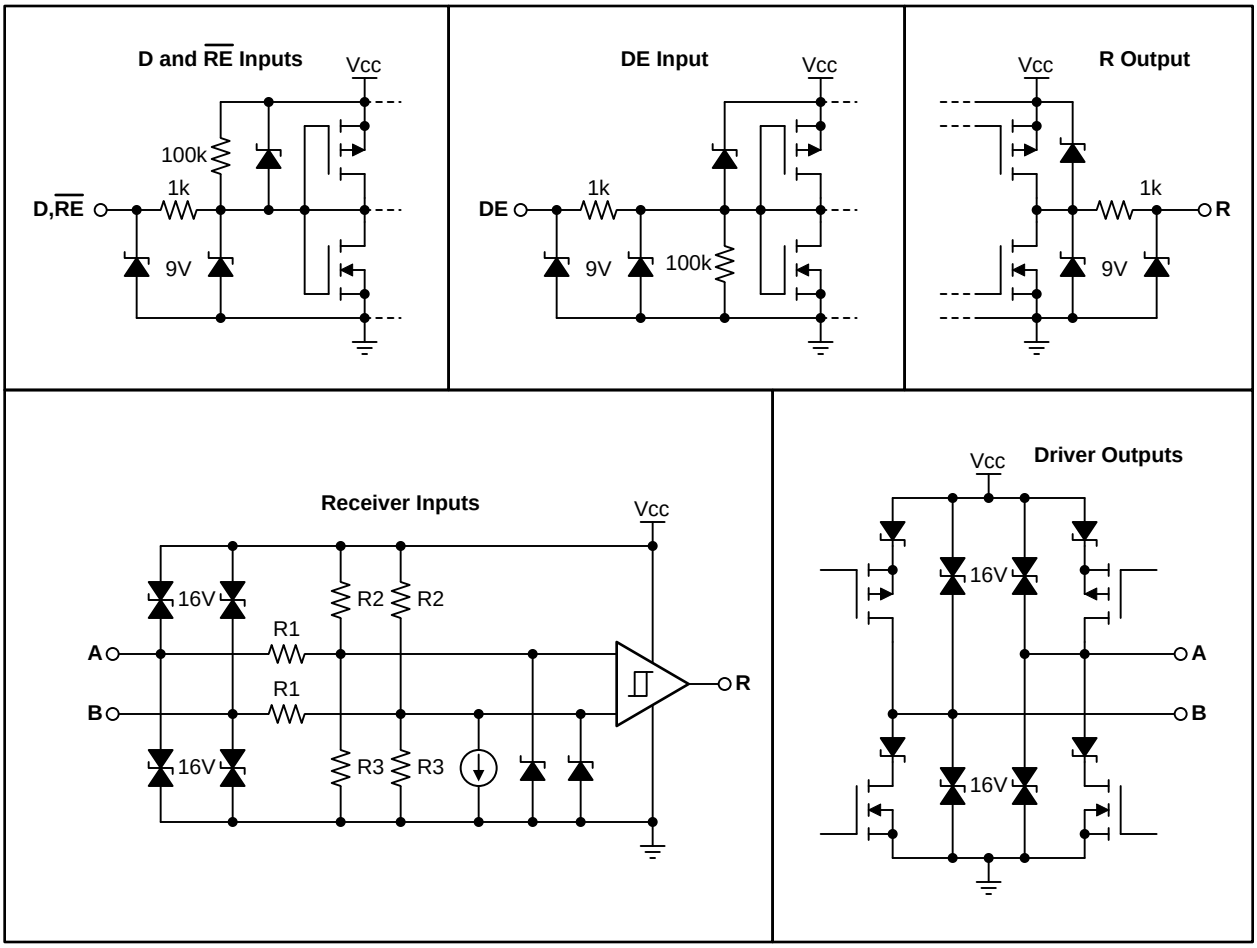
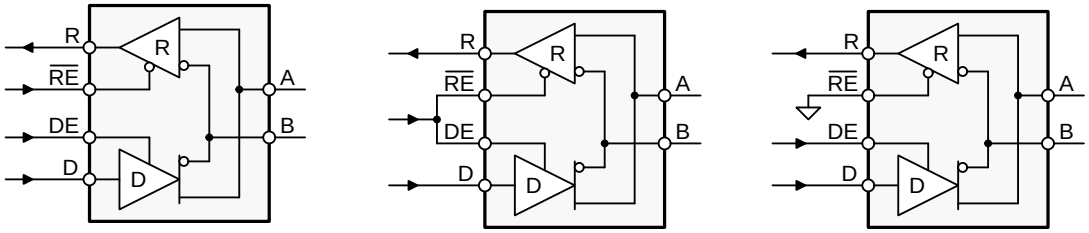


Figure 17. Equivalent Input and Output Schematic Diagrams

9 Applications and Implementation

9.1 Application Information

The SN65HVD01 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable terminals allow for the configuration of different operating modes.



a) *Independent driver and receiver enable signals*

b) *Combined enable signals for use as directional control pin*

c) *Receiver always on*

Figure 18. SN65HVD01 Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction- control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration, a node not only receives the data from the bus but also the data it sends and thus can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

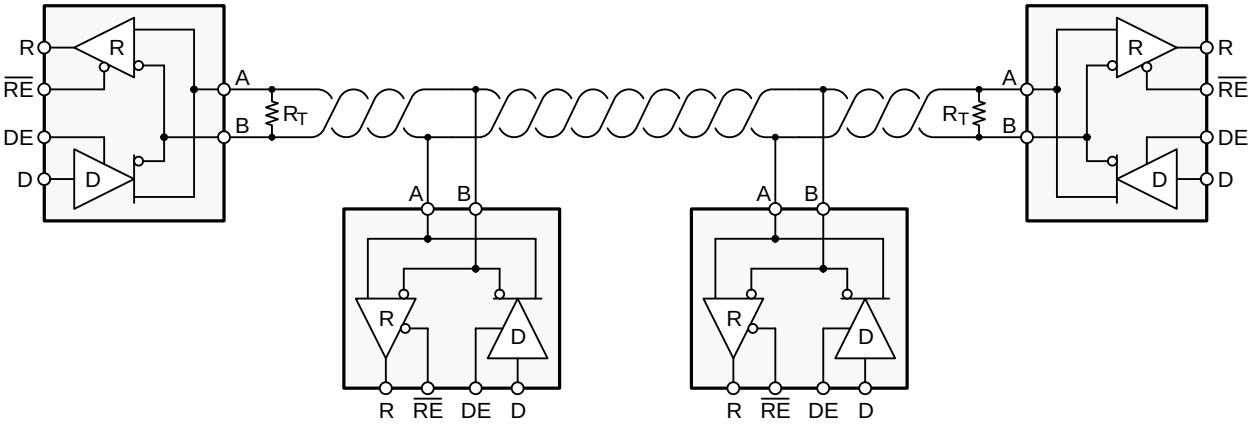


Figure 19. Typical RS-485 Network with SN65HVD01 Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Typical Application (continued)

9.2.1.1 Data Rate and Bus Length

The maximum bus length is limited by the transmission line losses and the signal jitter at a given data rate. Because data reliability sharply decreases for a jitter of 10% or more of the baud period, Figure 20 shows the cable length versus data rate characteristic of a conventional RS-485 cable for signal jitter of 10%.

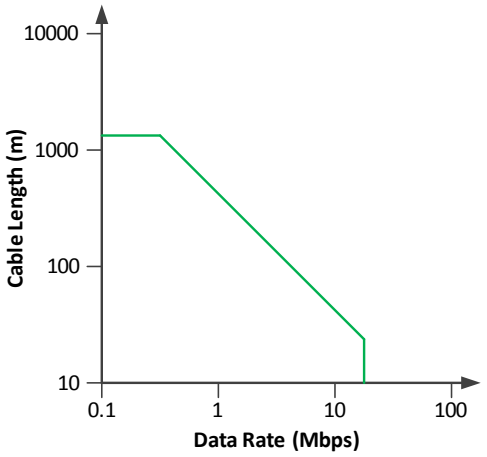


Figure 20. Cable Length vs Data Rate

9.2.1.2 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the SN65HVD01 is a 1/8 UL transceiver, it is possible to connect up to 256 devices to the bus.

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. Figure 21 suggests a protection circuit against 10 kV ESD, 4 kV EFT, and 1 kV surge transients.

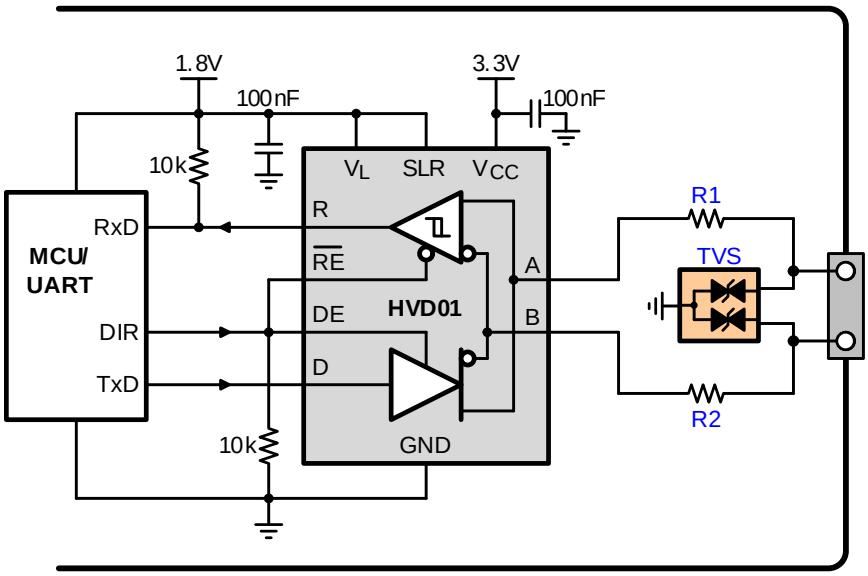


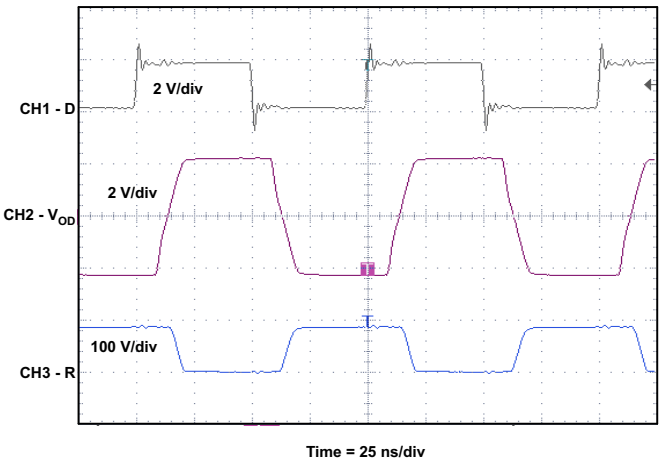
Figure 21. Transient Protection Against ESD, EFT, and Surge Transients

Typical Application (continued)

Table 4. Recommended Materials

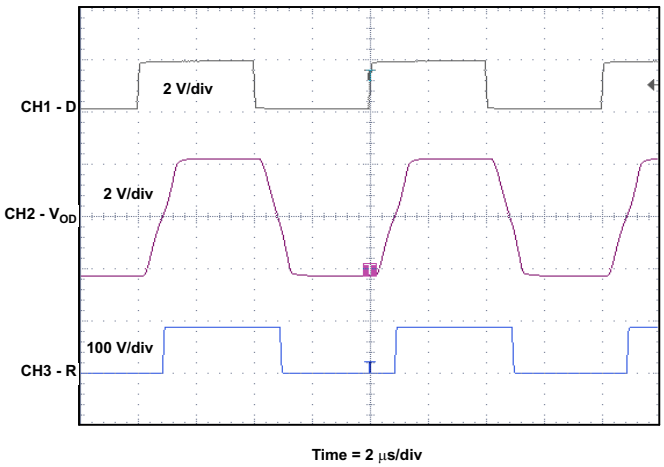
Device	Function	Order Number
XCVR	3.3V, 250kbps RS-485 Transceiver	SN65HVD01D
R1,R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712

9.2.3 Application Performance Curves



V_{CC} = 3.3 V V_L = 1.8 V SLR = GND

Figure 22. V_{OD} and R Transient Response - 20 Mbps



V_{CC} = 3.3 V V_L = 1.8 V SLR = V_L

Figure 23. V_{OD} and R Transient Response - 250 kbps

10 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100 nF ceramic capacitor located as close to the supply terminals as possible. Linear voltage regulators for the 1.8 V logic and 3.3 V bus supplies are TPS76318 and TPS76333 respectively.

11 Layout

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

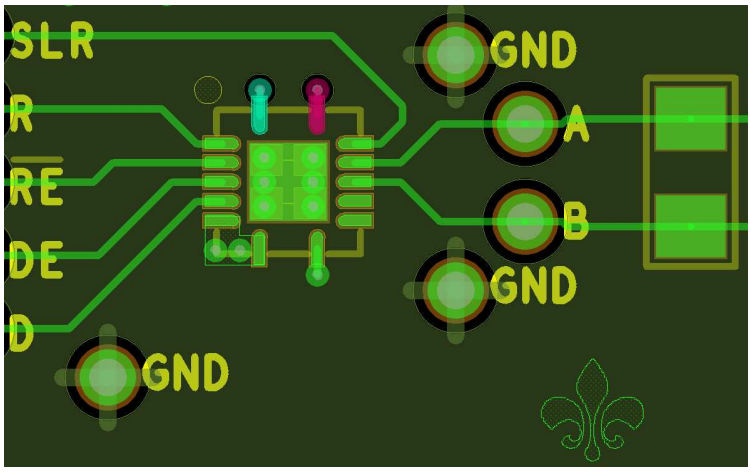
Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

11.1 Layout Guidelines

- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100 nF to 220 nF bypass capacitors as close as possible to the V_{CC} terminals of transceiver, UART, controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in theses lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD01DRCR	ACTIVE	SON	DRC	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD01	Samples
SN65HVD01DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD01	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

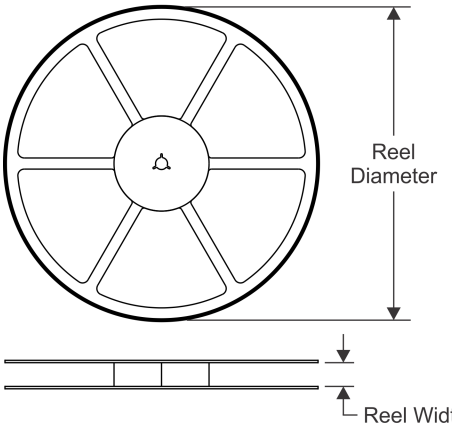
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

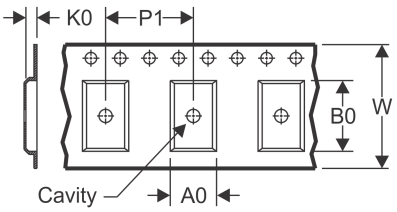
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

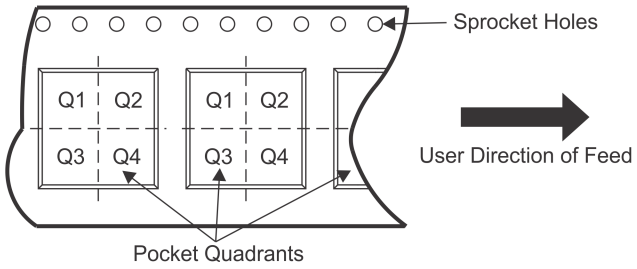


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

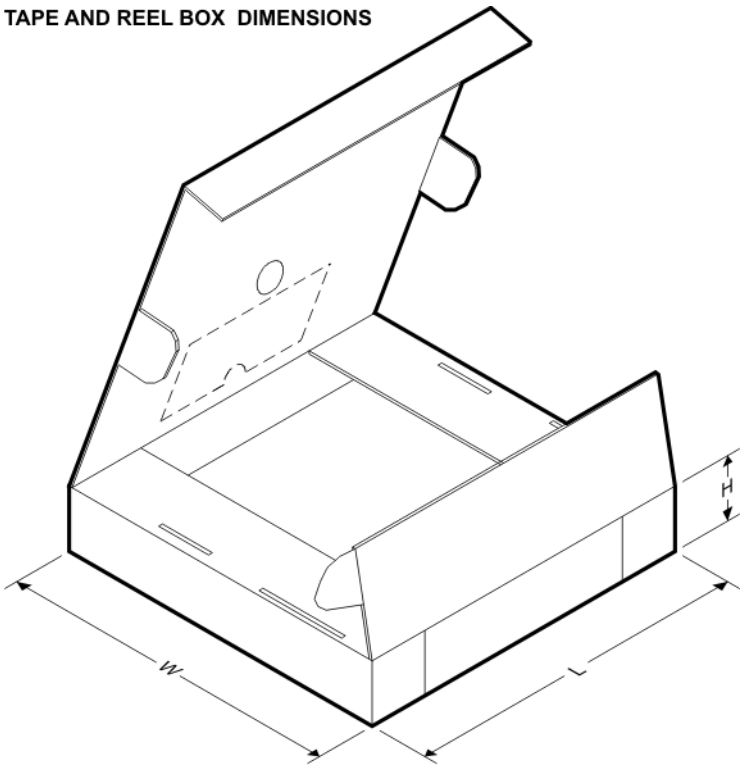
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD01DRCR	SON	DRC	10	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD01DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

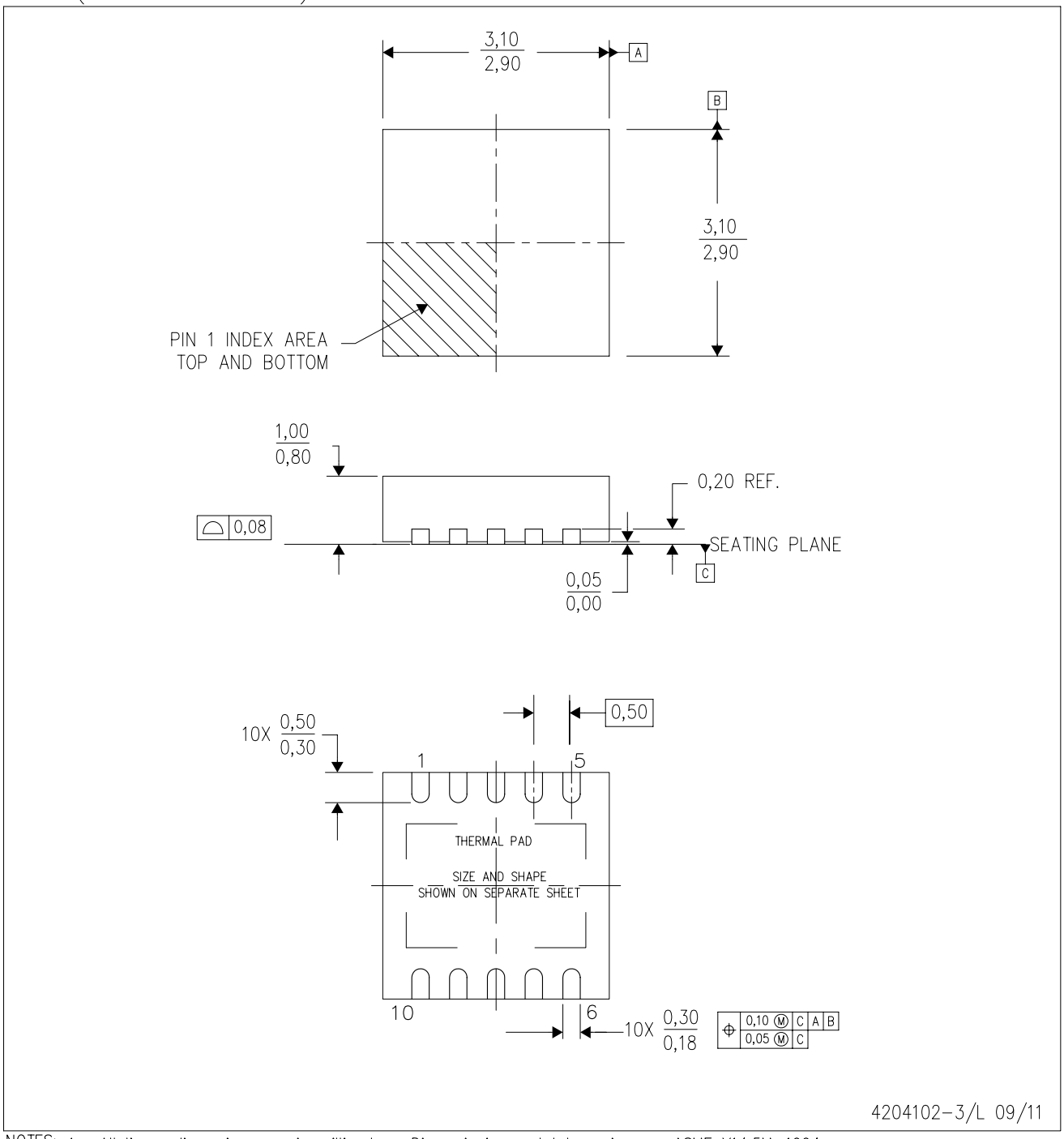
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD01DRCR	SON	DRC	10	2500	367.0	367.0	35.0
SN65HVD01DRCT	SON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

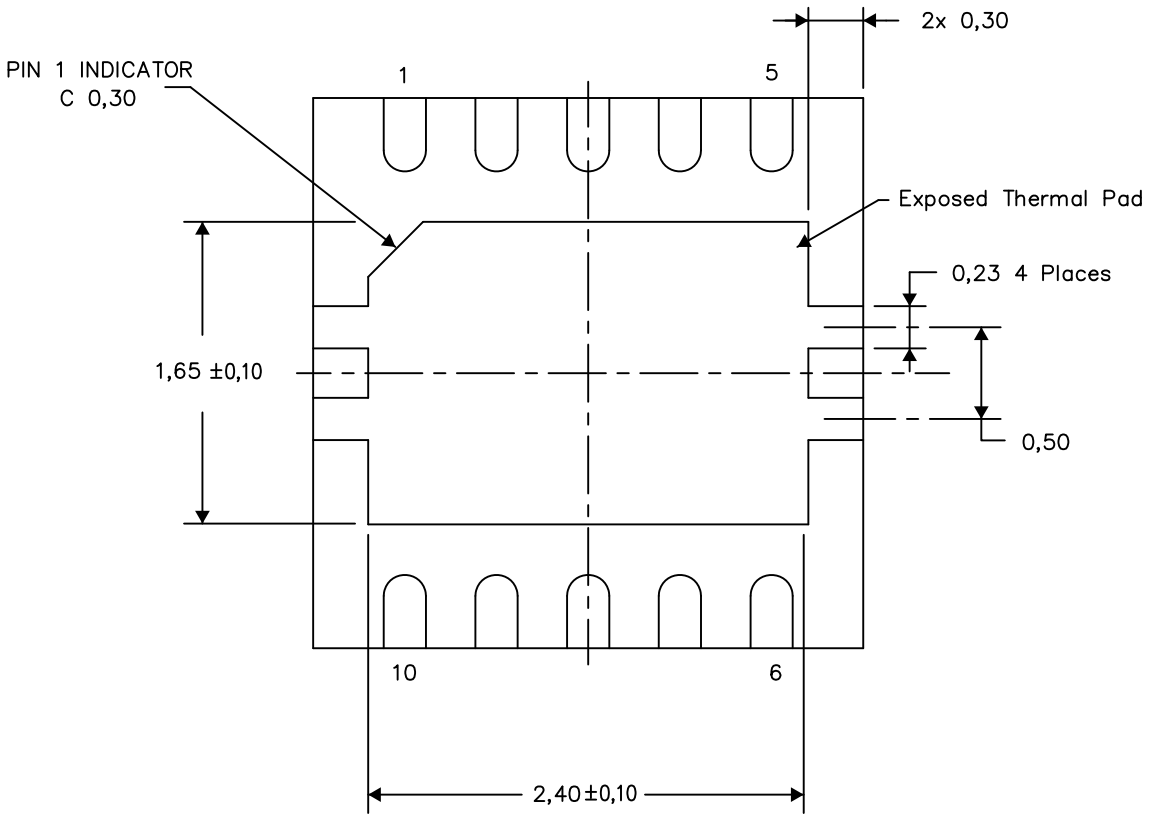
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



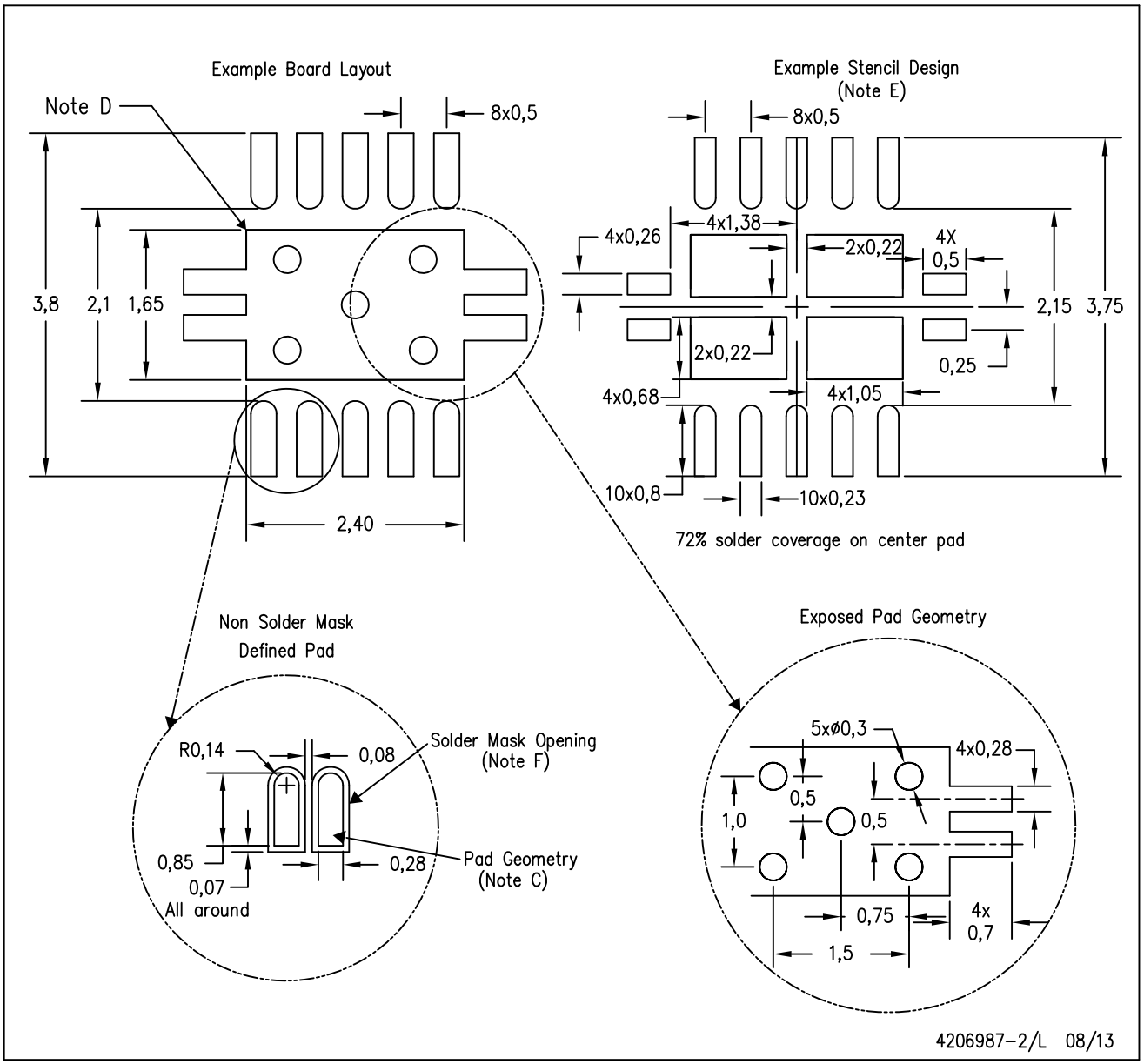
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/S 07/13

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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