CD54HC85/3A
CD54HCT85/3A

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

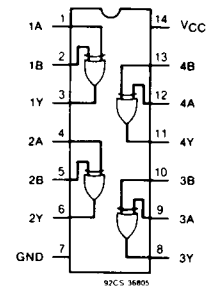
Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT85	5-7	1-4,8-15	16	5-7	8	1-4,9-16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT85	—	1,8,10,11,13	5-7	2-4,16	12,15	9,14

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54HC86/3A
CD54HCT86/3A

Quad 2-Input EXCLUSIVE-OR Gate

The RCA-CD54HC86 and CD54HCT86 contain four independent EXCLUSIVE-OR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-OR function.



FUNCTIONAL DIAGRAM

Package Specifications
See Section 11, Fig. 10

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	2•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	40•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All Inputs	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54HC86/3A
CD54HCT86/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-55°C to +125°C				UNITS
			HC		HCT		54HC		54HCT		
		V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay nA, nB to nY	t_{PLH} t_{PHL}	2	—	120	—	—	—	180	—	—	ns
		4.5	—	24•	—	32•	—	36•	—	48•	
		6	—	20	—	—	—	31	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT86	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT86	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

4-Bit Binary Ripple Counter

CD54HC93/3A
CD54HCT93/3A

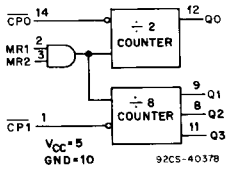
The RCA-CD54HC93 and the CD54HCT93 are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These four-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Qn outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR1 and MR2) is provided which overrides both clocks and resets (clears) all flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a four-bit ripple counter the output Q0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q0, Q1, Q2, and Q3 outputs as shown in the function table. As a three-bit ripple counter, the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q1, Q2, and Q3 outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the three-bit ripple-through counter.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 10