National Semiconductor

DM54ALS112A/DM74ALS112A Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS112A is a dual edge-triggered flip-flop. Each flip flop has individual J, K, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The JK design allows operation as a D flip flop by tying the J and K inputs together.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS112 at Approximately Half the Power.

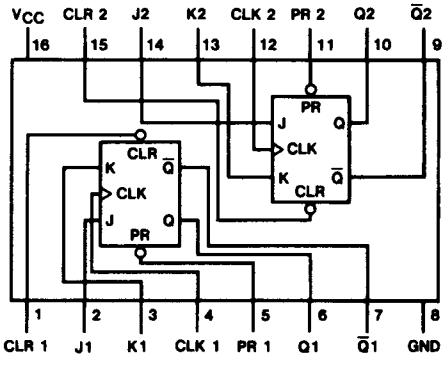
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



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54ALS112A (J) **74ALS112A (J, N)**

Function Table

Inputs					Outputs	
PR	CLR	CK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	H	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↓ = Negative Edge Transition, Q_0 = Previous Condition of Q

* This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54ALS112A			DM74ALS112A			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, fCLOCK		0		25	0		30	MHz
Pulse Width T_W	Clock High	20			16.5			ns
	Clock Low	20			16.5			ns
Pulse Width T_W, Preset or Clear Low		15			10			ns
Data Setup Time, T_{SU}	J or K	25↓			22↓			ns
	PRE or CLR inactive	22↓			20↓			
Data Hold Time, T_H		0↓			0↓			ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage		$I_{OH} = -0.4$ mA $V_{CC} = 4.5$ to 5.5V		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
				74ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$	J, K, CLK			0.1	mA
				$\overline{PRE}$ or $\overline{CLR}$			0.2	
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
		Preset, Clear					40	
I_{IL}	Low Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
		Preset, Clear					−0.4	
I_O	Output Drive Current		$V_{CC} = 5.5V$ $V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$			2.5	4.5	mA

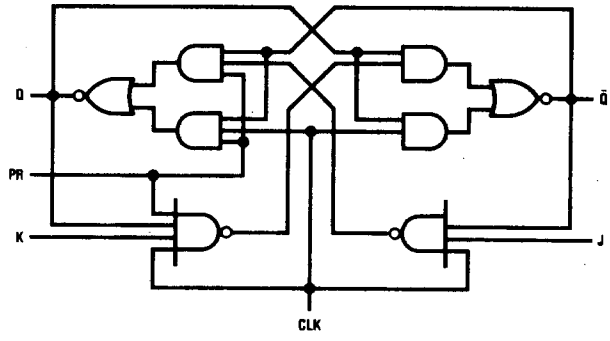
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS112A			DM74ALS112A			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3		20	3		15	ns
T_{PHL}				4		22	4		18	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3		18	3		15	ns
T_{PHL}				5		23	5		19	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



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