Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

PRELIMINARY
IDT 7381
IDT 7383

T-49-11

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- IDT7381:
  - 54/74S381 instruction set (8 functions)
  - Replaces Gould S614381 or Logic Devices L4C381
  - Cascadable with or without carry look-ahead
- IDT7383:
  - 32 advanced ALU functions
- — Cascadable without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 68-lead PGA and 68-pin surface mount PLCC, LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7381 and IDT7383 are high-speed cascadable Arithmetic Logic Units (ALUs). Both three-bus devices have two input registers, ultra-fast 16-bit ALUs and 16-bit output registers. With IDT's high-performance CEMOS technology, the IDT7381/7383 can do arithmetic or logic operations in 20ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry out, propagate and generate outputs for cascading using carry look-ahead.

The IDT7383 has five function pins to select 1 of 32 arithmetic or logic operations and the R, S input selections to the ALU. The R and S ALU inputs can be A, B, F, 0 or all 1s. This ALU has a carry out pin for cascading.

The IDT7381 and IDT7383 are available in 68-pin PLCC, LCC or PGA packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high reliability systems.

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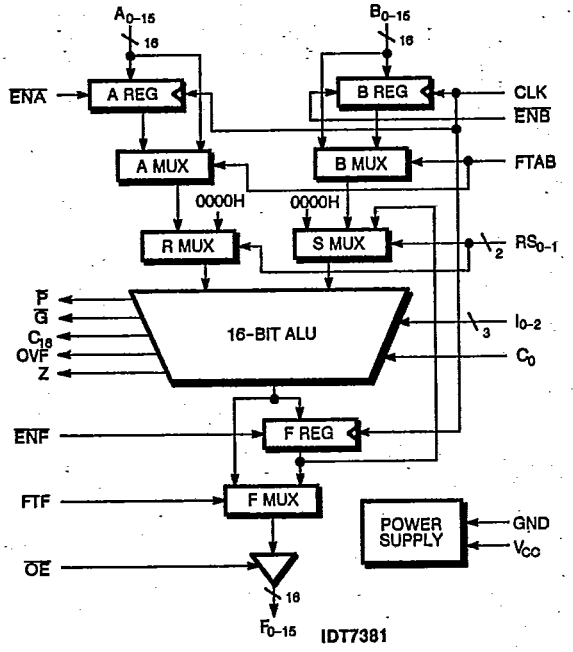
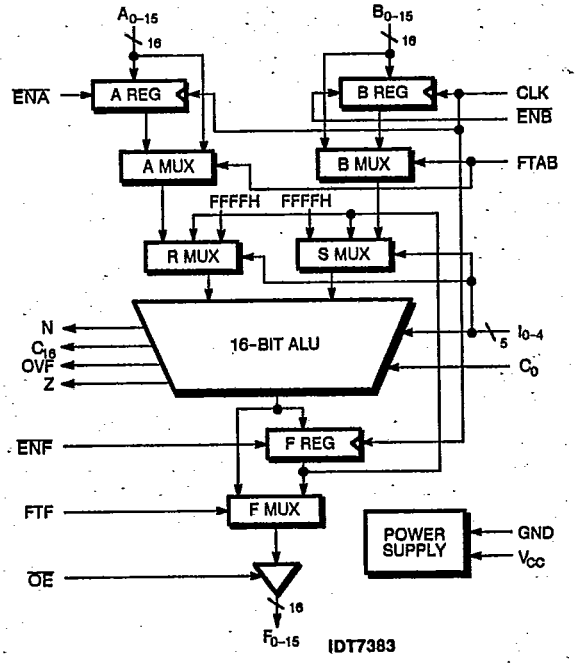
FUNCTIONAL BLOCK DIAGRAM



IDT7381



IDT7383

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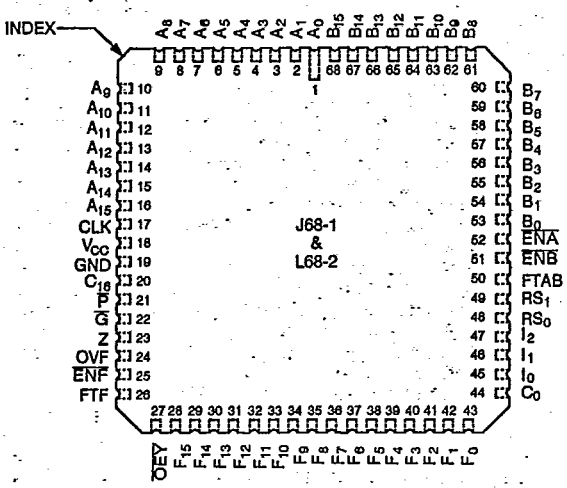
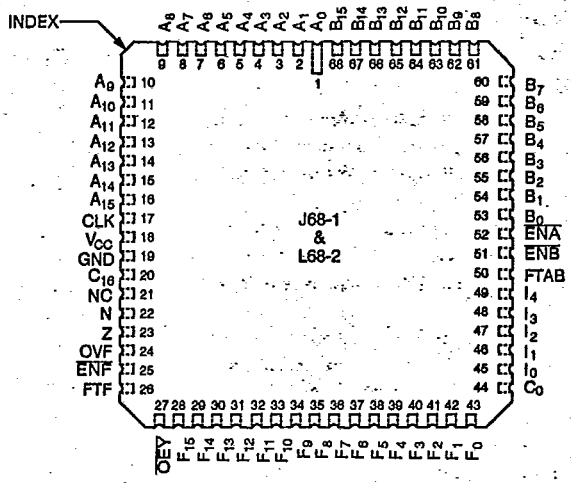
PIN CONFIGURATIONS

IDT7381

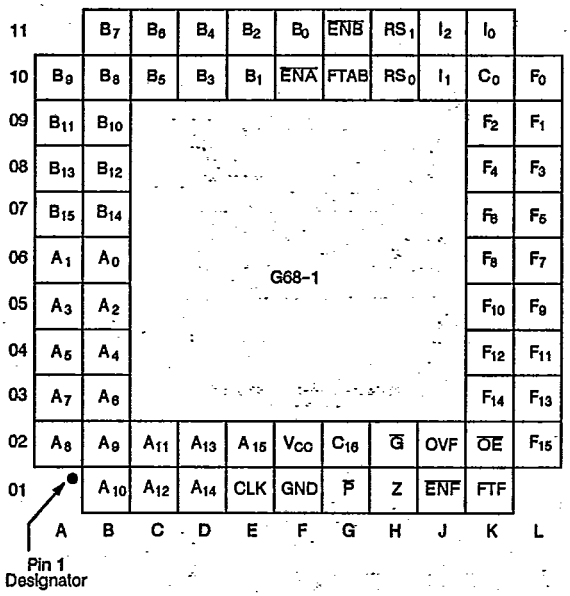


PLCC/LCC
TOP VIEW

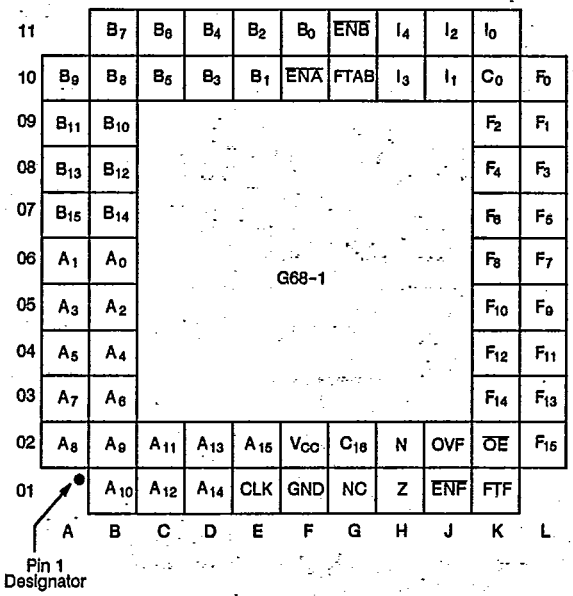
IDT7383



PLCC/LCC
TOP VIEW



PGA
TOP VIEW



PGA
TOP VIEW

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PIN DESCRIPTIONS

IDT7381 AND IDT7383 PINS

PIN NAME	I/O	DESCRIPTION
$A_0 - A_{15}$	I	Sixteen-bit data input port.
$B_0 - B_{15}$	I	Sixteen-bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow-through control pin. When this pin is high, both register A and B are transparent.
$F_0 - F_{15}$	O	Sixteen-bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow-through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascaded configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow.
Z	O	This pin indicates a zero output result.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V.

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IDT7381 PINS

PIN NAME	I/O	DESCRIPTION
$RS_0 - RS_1$	I	Two control pins used to select input operands for the R and S multiplexers.
$I_0 - I_2$	I	Three control pins to select the ALU function performed.
$\overline{P}$	O	Indicates the carry propagate output state of the ALU.
$\overline{G}$	O	Indicates the carry generate output state of the ALU.

IDT7381 R AND S MUX TABLE

RS_1	RS_0	R MUX	S MUX
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

IDT7381 ALU FUNCTION TABLE

I_2	I_1	I_0	FUNCTION
0	0	0	F = 0
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

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PIN DESCRIPTIONS (Continued)

IDT7383 PINS

PIN NAME	I/O	DESCRIPTION
$I_0 - I_4$	I	Five control pins to select the ALU function performed.
N	O	The sign bit of an ALU operation.

IDT7383 ALU FUNCTION TABLE

I_4	I_3	I_2	I_1	I_0	FUNCTION
0	0	0	0	0	$F = A + B + C_0$
0	0	0	0	1	F = A or B
0	0	0	1	0	$F = A + \overline{B}$ or C_0
0	0	0	1	1	$F = \overline{A} + B + C_0$
0	0	1	0	0	$F = A + C_0$
0	0	1	0	1	$F = \overline{A}$ or F
0	0	1	1	0	$F = A - 1 + C_0$
0	0	1	1	1	$F = \overline{A} + C_0$
0	1	0	0	0	$F = A + F + C_0$
0	1	0	0	1	F = A or F
0	1	0	1	0	$F = A + \overline{F} + C_0$
0	1	0	1	1	$F = \overline{A} + F + C_0$
0	1	1	0	0	$F = F + B + C_0$
0	1	1	0	1	$F = \overline{A}$ or B
0	1	1	1	0	$F = F + \overline{B} + C_0$
0	1	1	1	1	$F = \overline{F} + B + C_0$
1	0	0	0	0	F = A xor B
1	0	0	0	1	F = A and B
1	0	0	1	0	$F = \overline{A}$ and B
1	0	0	1	1	F = A xnor B
1	0	1	0	0	F = A xor F
1	0	1	0	1	F = A and F
1	0	1	1	0	$F = \overline{A}$ and F
1	0	1	1	1	F = all 1's
1	1	0	0	0	$F = B + C_0$
1	1	0	0	1	F = A and $\overline{B}$
1	1	0	1	0	$F = \overline{B} + C_0$
1	1	0	1	1	$F = B - 1 + C_0$
1	1	1	0	0	$F = F + C_0$
1	1	1	0	1	F = A or $\overline{B}$
1	1	1	1	0	$F = F - 1 + C_0$
1	1	1	1	1	$F = \overline{F} + C_0$

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V,	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
I_{CC}	Operating Power Supply Current	Outputs Open; f = 25 MHz	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	15	35	–	15	45	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq 0.2V$	–	2	10	–	2	15	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0mA	–	–	0.4	–	–	0.4	V

NOTE:

1. Typical implies V_{CC} = 5V, T_A = +25°C

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AC ELECTRICAL CHARACTERISTICS – COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

MAXIMUM COMBINATIONAL PROPAGATION DELAYS

FROM INPUT	TO OUTPUT								UNITS
	7381L20 7383L20		7381L25 7383L25		7381L40 7383L40		7381L55 7383L55		
	$F_0 - F_{15}$	FLAGS[2]	$F_0 - F_{15}$	FLAGS[2]	$F_0 - F_{15}$	FLAGS[2]	$F_0 - F_{15}$	FLAGS[2]	
FTAB = 0, FTF = 0									
CLK	9	18	11	23	18	36	25	50	ns
C_0	–	13	–	16	–	26	–	36	ns
$I_0 - I_4$, RS_0, RS_1[1]	–	18	–	23	–	36	–	50	ns
FTAB = 0, FTF = 1									
CLK	18	18	23	23	36	36	50	50	ns
C_0	14	13	18	16	28	26	39	36	ns
$I_0 - I_4$, RS_0, RS_1[1]	20	18	25	23	40	36	55	50	ns
FTAB = 1, FTF = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	–	16	–	20	–	32	–	44	ns
CLK	9	–	11	–	18	–	25	–	ns
C_0	–	13	–	16	–	26	–	36	ns
$I_0 - I_4$, RS_0, RS_1[1]	–	18	–	23	–	36	–	50	ns
FTAB = 1, FTF = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	17	16	21	20	34	32	47	44	ns
CLK	–	–	–	–	–	–	–	–	ns
C_0	14	13	18	16	28	26	39	36	ns
$I_0 - I_4$, RS_0, RS_1[1]	20	18	25	23	40	36	55	50	ns

MINIMUM SETUP AND HOLD TIMES RELATIVE TO CLOCK (CLK)

INPUT	7381L20 7383L20		7381L25 7383L25		7381L40 7383L40		7381L55 7383L55		UNITS
	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	
FTAB = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	4	0	5	0	8	0	11	0	ns
C_0	13	0	16	0	26	0	36	0	ns
$I_0 - I_4$, RS_0, RS_1[1]	19	0	24	0	38	0	52	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	4	0	5	0	8	0	11	0	ns
FTAB = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	20	0	25	0	40	0	55	0	ns
C_0	20	0	25	0	40	0	55	0	ns
$I_0 - I_4$, RS_0, RS_1[1]	20	0	25	0	40	0	55	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	–	–	–	–	–	–	–	–	ns

MINIMUM CLOCK CYCLE TIMES AND PULSE WIDTHS

PARAMETER	7381L20 7383L20	7381L25 7383L25	7381L40 7383L40	7381L55 7383L55	UNITS
Clock LOW Time	5	6	10	14	ns
Clock HIGH Time	5	6	10	14	ns
Clock Period	20	25	40	55	ns

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

PARAMETER	7381L20 7383L20	7381L25 7383L25	7381L40 7383L40	7381L55 7383L55	UNITS
Enable Time	8	10	16	22	ns
Disable Time	8	10	16	22	ns

NOTES:

1. For IDT7381, pins $I_0 - I_2$, RS_0, RS_1 apply. For IDT7383, pins $I_0 - I_4$ apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z, C_{16} for IDT7383.

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AC ELECTRICAL CHARACTERISTICS – MILITARY (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

MAXIMUM COMBINATIONAL PROPAGATION DELAYS

FROM INPUT	TO OUTPUT								UNITS
	7381L25 7383L25		7381L30 7383L30		7381L40 7383L40		7381L55 7383L55		
	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	
FTAB = 0, FTF = 0									
CLK	15	29	17	36	22	43	30	60	ns
C_0	–	21	–	25	–	31	–	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	–	29	–	36	–	43	–	60	ns
FTAB = 0, FTF = 1									
CLK	29	29	36	36	43	43	60	60	ns
C_0	23	21	28	25	34	31	47	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	33	29	39	36	48	43	66	60	ns
FTAB = 1, FTF = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	–	26	–	31	–	38	–	53	ns
CLK	15	–	17	–	22	–	30	–	ns
C_0	–	21	–	25	–	31	–	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	–	29	–	36	–	43	–	60	ns
FTAB = 1, FTF = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	28	26	33	31	41	38	56	53	ns
CLK	–	–	–	–	–	–	–	–	ns
C_0	23	21	28	25	34	31	47	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	33	29	39	36	48	43	66	60	ns

MINIMUM SETUP AND HOLD TIMES RELATIVE TO CLOCK (CLK)

INPUT	7381L25 7383L25		7381L30 7383L30		7381L40 7383L40		7381L55 7383L55		UNITS
	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	
FTAB = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	7	0	8	0	10	0	13	0	ns
C_0	21	0	25	0	31	0	43	0	ns
$I_0 - I_4$, RS_0, RS_1(1)	31	0	37	0	46	0	62	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	8	0	10	0	13	0	ns
FTAB = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	33	0	39	0	48	0	66	0	ns
C_0	33	0	39	0	48	0	66	0	ns
$I_0 - I_4$, RS_0, RS_1(1)	33	0	39	0	48	0	66	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	–	–	–	–	–	–	–	–	ns

MINIMUM CLOCK CYCLE TIMES AND PULSE WIDTHS

PARAMETER	7381L25 7383L25	7381L30 7383L30	7381L40 7383L40	7381L55 7383L55	UNITS
Clock LOW Time	6	8	10	14	ns
Clock HIGH Time	6	8	10	14	ns
Clock Period	25	30	40	55	ns

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

PARAMETER	7381L25 7383L25	7381L30 7383L30	7381L40 7383L40	7381L55 7383L55	UNITS
Enable Time	13	16	19	26	ns
Disable Time	13	16	19	26	ns

NOTES:

1. For IDT7381, pins $I_0 - I_2$, RS_0, RS_1 apply. For IDT7383, pins $I_0 - I_4$ apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z, C_{16} for IDT7383.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

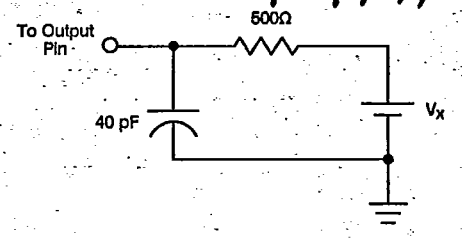

Figure 1. AC Output Test Load (V_X = 2.0V except for $\overline{OE}$ enable/disable)

ORDERING INFORMATION