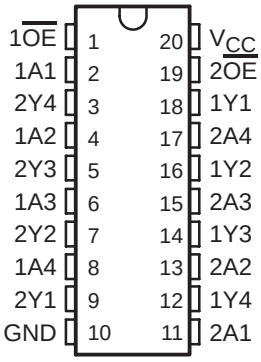
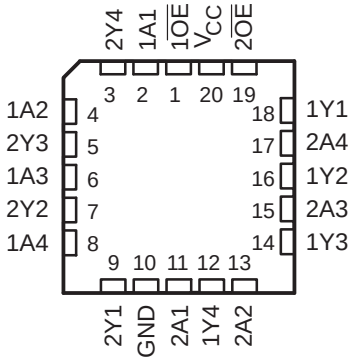
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **High-Impedance State During Power Up and Power Down**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs**

SN54LVTZ240 . . . J PACKAGE
SN74LVTZ240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTZ240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

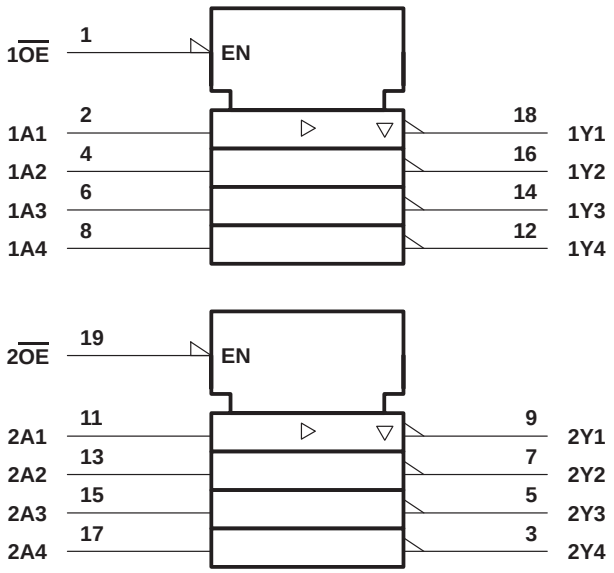
The SN54LVTZ240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVTZ240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

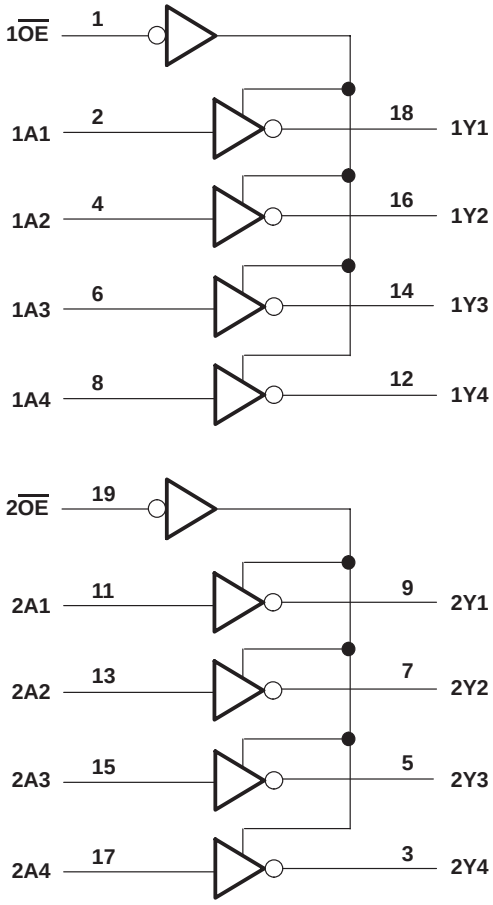
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTZ240 . . . . . 96 mA
SN74LVTZ240 . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTZ240 . . . . . 48 mA
SN74LVTZ240 . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package . . . . . 0.6 W
DW package . . . . . 1.6 W
PW package . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LVTZ240		SN74LVTZ240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTZ240			SN74LVTZ240			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 μA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 μA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	μA
	V_{CC} = 0 to 3.6 V	V_I = V_{CC} or GND	Control inputs			±1			±1	
		V_I = V_{CC}	Data inputs			1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0 V,	V_I or V_O = 0 to 4.5 V							±100	μA
I_{OZPU}§	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = X						±50	μA
I_{OZPD}§	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = X						±50	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			μA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−5			−5	μA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.225	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.225	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

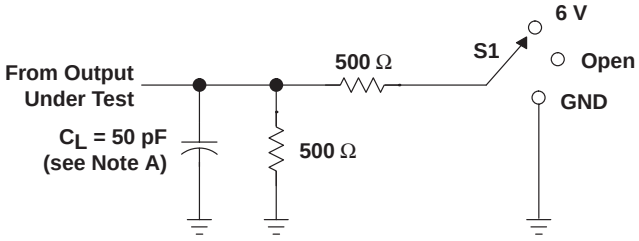
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This parameter is specified by characterization.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ240				SN74LVTZ240				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A	Y	1	4.5		5.4	1	2.5	4.3	5.2	ns
t_{PHL}			1	4.5		5.2	1	2.5	4.3	5	
t_{PZH}	$\overline{OE}$	Y	1	5.4		6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1	5.4		7.4	1	3.1	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	2	5.8		6.5	2	3.9	5.6	6.3	ns
t_{PLZ}			1.6	5.3		5.8	1.6	3.2	5.1	5.6	

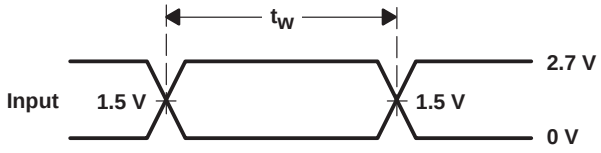
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

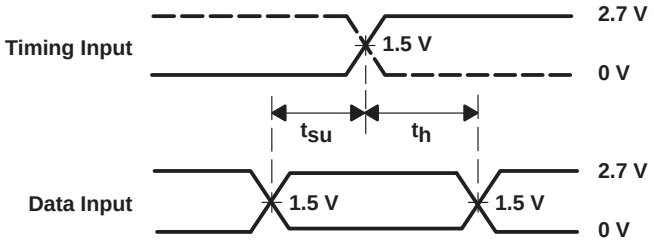


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

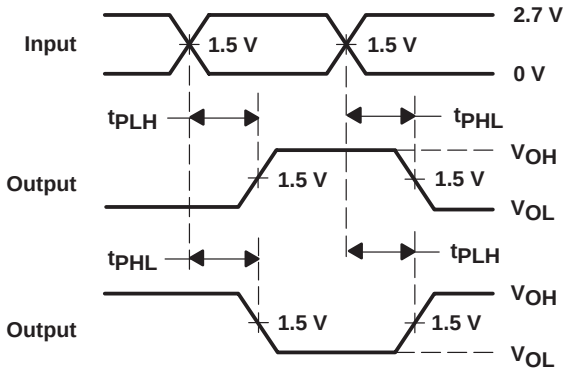
LOAD CIRCUIT FOR OUTPUTS



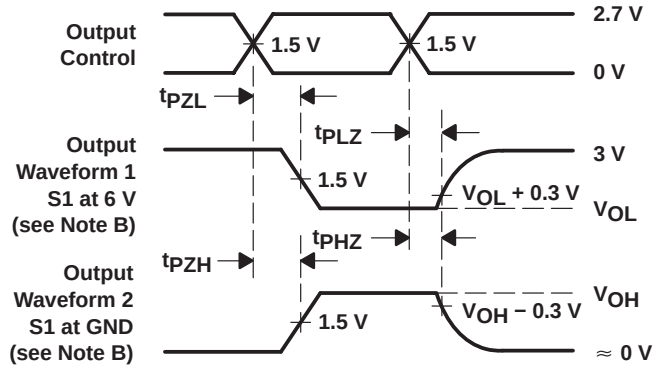
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



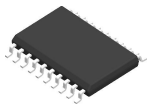
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

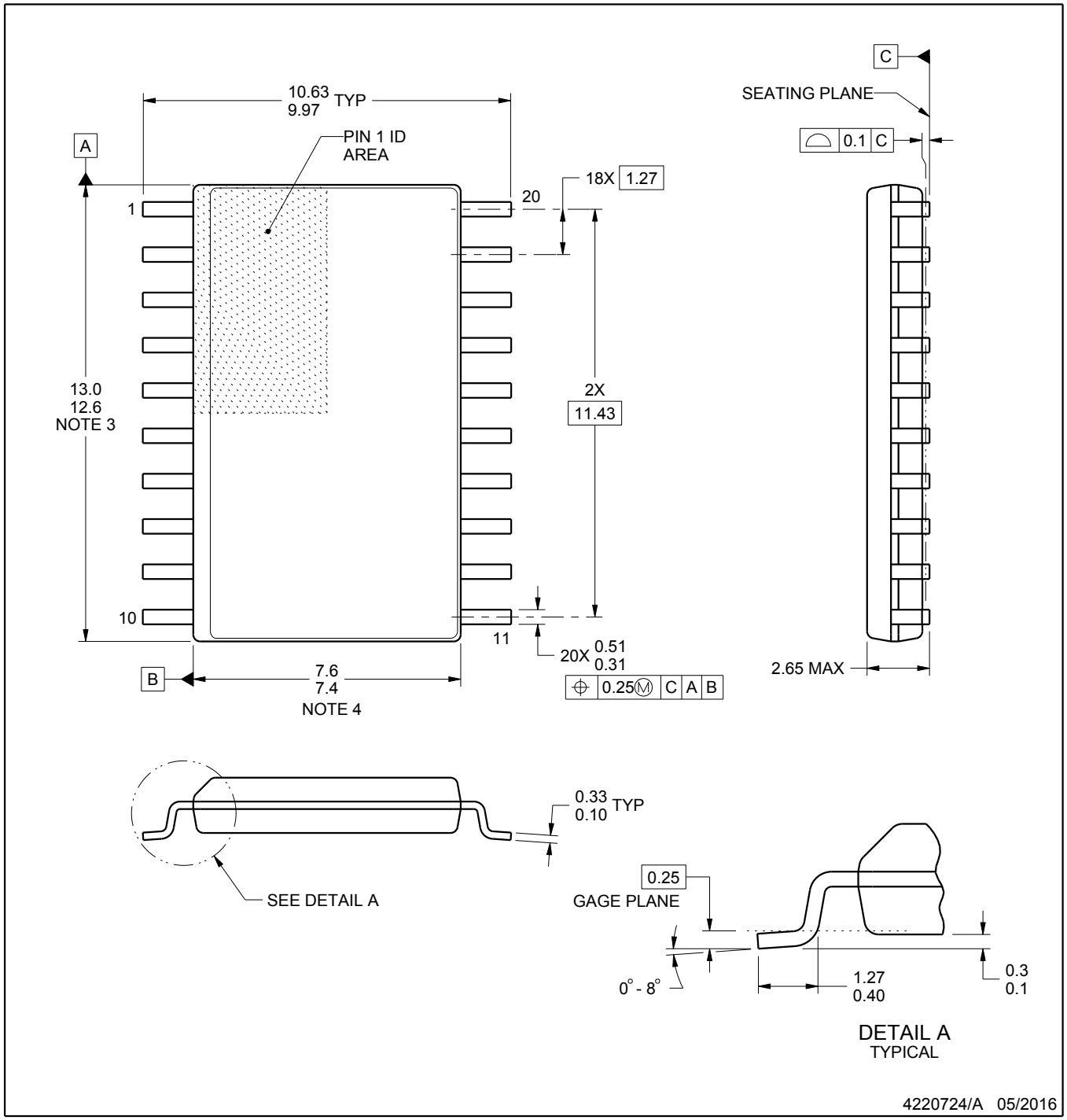


PACKAGE OUTLINE

DW0020A

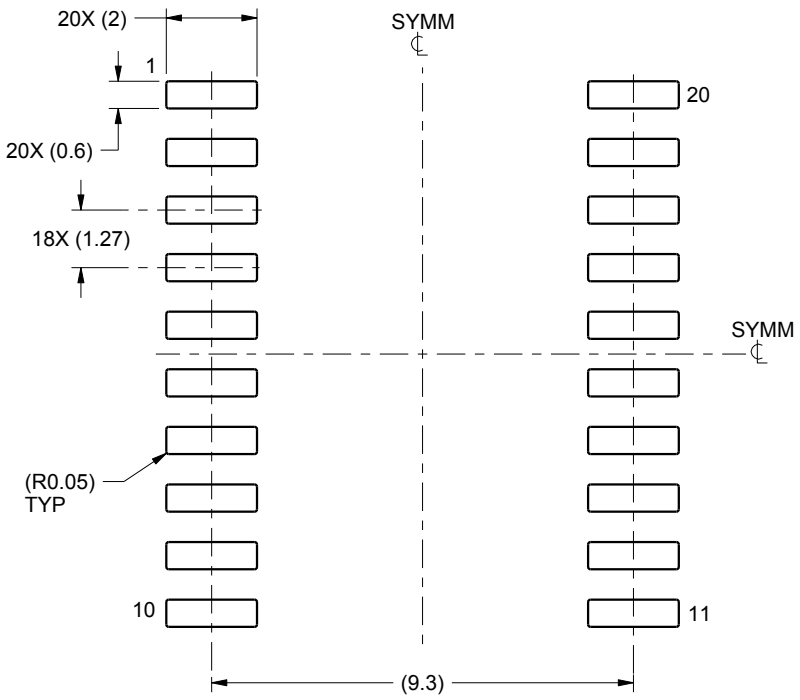
SOIC - 2.65 mm max height

SOIC

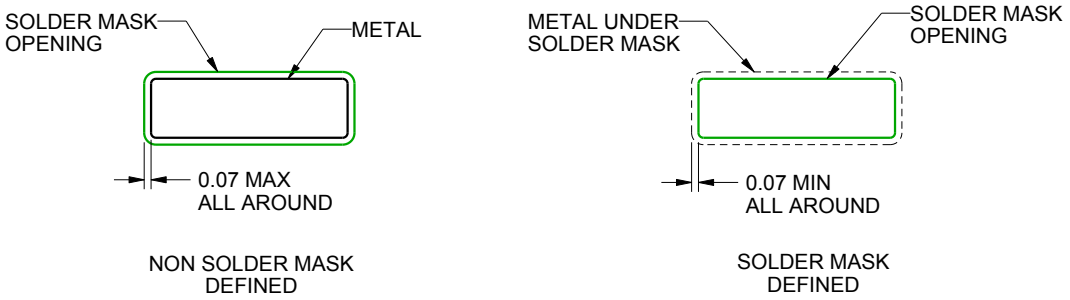


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

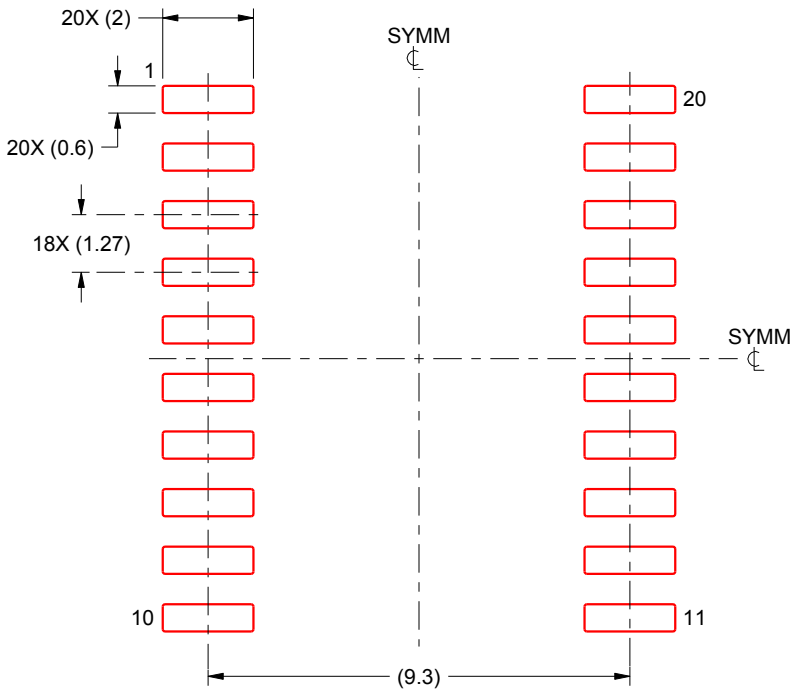


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



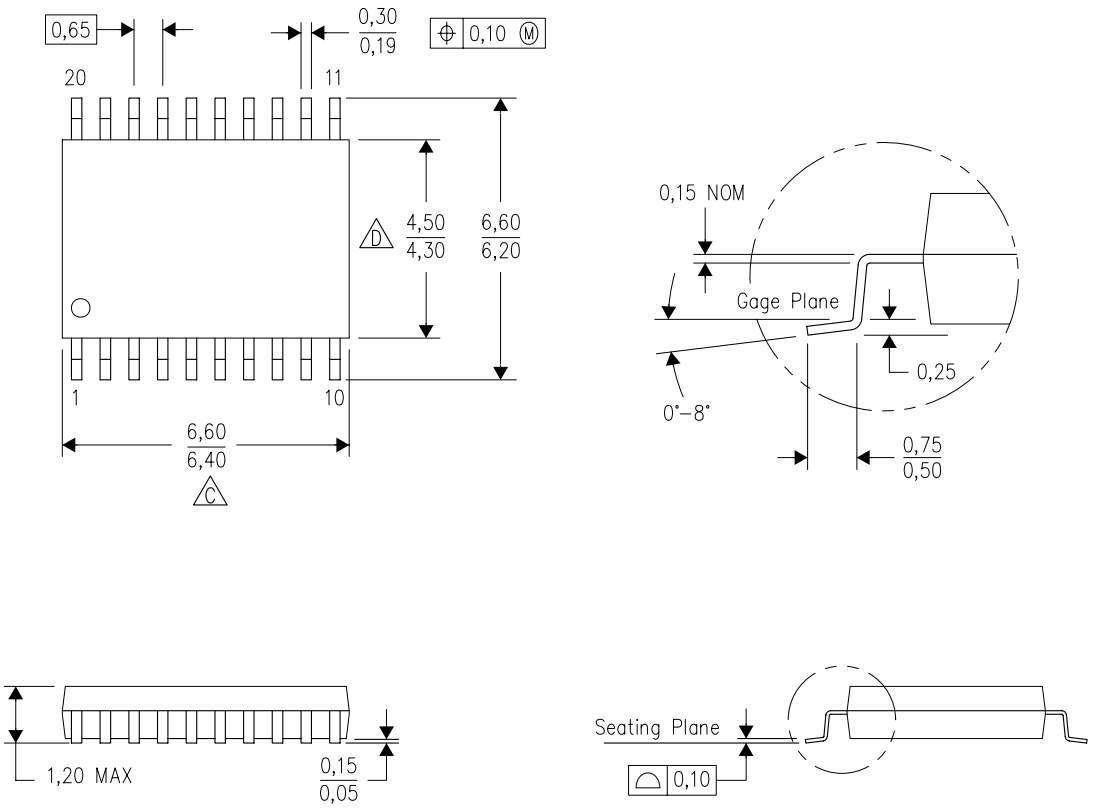
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



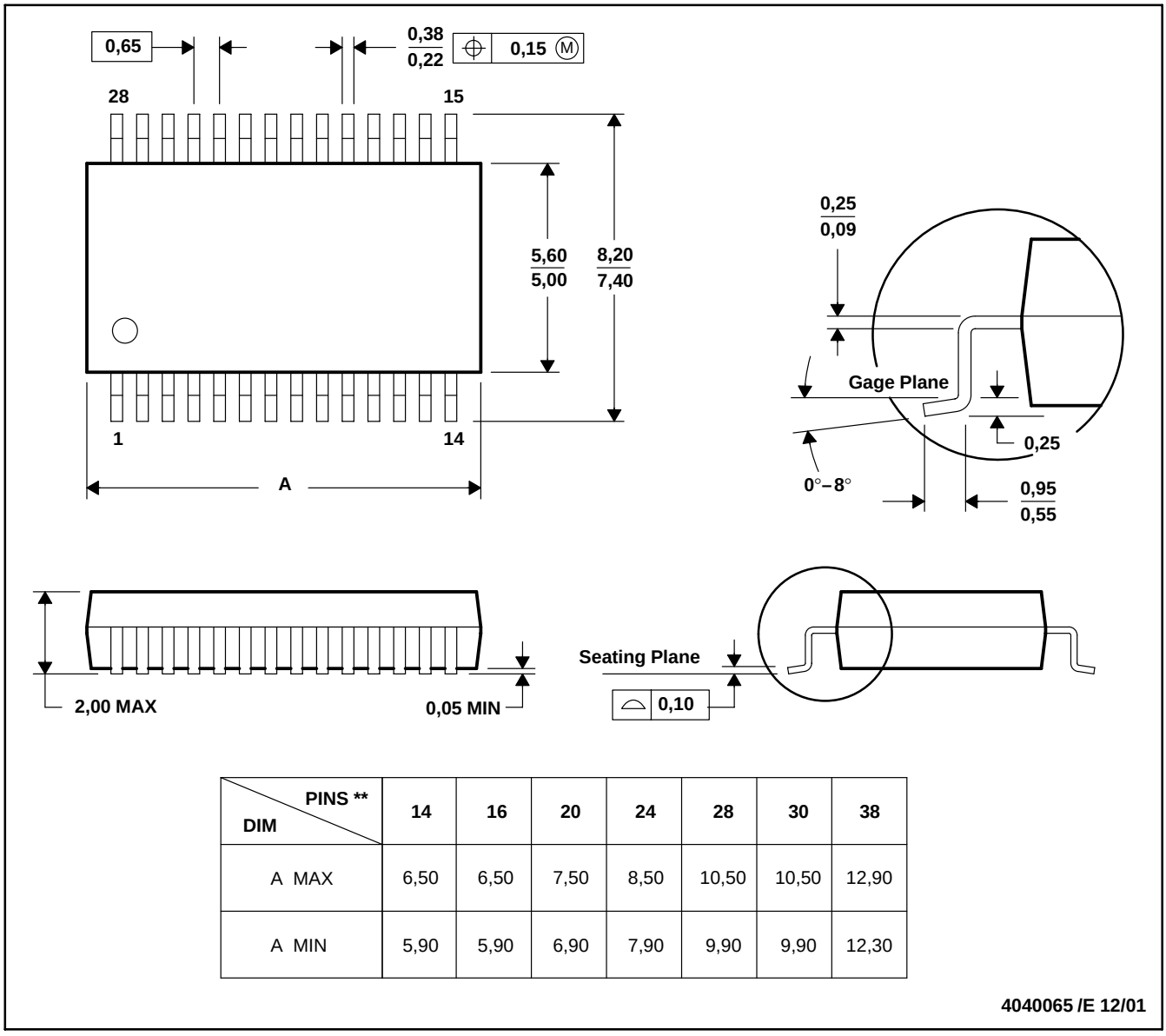
4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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