Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

MOTOROLA

SN54/74LS174

HEX D FLIP-FLOP

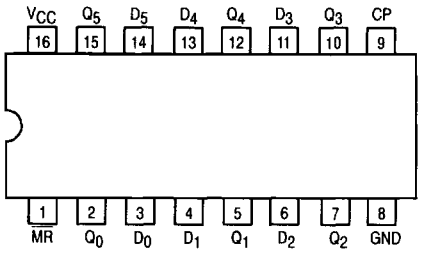
HEX D FLIP-FLOP

LOW POWER SCHOTTKY

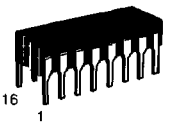
The LSTTL/MSI SN54/74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Asynchronous Common Reset
- Input Clamp Diodes Limit High Speed Termination Effects

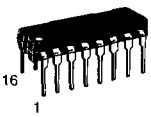
CONNECTION DIAGRAM DIP (TOP VIEW)



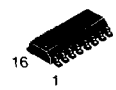
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

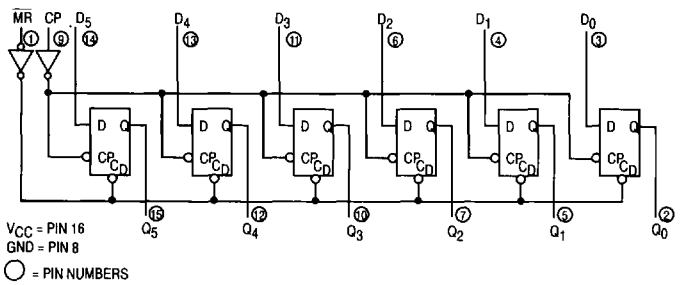
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

PIN NAMES

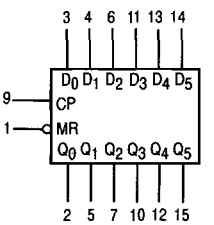
		LOADING (Note a) HIGH	LOW
D_0-D_5	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_5	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

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FUNCTIONAL DESCRIPTION

The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				26	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

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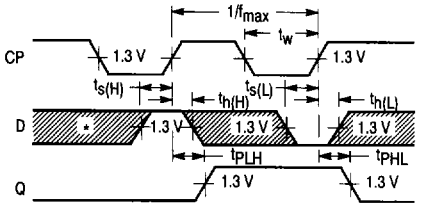
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Input Clock Frequency	30	40		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		23	35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 21	30 30	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock or $\overline{MR}$ Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	25			ns	

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

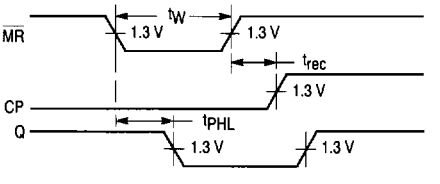


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.