PREPROGRAMMED CPU MOTHER BOARD FREQUENCY GENERATOR

DESCRIPTION

The ST49C107 is a mask programmable monolithic analog CMOS device designed to generate two simultaneous clocks. One clock is either the BCLK (buffered reference clock) or programmable. The other clock (called CLOCK or 2XCLOCK in different versions) is programmable only. The output frequency can vary from 2 to 100MHz, with up to 16 single selectable preprogrammed frequencies stored in internal ROM.

The ST49C107 is designed to replace existing CPU mother board clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via four address lines (two address lines for ST49C107-05).

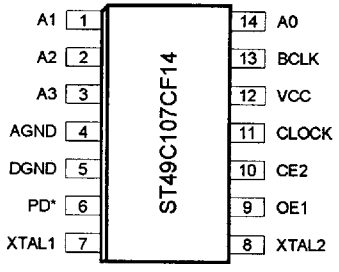
FEATURES

- Provides reference clock and synthesized clock
- 5 to 32MHz input reference frequency
- Pin-to-pin compatible to Avasem AV9107
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- Up to 16 frequencies stored internally
- 8/14 pin DIP or SOIC package.

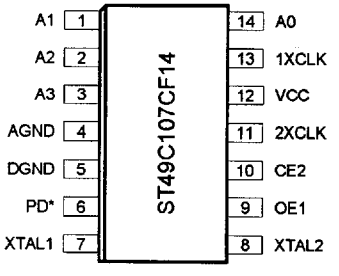
ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C107CP8	Plastic-DIP	0 ° C to +70° C
ST49C107CF8	SOIC	0° C to +70° C
ST49C107CP14	Plastic-DIP	0 ° C to +70° C
ST49C107CF14	SOIC	0° C to +70° C

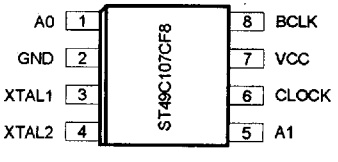
SOIC Package



ST49C107CF-03



ST49C107CF-04



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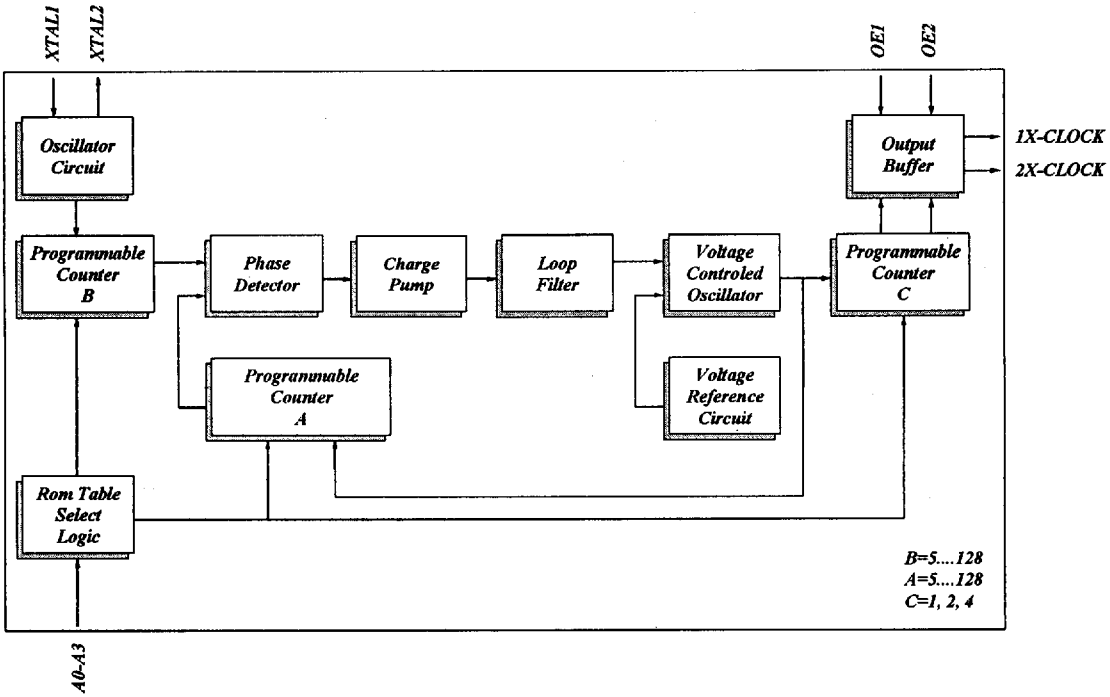
BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C107-03 package)

Symbol	Pin	Signal Type	Pin Description
A1	1*	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
A3	3*	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6*	I	Power-Down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9*	I	Buffered clock Output Enable (Active high). BCLK output is three stated when this pin is low.
OE2	10*	I	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
CLOCK	11	O	Programmed output clock.
VCC	12	I	Positive supply voltage. Single +5 volts.
BCLK	13	O	Buffered crystal clock output.
A0	14*	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

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SYMBOL DESCRIPTION (ST49C107-04 package)

Symbol	Pin	Signal Type	Pin Description
A1	1*	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
A3	3*	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6*	I	Power-Down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9*	I	1X-CLOCK Output Enable (Active high). 1X-CLOCK output is three stated when this pin is low.
OE2	10*	I	2X-CLOCK Output Enable (Active high). 2X-CLOCK output is three stated when this pin is low.
2XCLK	11	O	Programmed output clock.
VCC	12	I	Positive supply voltage. Single +5 volts.
1XCLK	13	O	2X-CLOCK Divide-by-two output.
A0	14*	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

SYMBOL DESCRIPTION (ST49C107-05 package)

Symbol	Pin	Signal Type	Pin Description
A0	1	I	Frequency select address input 1.
A1	5	I	Frequency select address input 2.
GND	2	O	Supply ground.
XTAL1	3	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLOCK	6	O	Programmed output clock.
VCC	7	I	Positive supply voltage. Single +5 volts.
BCLK	8	O	Buffered crystal clock output.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C107 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C107 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B X C)

where A=5, 6, 7,.....128
B=5, 6, 7,.....128
C=1,2

For proper output frequency, the ST49C107 can accept a reference frequency from 5 - 32 MHz and divider ratio up to 15.

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-10	µA	Exc. crystal input
I_{IH}	Input high current			1	µA	VIN=Vcc
I_{CC}	Operating current		45	55	mA	No load. CLOCK=100MHz
I_{SB}	Standby current		25		µA	No load.
R_{IN}	Input pull-up resistance	500	900	1300	kΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	1X, 2X-CLOCK rise time		1	2	ns	CL=20pF 0.8V - 2.0V
T_2	1X, 2X-CLOCK fall time		1	2	ns	CL=20pF 2.0V - 0.8V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±3	±5	%	
T	Input frequency	2		32	MHz	
T_7	Buffered clock rise time			20	ns	
T_8	Buffered clock fall time			20	ns	

CLOCK OUTPUT TABLE FOR ST49C107-03 (using 14.318 MHz input. All frequencies in MHz).

A3 A2 A1 A0	CLOCK
0 0 0 0	16.00
0 0 0 1	40.01
0 0 1 0	50.11
0 0 1 1	80.01
0 1 0 0	66.58
0 1 0 1	100.23
0 1 1 0	8.02
0 1 1 1	4.01
1 0 0 0	8.02
1 0 0 1	20.00
1 0 1 0	25.06
1 0 1 1	40.01
1 1 0 0	33.29
1 1 0 1	50.11
1 1 1 0	4.01
1 1 1 1	2.05

CLOCK OUTPUT TABLE FOR ST49C107-04 (using 14.318 MHz input. All frequencies in MHz).

A3 A2 A1 A0	2X-CLOCK	CLOCK
0 0 0 0	80.02	40.01
0 0 0 1	66.62	33.31
0 0 1 0	50.11	25.06
0 0 1 1	40.01	20.00
0 1 0 0	100.23	50.11
0 1 0 1	33.31	16.66
0 1 1 0	32.01	16.00
0 1 1 1	25.06	12.47
1 0 0 0	64.02	32.01
1 0 0 1	2X-Input	1X-Input
1 0 1 0	3X-Input	1.5X-Input
1 0 1 1	8X-Input	4X-Input
1 1 0 0	0.5X-Input	0.25X-Input
1 1 0 1	0.25X-Input	0.125X-Input
1 1 1 0	120.00	60.00
1 1 1 1	129.96	64.98

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CLOCK OUTPUT TABLE FOR ST49C107-05 (using 14.318 MHz input. All frequencies in MHz).

A1 A0	CLOCK
0 0	40.01
0 1	50.11
1 0	66.61
1 1	80.01

TIMING DIAGRAM