Dual D-type flip-flop with set and reset | 74ALS74A

DESCRIPTION

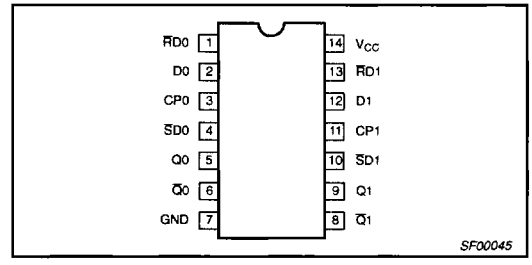
The 74ALS74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active-Low inputs and operate independently of the clock input. When set and reset are inactive (High), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the Low-to-High transition of the clock. Data must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS74A	150MHz	3.0mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
14-pin plastic DIP	74ALS74AN	SOT27-1
14-pin plastic SO	74ALS74AD	SOT108-1
14-pin plastic SSOP Type II	74ALS74ADB	SOT337-1

PIN CONFIGURATION

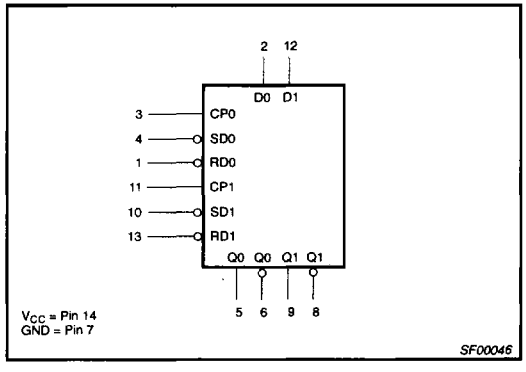


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

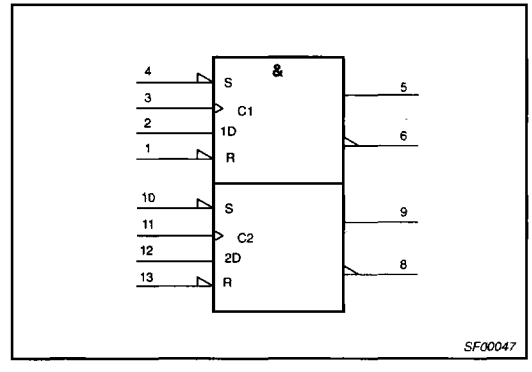
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0, D1	Data inputs	1.0/2.0	20µA/0.2mA
CP0, CP1	Clock inputs (active rising edge)	1.0/2.0	20µA/0.2mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active-Low)	2.0/4.0	40µA/0.4mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active-Low)	2.0/4.0	40µA/0.4mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

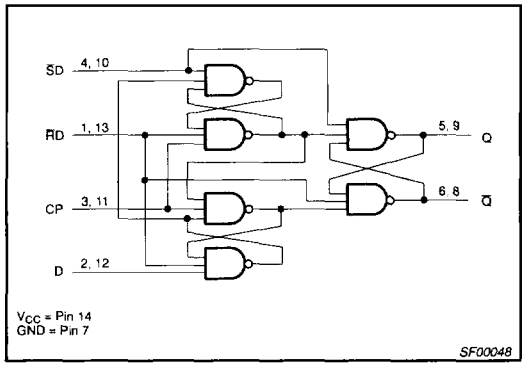
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

H = High voltage level
h = High state must be present one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time prior to Low-to-High clock transition
NC= No change from the previous setup
X = Don't care
↑ = Low-to-High clock transition
↕ = Not Low-to-High clock transition
* = Both outputs will be High while both $\overline{SD}$ and $\overline{RD}$ are Low, but the output states are unpredictable if $\overline{SD}$ and $\overline{RD}$ go High simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	Dn, CPn	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		$\overline{SD}$n, $\overline{RD}$n					0.2	mA
I_{IH}	High–level input current	Dn, CPn	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{SD}$n, $\overline{RD}$n					40	µA
I_{IL}	Low–level input current	Dn, CPn	V_{CC} = MAX, V_I = 0.4V				–0.2	mA
		$\overline{SD}$n, $\overline{RD}$n					–0.4	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			3.0	4.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.
4. Measure I_{CC} with the Dn, CPn, and $\overline{SD}$n grounded, then with Dn, CPn, and $\overline{RD}$n grounded.

AC ELECTRICAL CHARACTERISTICS

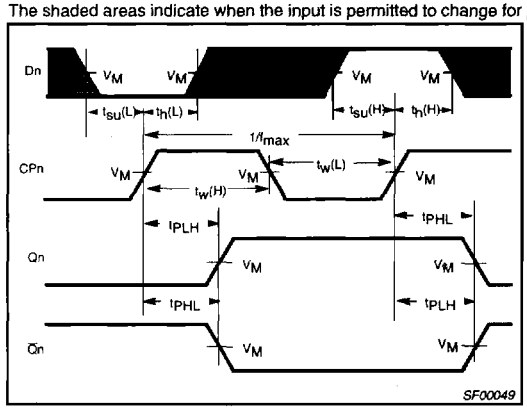
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.0 3.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n or $\overline{RD}$ to Qn or $\overline{Q}$n	Waveform 2, 3	1.0 3.0	8.0 10.0	ns

AC SETUP REQUIREMENTS

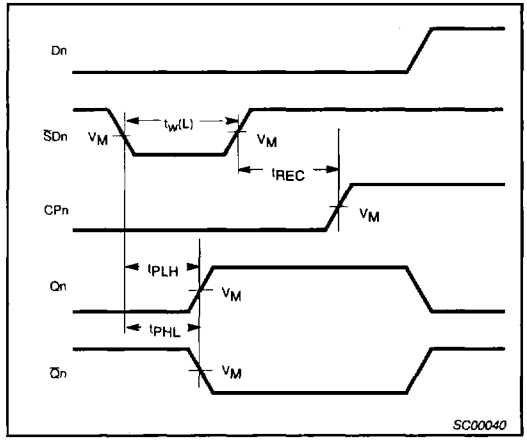
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, High or Low Dn to CPn	Waveform 1	6.0 6.0		ns
t_h (H) t_h (L)	Hold time, High or Low Dn to CPn	Waveform 1	0.0 0.0		ns
t_w (H) t_w (L)	CPn Pulse width High or Low	Waveform 1	6.0 6.0		ns
t_w (L)	$\overline{SD}$n or $\overline{RD}$n Pulse width, Low	Waveform 2, 3	6.0		ns
t_{rec}	Recovery time, $\overline{SD}$n or $\overline{RD}$n to CPn	Waveform 2, 3	6.0		ns

AC WAVEFORMS

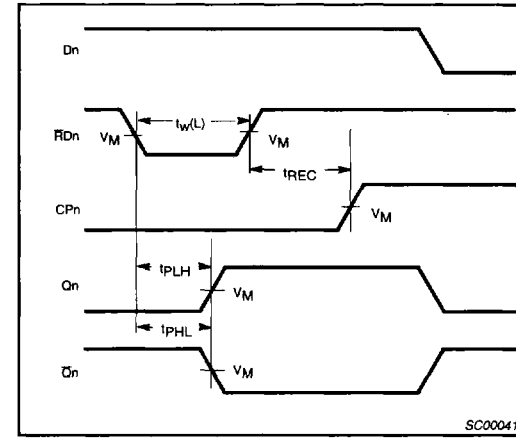
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup and Hold Times, Clock Width, and Maximum Clock Frequency

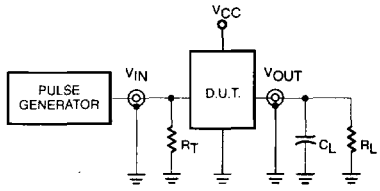


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width and Recovery Time for Set to Clock

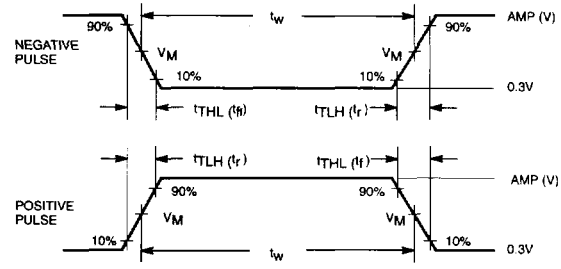


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width and Recovery Time for Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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