

**KM23C8000A(G)****CMOS MASK ROM****8M-Bit (1M × 8) CMOS MASK ROM****FEATURES**

- 1,048,576 × 8 bit organization
- Fast access time: 150ns (max.)
- Supply voltage: single +5V
- Current consumption
  - Operating: 50mA (max.)
  - Standby : 50 $\mu$ A (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)
- 32-pin, 525 mil, plastic SOP

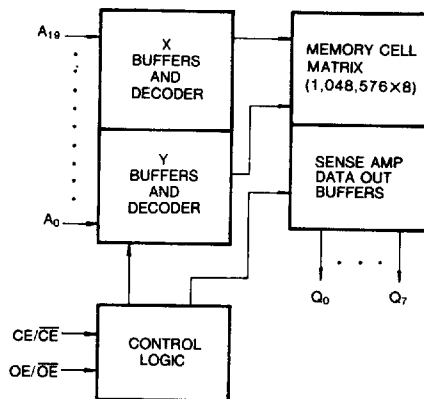
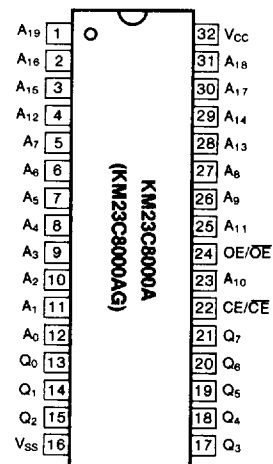
**GENERAL DESCRIPTION**

The KM23C8000A is a fully static mask programmable ROM organized 1,048,576 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C8000A is packaged in a 32-DIP and the KM23C8000AG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

**FUNCTIONAL BLOCK DIAGRAM****PIN CONFIGURATION**

Pin Name	Pin Function
A <sub>0</sub> -A <sub>19</sub>	Address Inputs
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs
CE/ $\overline$ CE*	Chip Enable
OE/ $\overline$ OE*	Output Enable
V <sub>CC</sub>	Power (+5V)
V <sub>SS</sub>	Ground

\* User Selectable Polarity

**KM23C8000A(G)****CMOS MASK ROM****ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to +7.0	V
Temperature Under Bias	T <sub>bias</sub>	-10 to +85	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage reference to V<sub>SS</sub>, T<sub>A</sub>=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V

**DC CHARACTERISTICS**

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I <sub>CC</sub>	$\overline{CE} = \overline{OE} = V_{IL}$ , f = 6.7MHz all output open	—	50	mA
Standby Current (TTL)	I <sub>SB1</sub>	$\overline{CE} = V_{IH}$ , all output open	—	1	mA
Standby Current (CMOS)	I <sub>SB2</sub>	$\overline{CE} = V_{CC}$ , all output open	—	50	μA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	—	10	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 to V <sub>CC</sub>	—	10	μA
Input High Voltage, All Inputs	V <sub>IH</sub>		2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage, All Inputs	V <sub>IL</sub>		-0.3	0.8	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> = -400μA	2.4	—	V
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	0.4	V

**CAPACITANCE** (T<sub>A</sub>=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V	—	10.0	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

**MODE SELECTION**

CE/ $\overline{CE}$	OE/ $\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	Dout	Active

## KM23C8000A(G)

## CMOS MASK ROM

## AC CHARACTERISTICS (Ta=0° to +70°C, VCC=5V±10%, unless otherwise noted.)

## TEST CONDITIONS

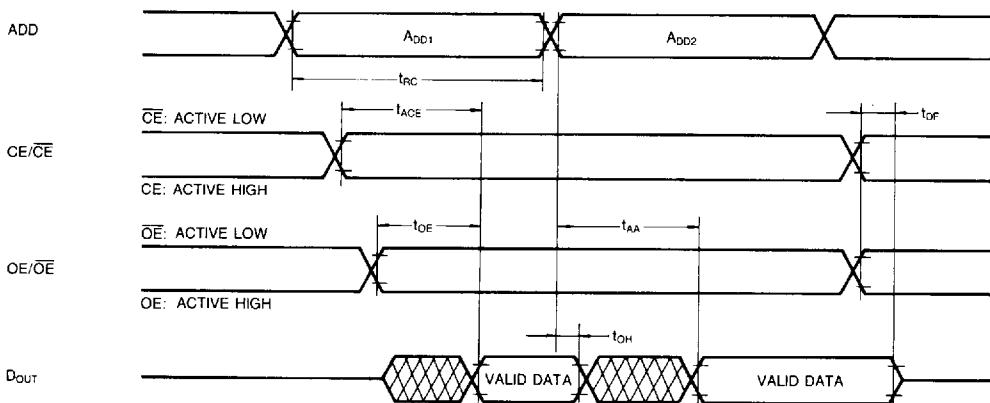
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C <sub>L</sub> = 100pF

## READ CYCLE

Parameter	Symbol	KM23C8000A(G)-15		KM23C8000A(G)-20		KM23C8000A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	150		200		250		ns
Chip Enable Access Time	t <sub>ACE</sub>		150		200		250	ns
Address Access Time	t <sub>AA</sub>		150		200		250	ns
Output Enable Access Time	t <sub>OE</sub>		70		90		110	ns
Output or Chip Disable to Output High-Z	t <sub>DF</sub>		30		40		50	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		ns

## TIMING DIAGRAM

## READ



\* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

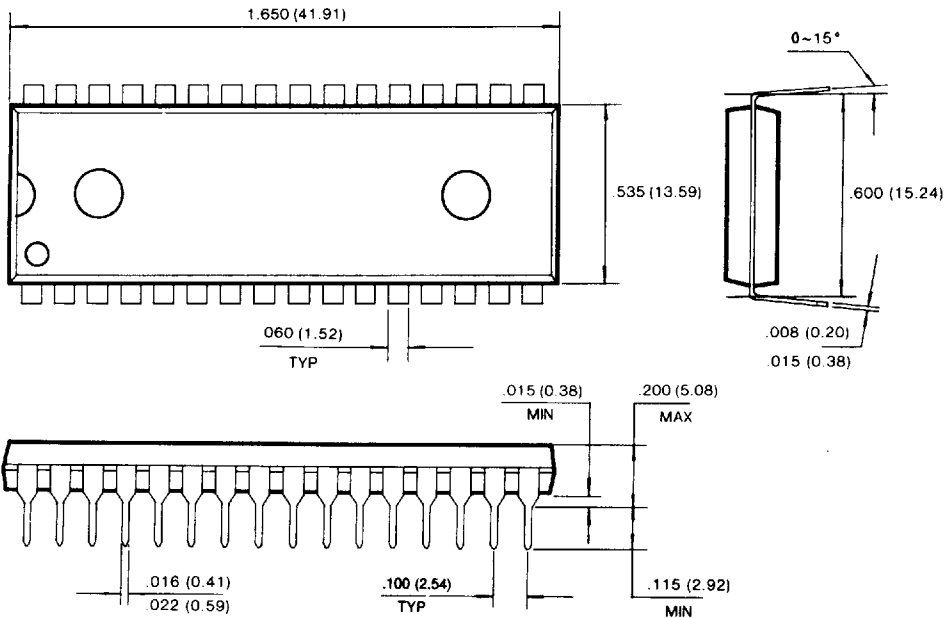
**KM23C8000A(G)**

**CMOS MASK ROM**

**PACKAGE DIMENSIONS**

**32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8000A)**

Units: Inches (millimeters)



**32 LEAD SMALL OUTLINE PACKAGE (KM23C8000AG)**

