

M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418160BXX-6, -6S	60	15	30	15	110	680
M5M418160BXX-7, -7S	70	20	35	20	130	590
M5M418160BXX-8, -8S	80	20	40	20	150	500

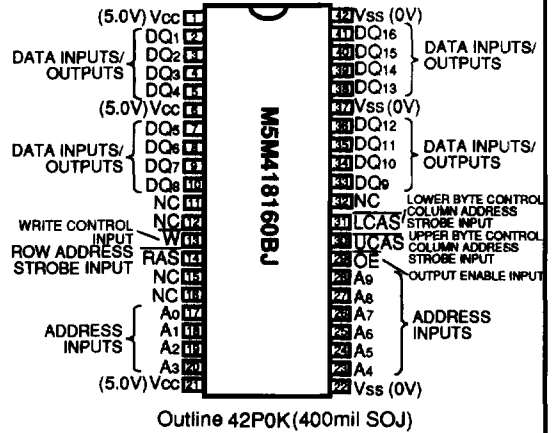
XX=J, TP, RT

- Standard 42pin SOJ, 50pin TSOP
- Single 5.0V \pm 10% supply
- Low stand-by power dissipation
5.5mW (Max) CMOS Input level
- Low operating power dissipation
M5M418160Bxx -6, -6S 830.0mW (Max)
M5M418160Bxx -7, -7S 720.0mW (Max)
M5M418160Bxx -8, -8S 610.0mW (Max)
- Fast-page mode, Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A₀ ~A₉)

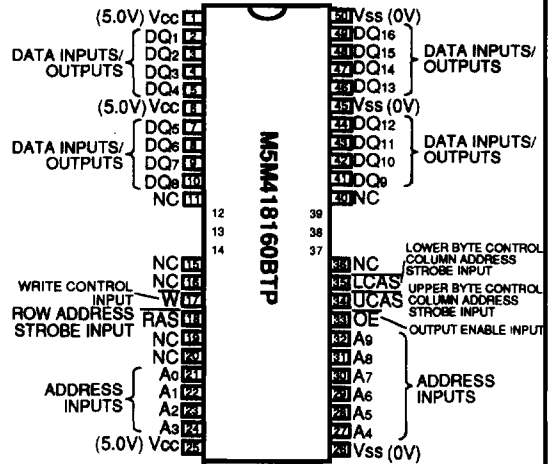
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

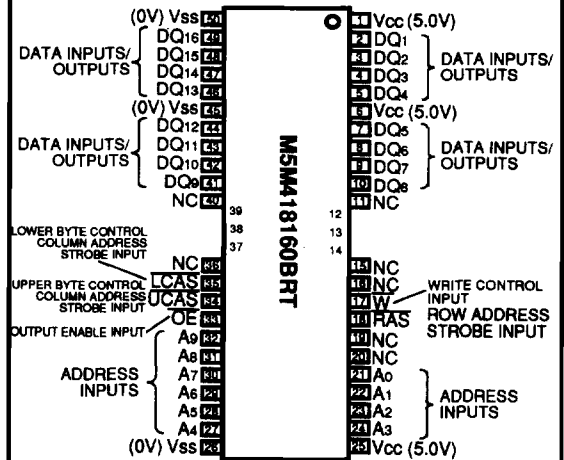
PIN CONFIGURATION (TOP VIEW)



Outline 42P0K (400mil SOJ)



Outline 50P3W-L (400mil TSOP)



Outline 50P3W-M (400mil TSOP)

NC : NO CONNECTION

M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

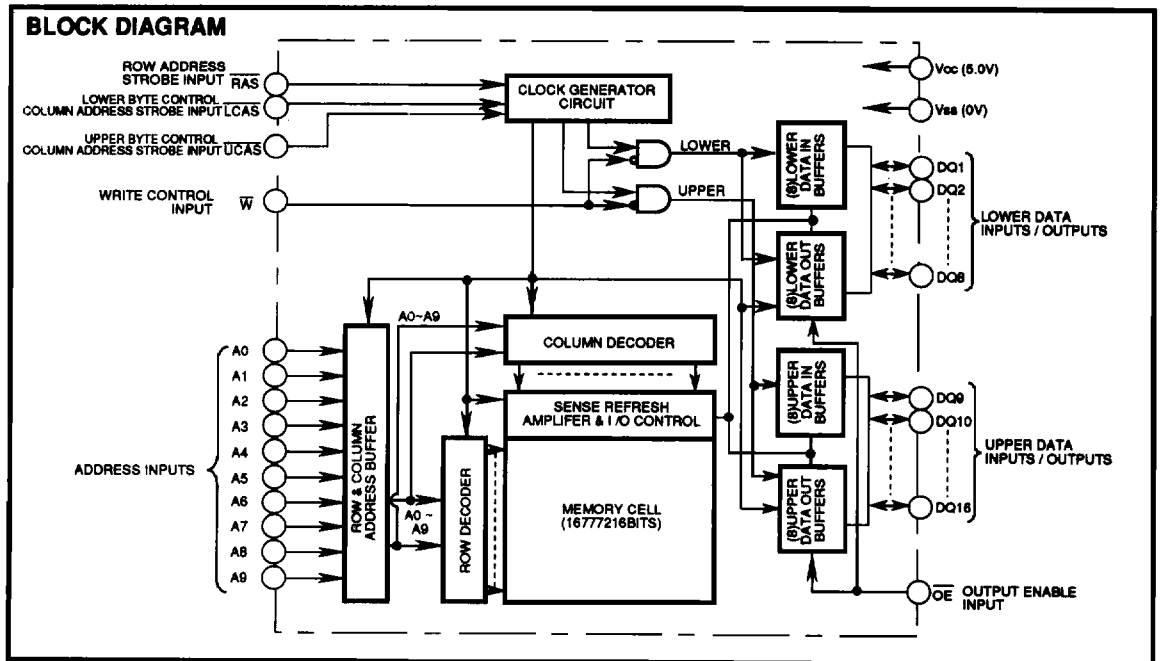
FUNCTION

The M5M418160BJ, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, \overline{RAS} -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	\overline{RAS}	\overline{LCAS}	\overline{UCAS}	\overline{W}	\overline{OE}	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
\overline{RAS} -only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
\overline{CAS} before \overline{RAS} refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open



M5M418160BJ,TP,RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.0	V
V _{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5.0V ± 10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} =-5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} =4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating, 0V ≤ V _{out} ≤ 5.5V	-10		10	μA
I _I	Input current	0V ≤ V _{IH} ≤ 6V, Other inputs pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	M5M418160B-6,-6S	RAS, CAS cycling trc=trw=min. output open		150	mA
		M5M418160B-7,-7S			130	
		M5M418160B-8,-8S			110	
I _{CC2}	Supply current from V _{CC} , stand-by (Note 6)	RAS=CAS=V _{IH} , output open			2	mA
		RAS=CAS ≥ V _{CC} -0.2V			0.5	
I _{CC3} (AV)	Average supply current from V _{CC} refreshing (Note 3,5)	M5M418160B-6,-6S	RAS cycling, CAS=V _{IH} trc=min. output open		150	mA
		M5M418160B-7,-7S			130	
		M5M418160B-8,-8S			110	
I _{CC4} (AV)	Average supply current from V _{CC} Fast-Page-Mode (Note 3,4,5)	M5M418160B-6,-6S	RAS=V _{IL} , CAS cycling trc=min. output open		70	mA
		M5M418160B-7,-7S			60	
		M5M418160B-8,-8S			50	
I _{CC6} (AV)	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3)	M5M418160B-6,-6S	CAS before RAS refresh cycling trc=min. output open		150	mA
		M5M418160B-7,-7S			130	
		M5M418160B-8,-8S			110	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1}(AV), I_{CC3}(AV) and I_{CC4}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and LCAS/UCAS=V_{IH}.

CAPACITANCE (T_a=0~70°C, V_{CC}=5.0V ± 10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I =V _{SS} f=1MHz V _I =25mVrms			5	pF
C _{I(ØE)}	Input capacitance, ØE input				7	pF
C _{I(W)}	Input capacitance, W input				7	pF
C _{I(RAS)}	Input capacitance, RAS input				7	pF
C _{I(CAS)}	Input capacitance, CAS input				7	pF
C _{I/O}	Input/Output capacitance, data ports				8	pF

M5M418160BJ,TP,RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note7,8)		15		20		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note7,9)		60		70		80	ns
tAA	Column address access time (Note 7,10)		30		35		40	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		35		40		45	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		15		20		20	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	15	0	15	0	15	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	15	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 2TTL loads and 100pF.

8: Assumes that $t_{\text{RCO}} \geq t_{\text{RCO}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

9: Assumes that $t_{\text{RCO}} \leq t_{\text{RCO}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{ASC}}(\text{max})$. If t_{RCO} or t_{ASC} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCO} exceeds the value shown.

10: Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

11: Assumes that $t_{\text{CP}} \leq t_{\text{CP}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

12: $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ defines the time at which the output achieves the high impedance state ($I_{\text{OH}} \leq \pm 10 \mu\text{A}$) and is not reference to $V_{\text{OH}}(\text{min})$ or $V_{\text{OL}}(\text{max})$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tRP	$\overline{\text{RAS}}$ high pulse width	40		50		60		ns
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note15)	20	45	20	50	20	60	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	10		10		10		ns
tRPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		0		ns
tCPN	$\overline{\text{CAS}}$ high pulse width	10		10		10		ns
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note16)	15	30	15	35	15	40	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low	0		0		0		ns
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low	10		10		10		ns
tCAH	Column address hold time after $\overline{\text{CAS}}$ low	15		15		15		ns
tDZC	Delay time, data to $\overline{\text{CAS}}$ low (Note18)	0		0		0		ns
tDZO	Delay time, data to $\overline{\text{OE}}$ low (Note18)	0		0		0		ns
tCDD	Delay time, $\overline{\text{CAS}}$ high to data (Note19)	15		15		15		ns
tODD	Delay time, $\overline{\text{OE}}$ high to data (Note19)	15		15		15		ns
tT	Transition time (Note20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed $t_r = 5\text{ns}$.

14: $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals.

15: $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is less than $t_{\text{RCD}}(\text{max})$, access time is t_{RAC} . If t_{RCD} is greater than $t_{\text{RCD}}(\text{max})$, access time is controlled exclusively by t_{CAC} or t_{AA} . $t_{\text{RCD}}(\text{min})$ is specified as $t_{\text{RCD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + 2t_{\text{T}} + t_{\text{ASC}}(\text{min})$.

16: $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{ASC}}(\text{max})$, access time is controlled exclusively by t_{AA} .

17: $t_{\text{ASC}}(\text{max})$ is specified as a reference point only. If $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$, access time is controlled exclusively by t_{CAC} .

18: Either t_{DZC} or t_{DZO} must be satisfied.

19: Either t_{CDD} or t_{ODD} must be satisfied.

20: t_{T} is measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.

M5M418160BJ,TP,RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	110		130		150		ns
tRAS	\overline{RAS} low pulse width	60	10000	70	10000	80	10000	ns
tCAS	\overline{CAS} low pulse width	15	10000	20	10000	20	10000	ns
tCSH	\overline{CAS} hold time after \overline{RAS} low	60		70		80		ns
tRSH	\overline{RAS} hold time after \overline{CAS} low	15		20		20		ns
tRCS	Read Setup time after \overline{CAS} high	0		0		0		ns
tRCH	Read hold time after \overline{CAS} low (Note 21)	0		0		0		ns
tRRH	Read hold time after \overline{RAS} low (Note 21)	10		10		10		ns
tRAL	Column address to \overline{RAS} hold time	30		35		40		ns
tOCH	\overline{CAS} hold time after \overline{OE} low	15		20		20		ns
tORH	\overline{RAS} hold time after \overline{OE} low	15		20		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	110		130		150		ns
tRAS	\overline{RAS} low pulse width	60	10000	70	10000	80	10000	ns
tCAS	\overline{CAS} low pulse width	15	10000	20	10000	20	10000	ns
tCSH	\overline{CAS} hold time after \overline{RAS} low	60		70		80		ns
tRSH	\overline{RAS} hold time after \overline{CAS} low	15		20		20		ns
tWCS	Write setup time before \overline{CAS} low (Note 23)	0		0		0		ns
tWCH	Write hold time after \overline{CAS} low	10		10		15		ns
tCWL	\overline{CAS} hold time after \overline{W} low	15		20		20		ns
tRWL	\overline{RAS} hold time after \overline{W} low	15		20		20		ns
tWP	Write pulse width	10		10		15		ns
tDS	Data setup time before \overline{CAS} low or \overline{W} low	0		0		0		ns
tDH	Data hold time after \overline{CAS} low or \overline{W} low	10		15		15		ns
tOEH	\overline{OE} hold time after \overline{W} low	15		20		20		ns

M5M418160BJ,TP,RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
trwc	Read write/read modify write cycle time (Note22)	155		180		200		ns
trAS	RAS low pulse width	105	10000	120	10000	130	10000	ns
tcAS	CAS low pulse width	60	10000	70	10000	70	10000	ns
tcSH	CAS hold time after RAS low	105		120		130		ns
trSH	RAS hold time after CAS low	60		70		70		ns
trCS	Read setup time before CAS low	0		0		0		ns
tcWD	Delay time, CAS low to W low (Note23)	40		45		45		ns
trWD	Delay time, RAS low to W low (Note23)	85		95		105		ns
tAWD	Delay time, address to W low (Note23)	55		60		65		ns
tcWL	CAS hold time after W low	15		20		20		ns
trWL	RAS hold time after W low	15		20		20		ns
tWP	Write pulse width	10		10		15		ns
tDS	Data setup time before W low	0		0		0		ns
tDH	Data hold time after W low	10		15		15		ns
tOEH	OE hold time after W low	15		15		15		ns

Note 22: trwc is specified as $trwc_{(min)} = trAS_{(max)} + tODD_{(min)} + trWL_{(min)} + trP_{(min)} + 5T$.

Note 23: tcws, tcwd, trwd and tawd and, tcpwd are specified as reference points only. If $tcws \geq tcws_{(min)}$ the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If $tcwd \geq tcwd_{(min)}$, $trwd \geq trwd_{(min)}$, $tawd \geq tawd_{(min)}$ and $tcpwd \geq tcpwd_{(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to V_{ih}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
tpc	Fast page mode read/write cycle time	40		45		50		ns
tpRWC	Fast page mode read write/read modify write cycle time	85		95		105		ns
trAS	RAS low pulse width for read write cycle (Note25)	100	125000	115	125000	130	125000	ns
tcp	CAS high pulse width (Note26)	10	15	10	15	10	15	ns
tcPRH	RAS hold time after CAS precharge	35		40		45		ns
tcpWD	Delay time, CAS precharge to W low (Note23)	60		65		70		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: trAS_(min) is specified as two cycles of CAS input are performed.

26: tcp_(max) is specified as a reference point only.

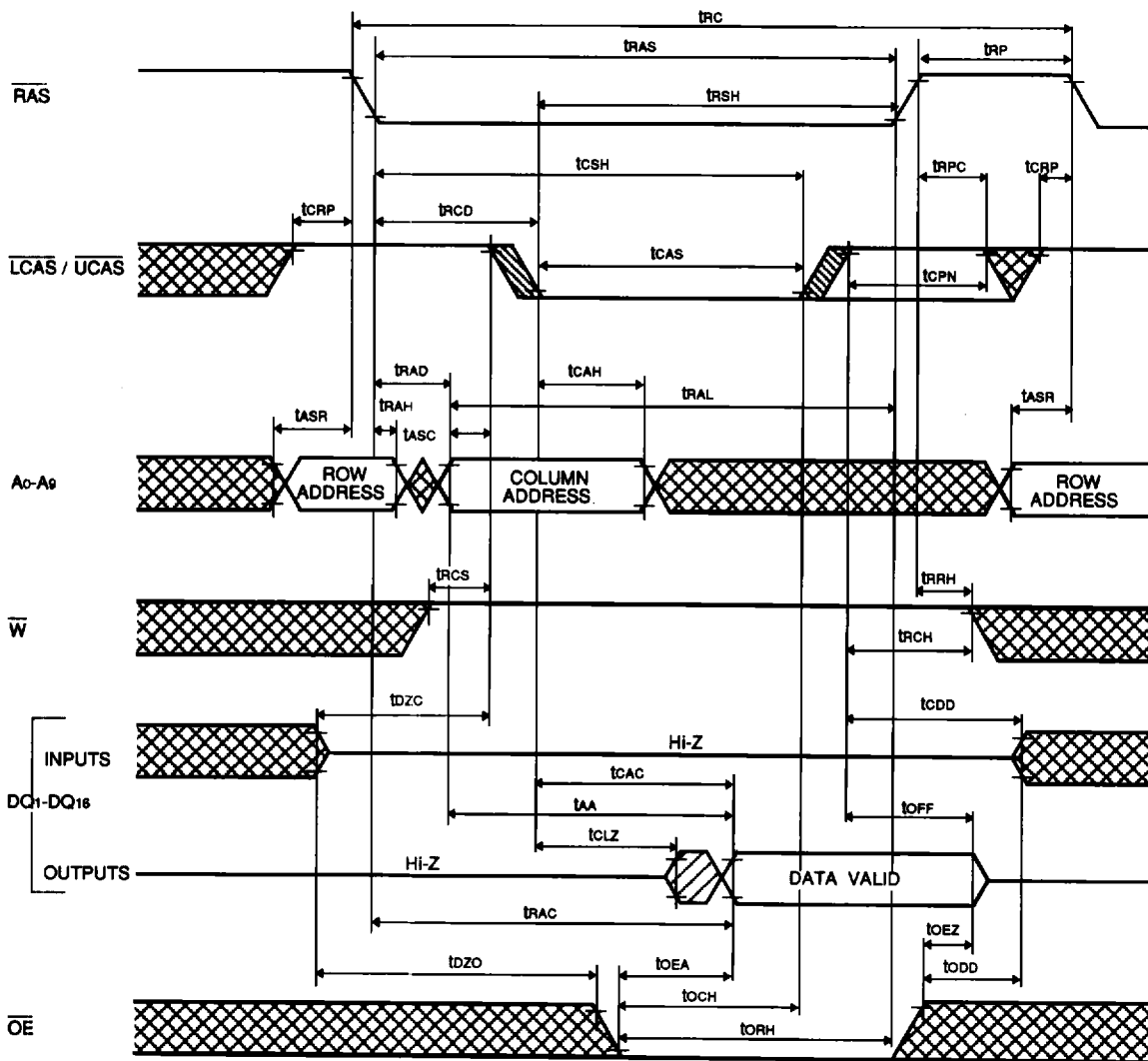
CAS before RAS Refresh Cycle (Note 27)




Symbol	Parameter	Limits						Unit
		M5M418160B-6,-6S		M5M418160B-7,-7S		M5M418160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
tcSR	CAS setup time before RAS low	10		10		10		ns
tcHR	CAS hold time after RAS low	10		15		15		ns

Note 27: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

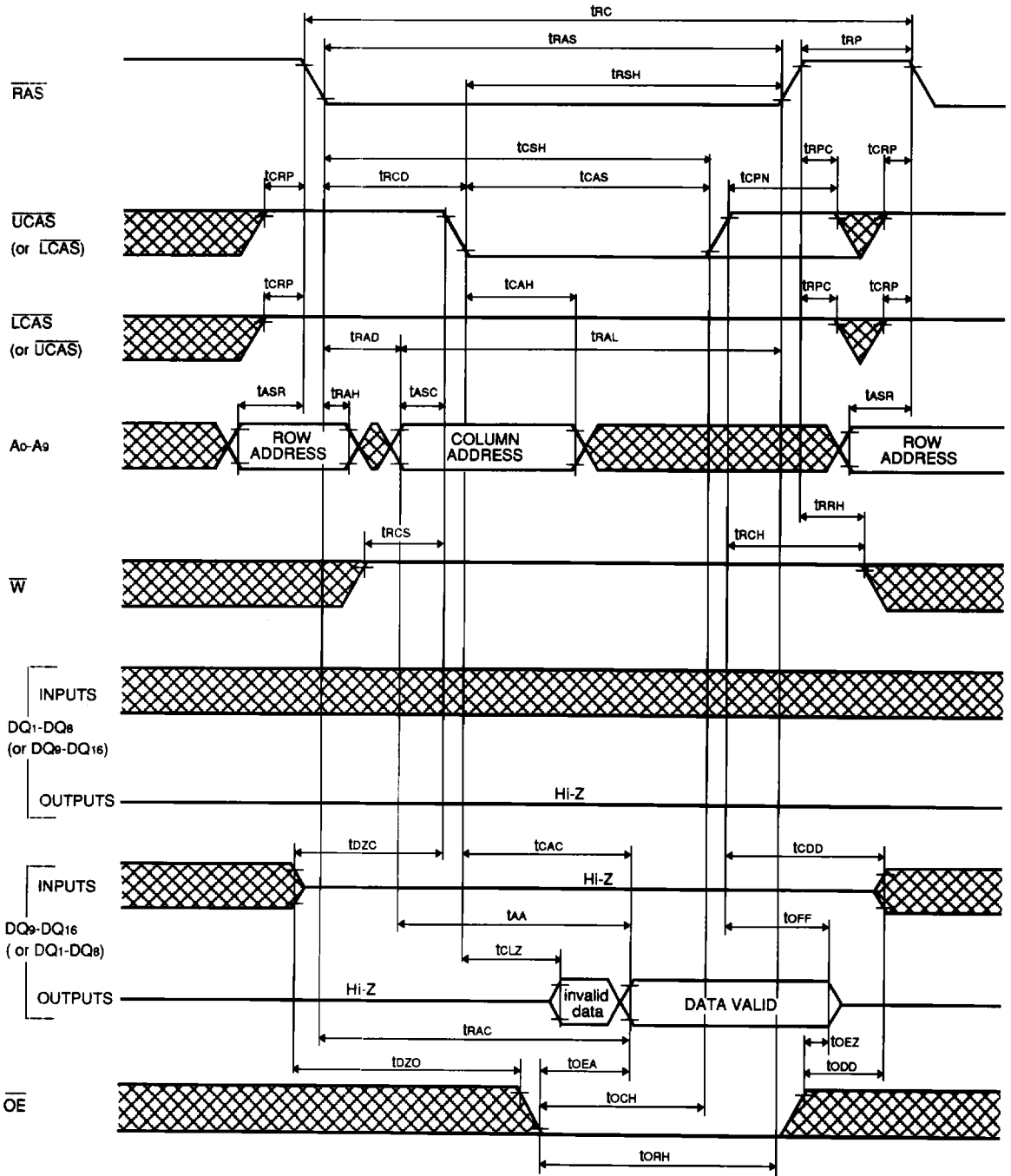
**Timing Diagrams (Note 28)
 Read Cycle**



- Note 28**
-  Indicates the don't care input.
 $V_{IH(min.)} \leq V_{IN} \leq V_{IH(max.)}$ or $V_{IL(min.)} \leq V_{IN} \leq V_{IL(max.)}$
 -  Indicates the invalid output.
 -  Indicates the skew of the two inputs.

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

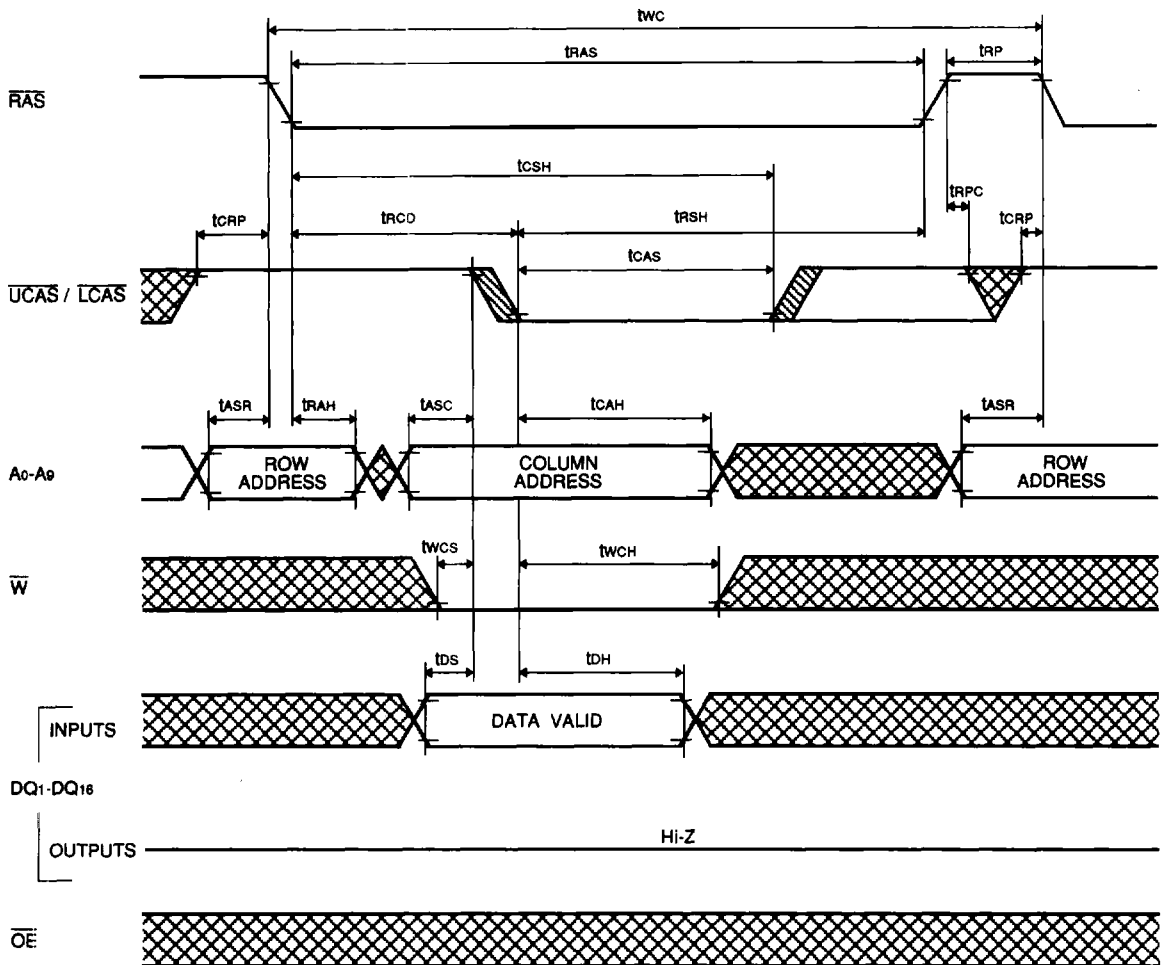
Upper / (Lower) Byte Read Cycle



M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

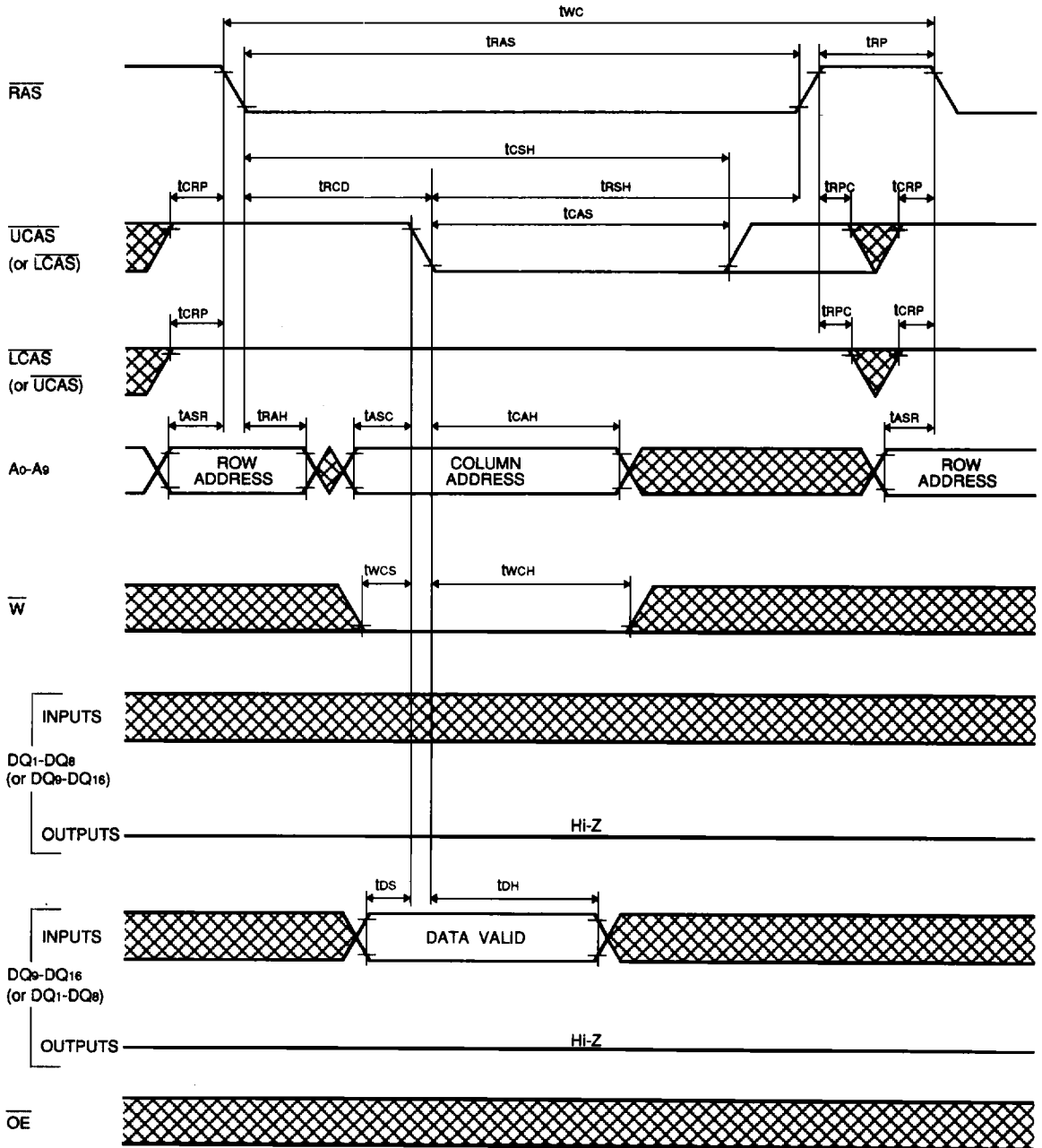
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Write Cycle (Early write)



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

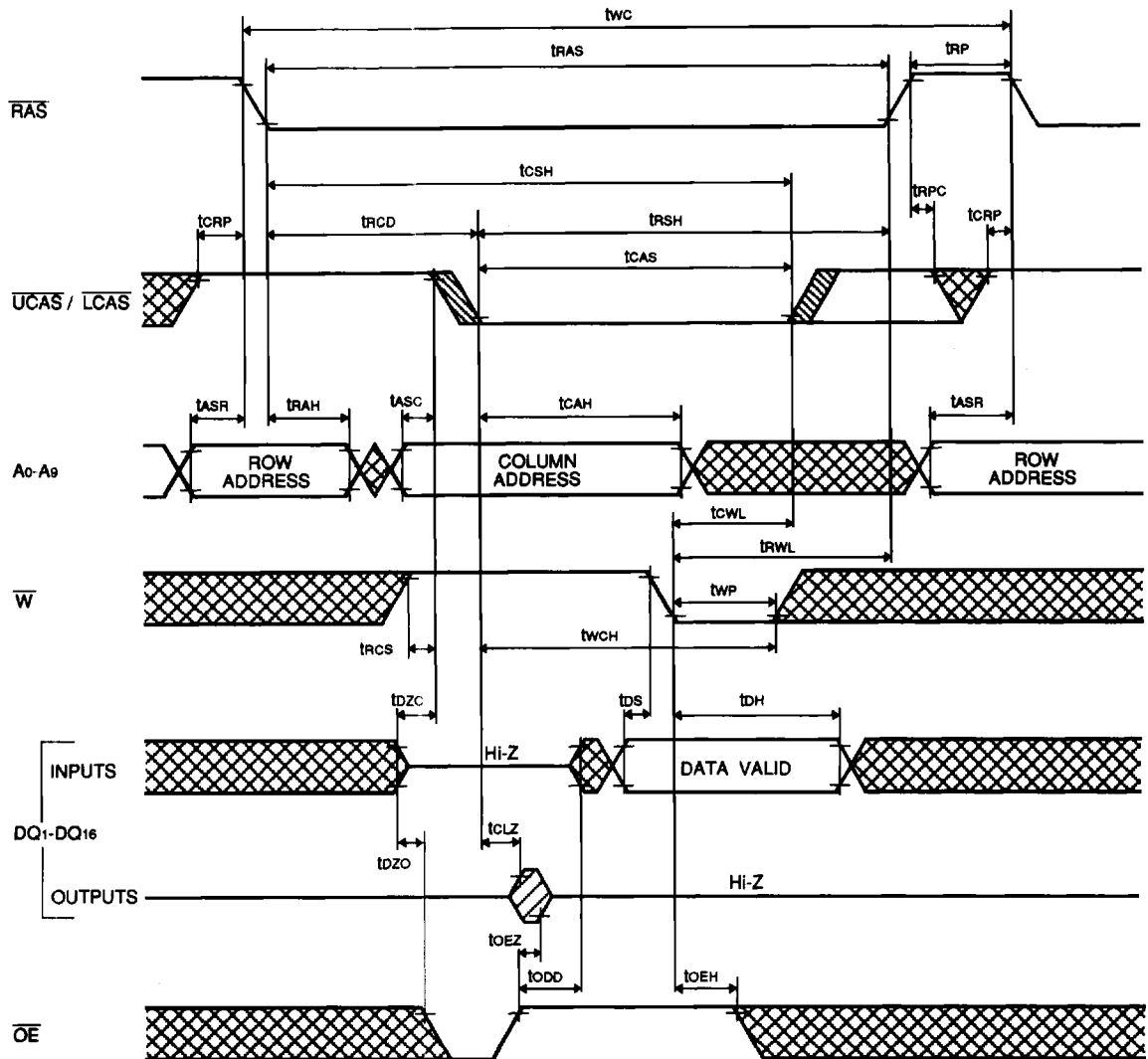
Upper/(Lower) Byte Write Cycle (Early write)



M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

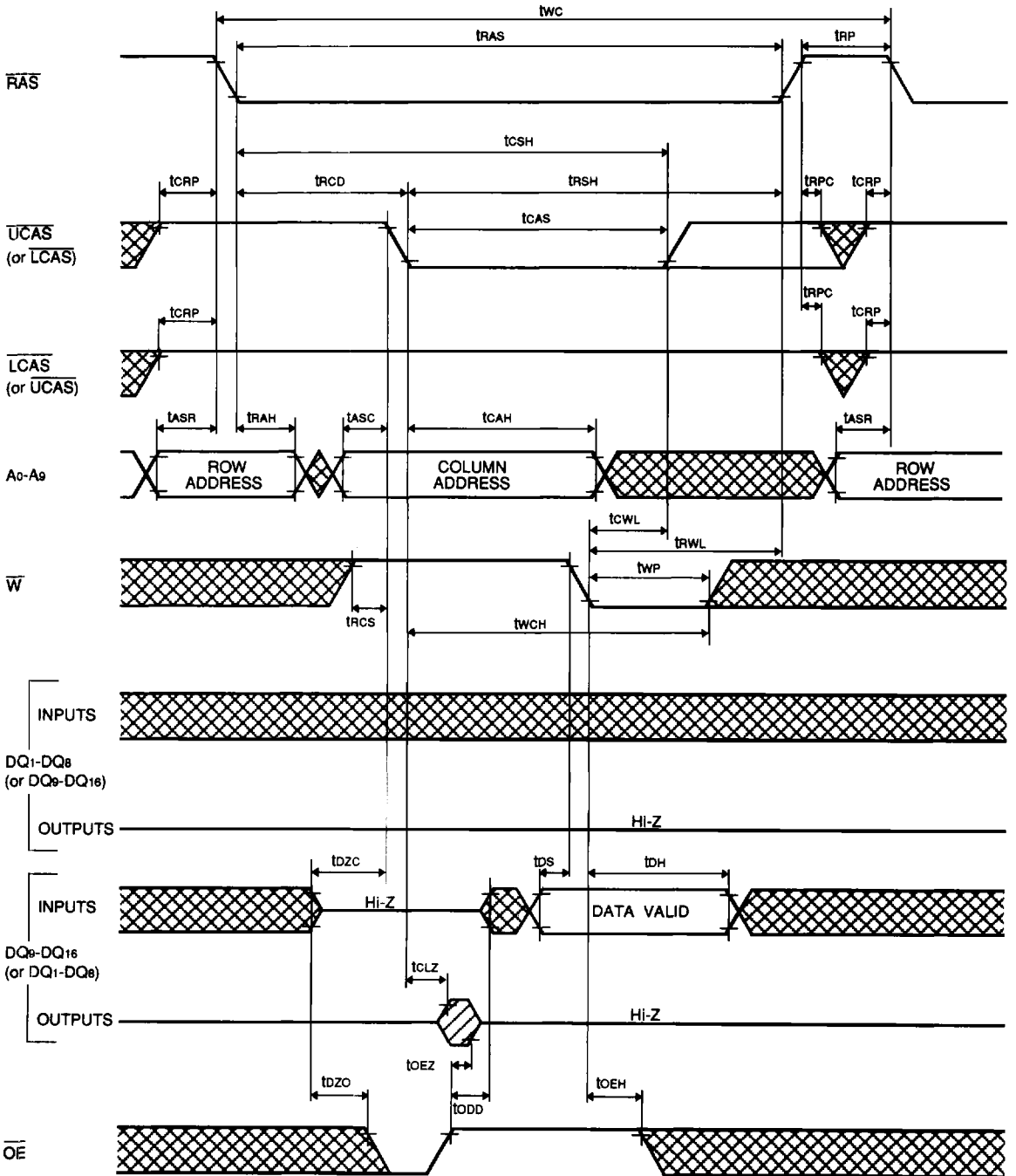
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Write Cycle (Delayed write)



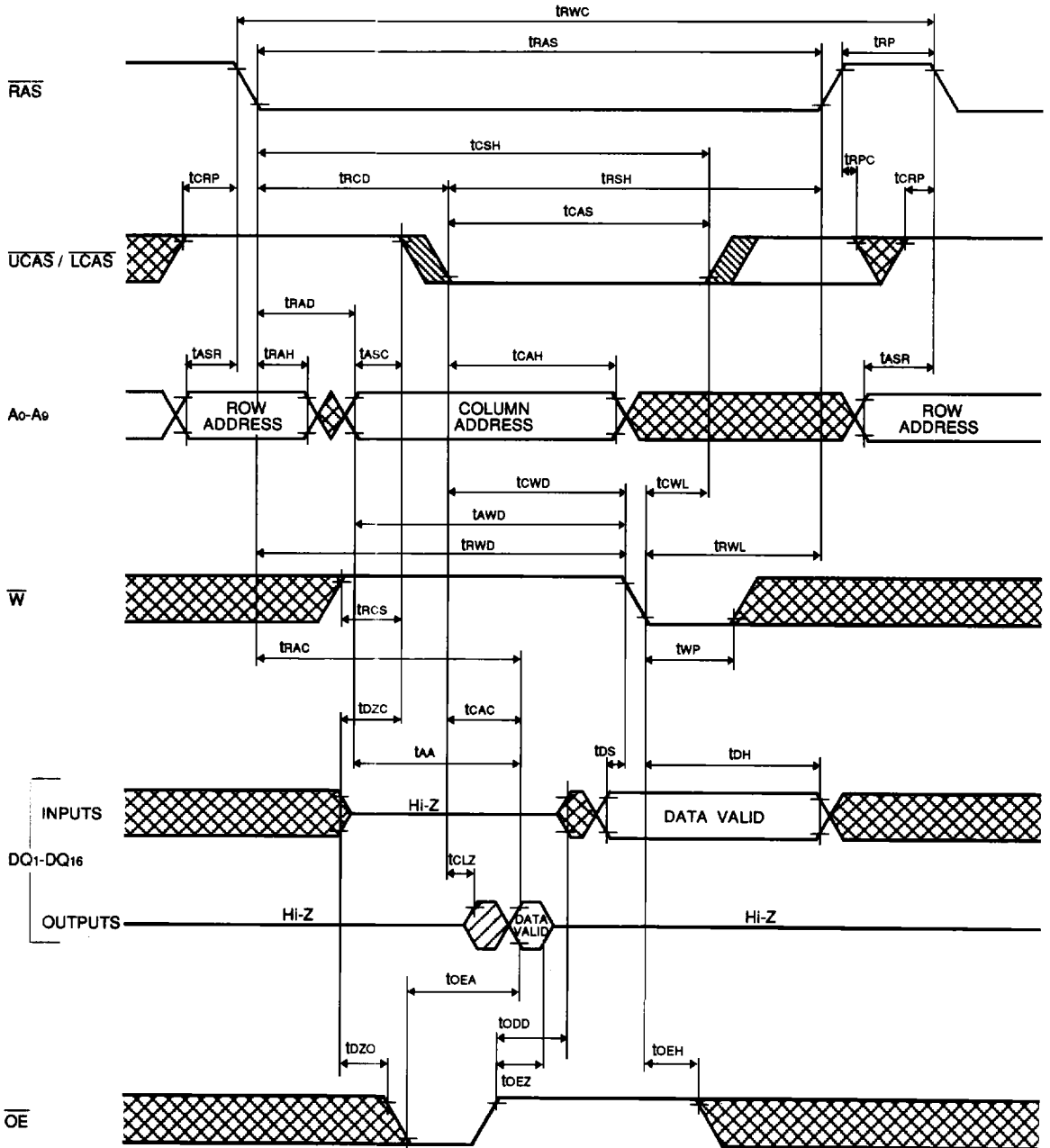
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Byte Write Cycle (Delayed write)



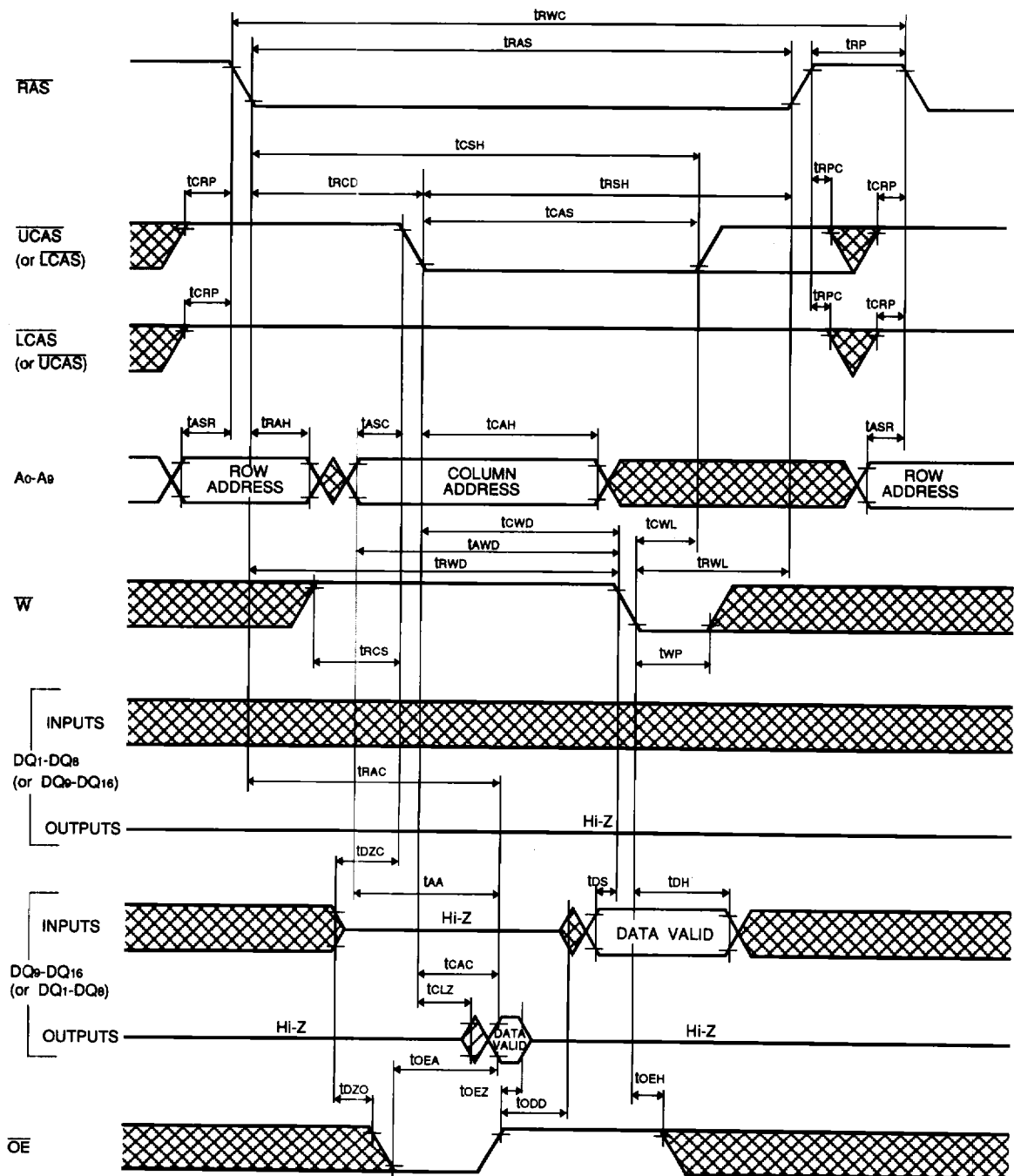
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read-Write, Read-Modify-Write Cycle



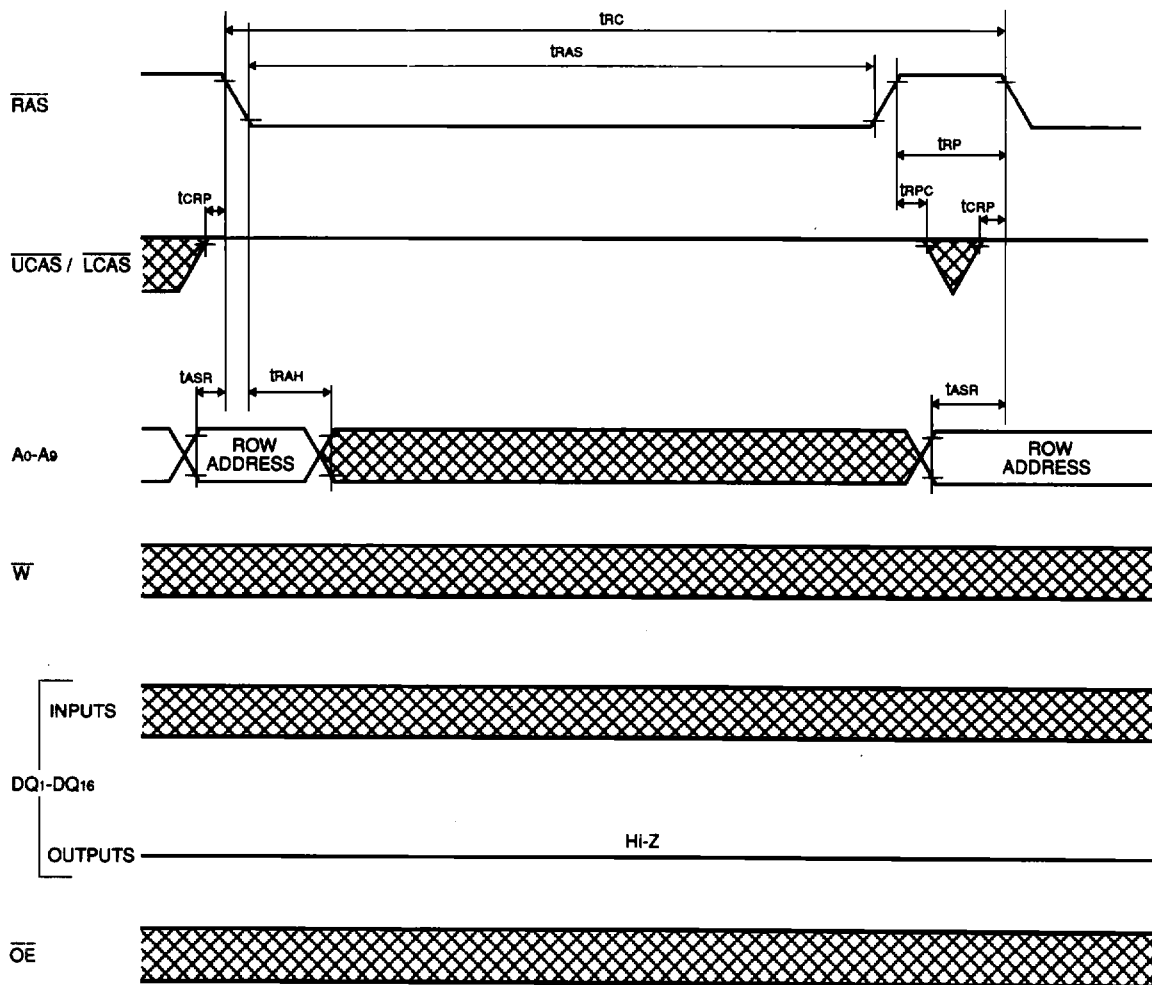
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



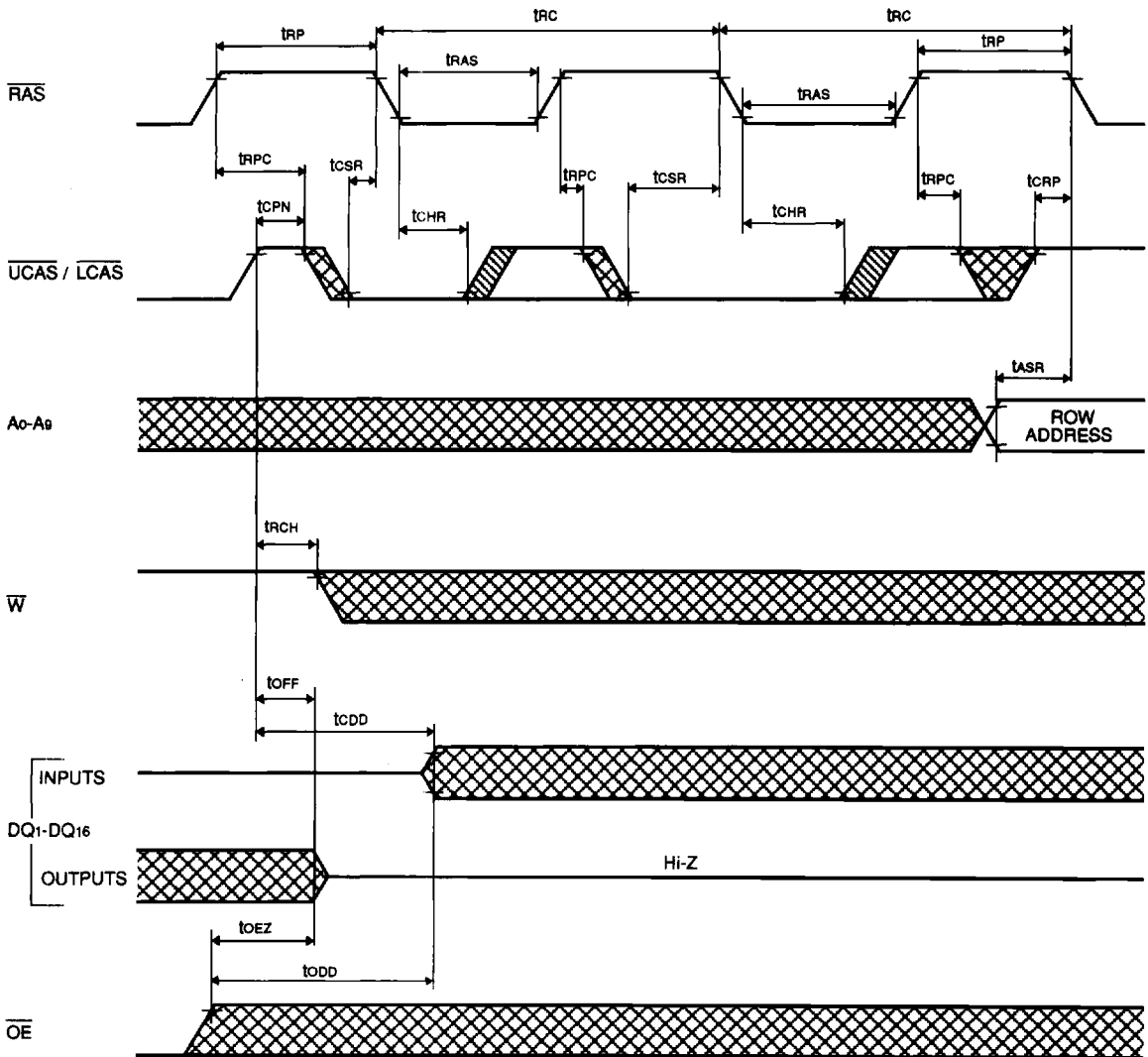
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

RAS-only Refresh Cycle



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

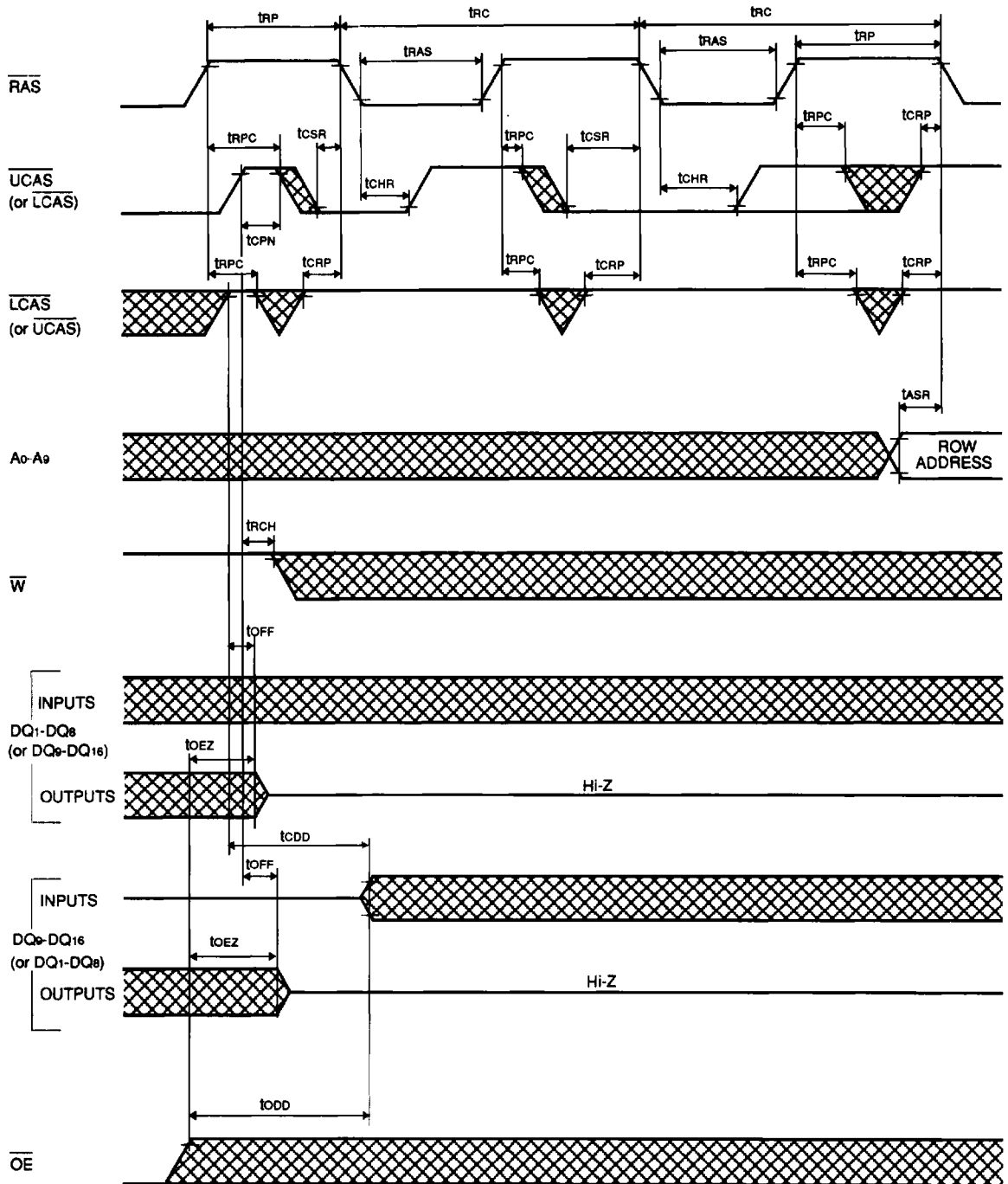
CAS before RAS Refresh Cycle



M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

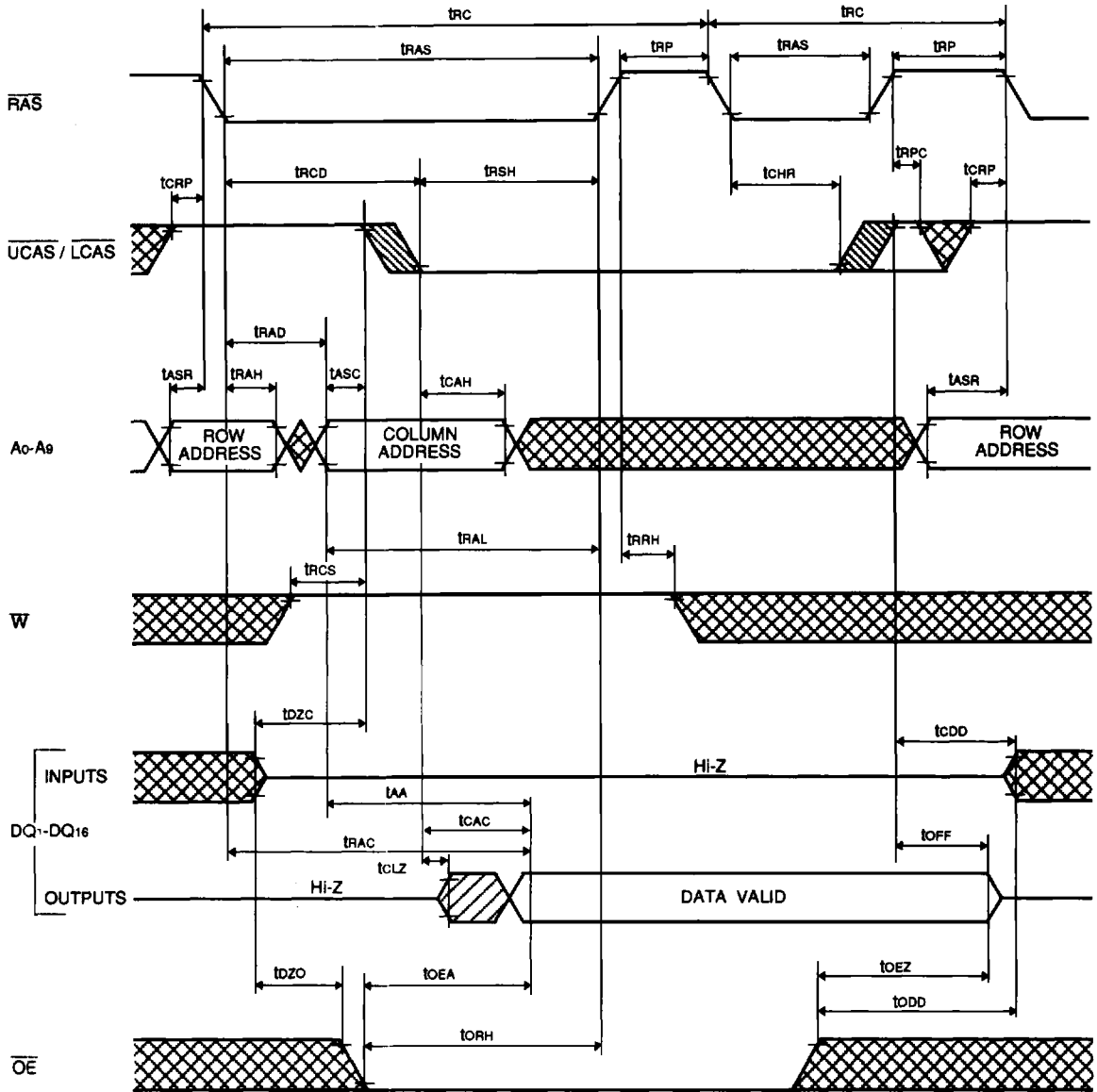
Upper/(Lower) CAS before RAS Refresh Cycle



M5M418160BJ, TP, RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

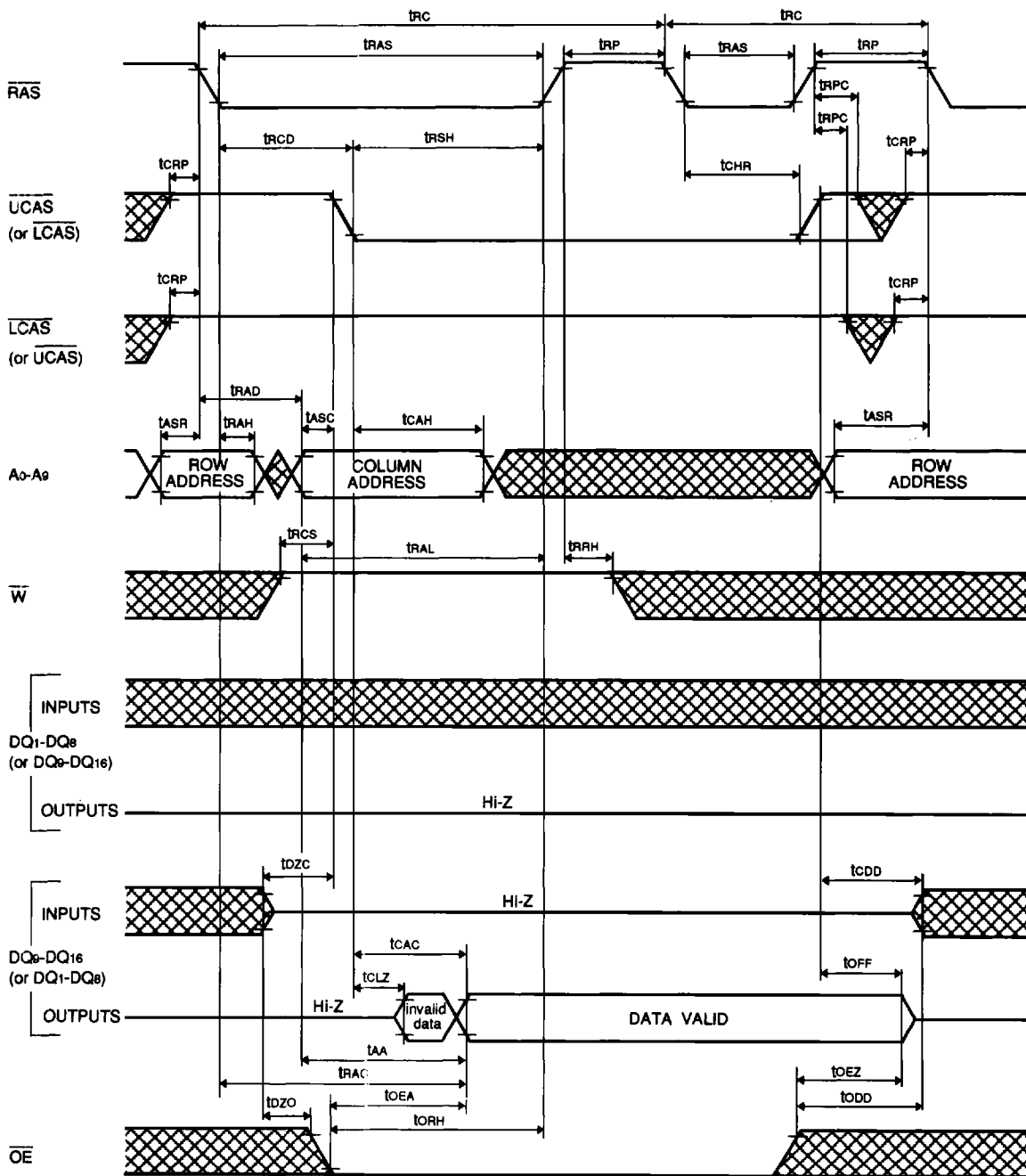
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)

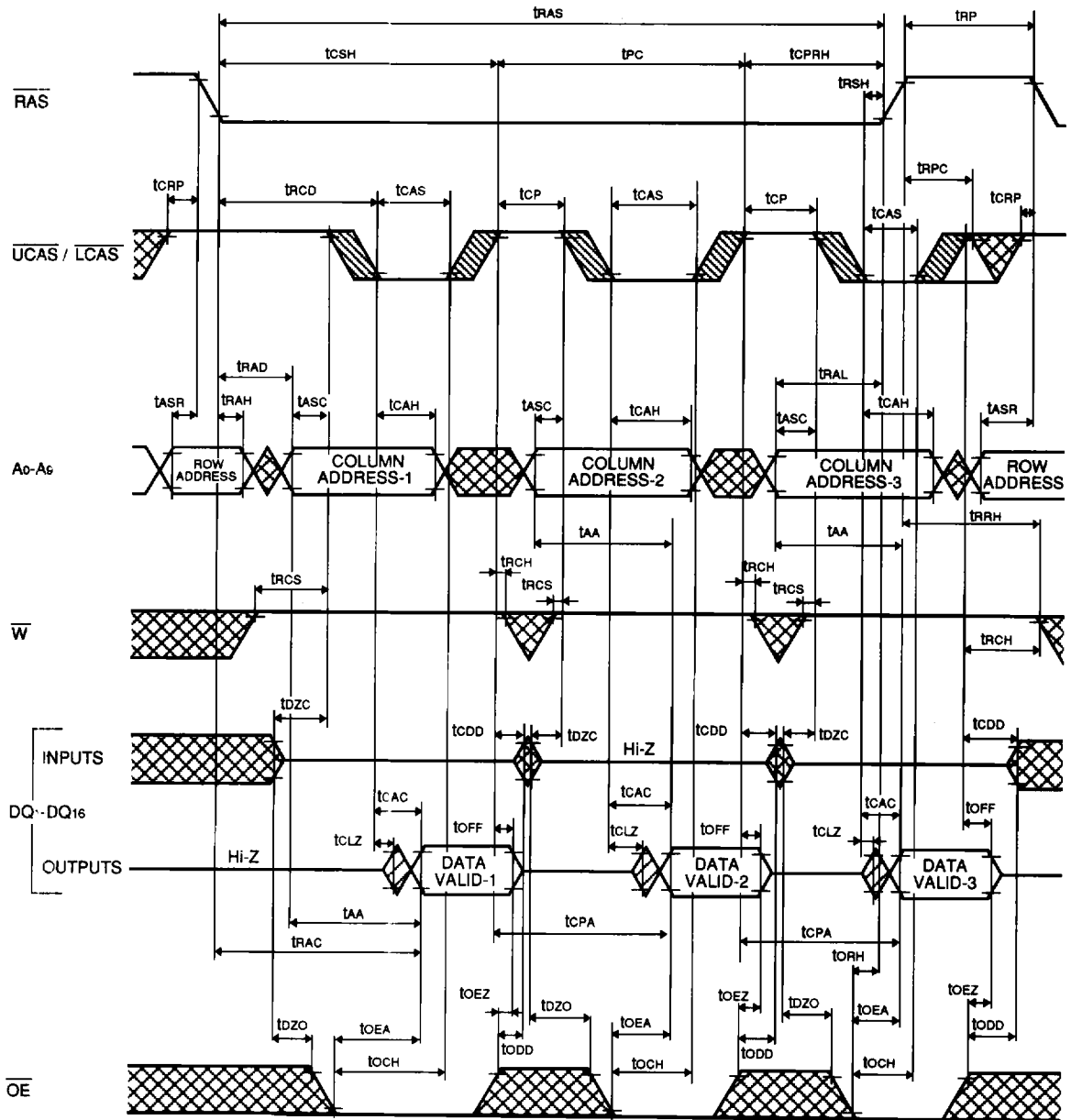


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

M5M418160BJ,TP,RT-6,-7,-8,-8S,-7S,-8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

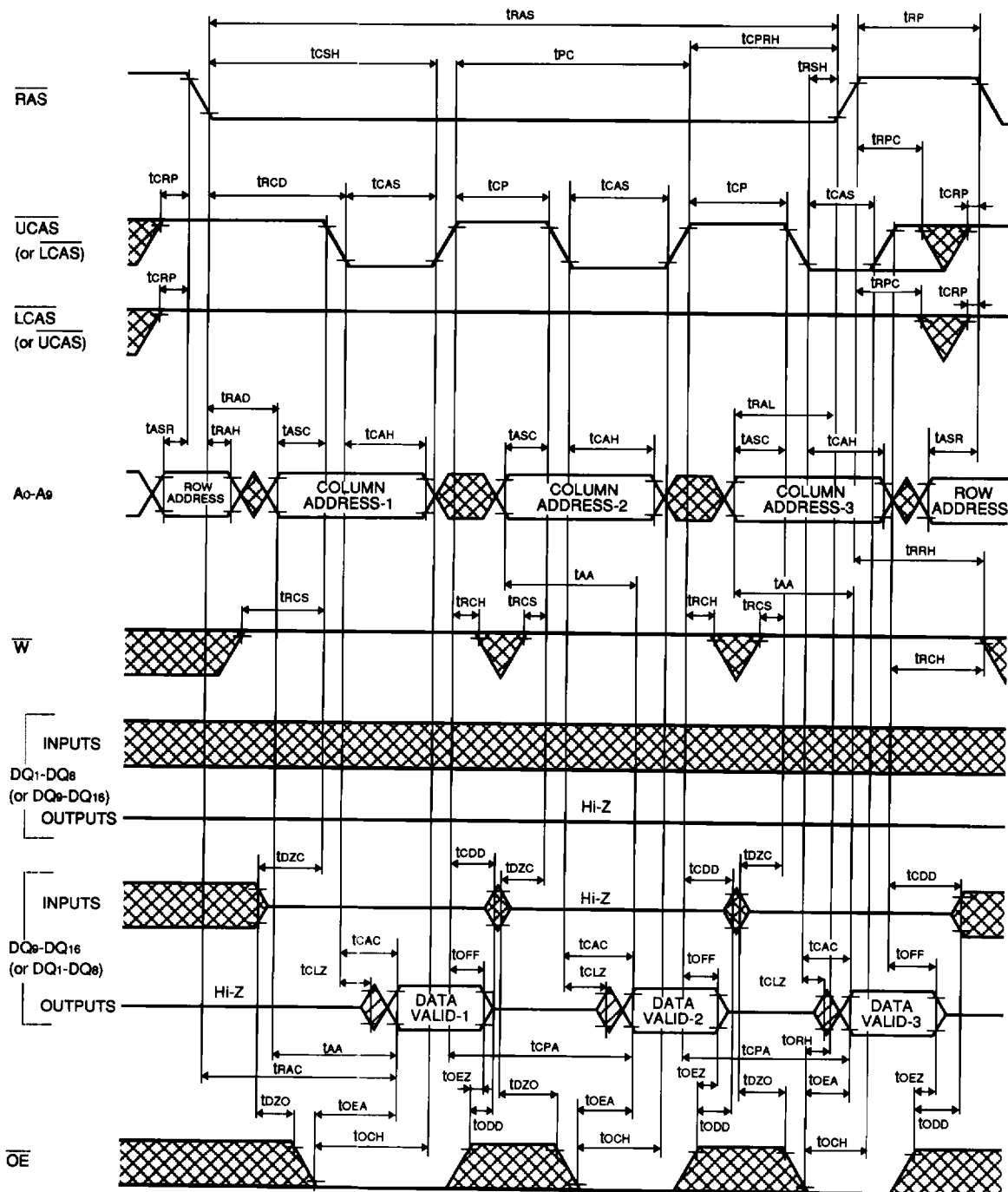
Fast Page Mode Read Cycle



M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

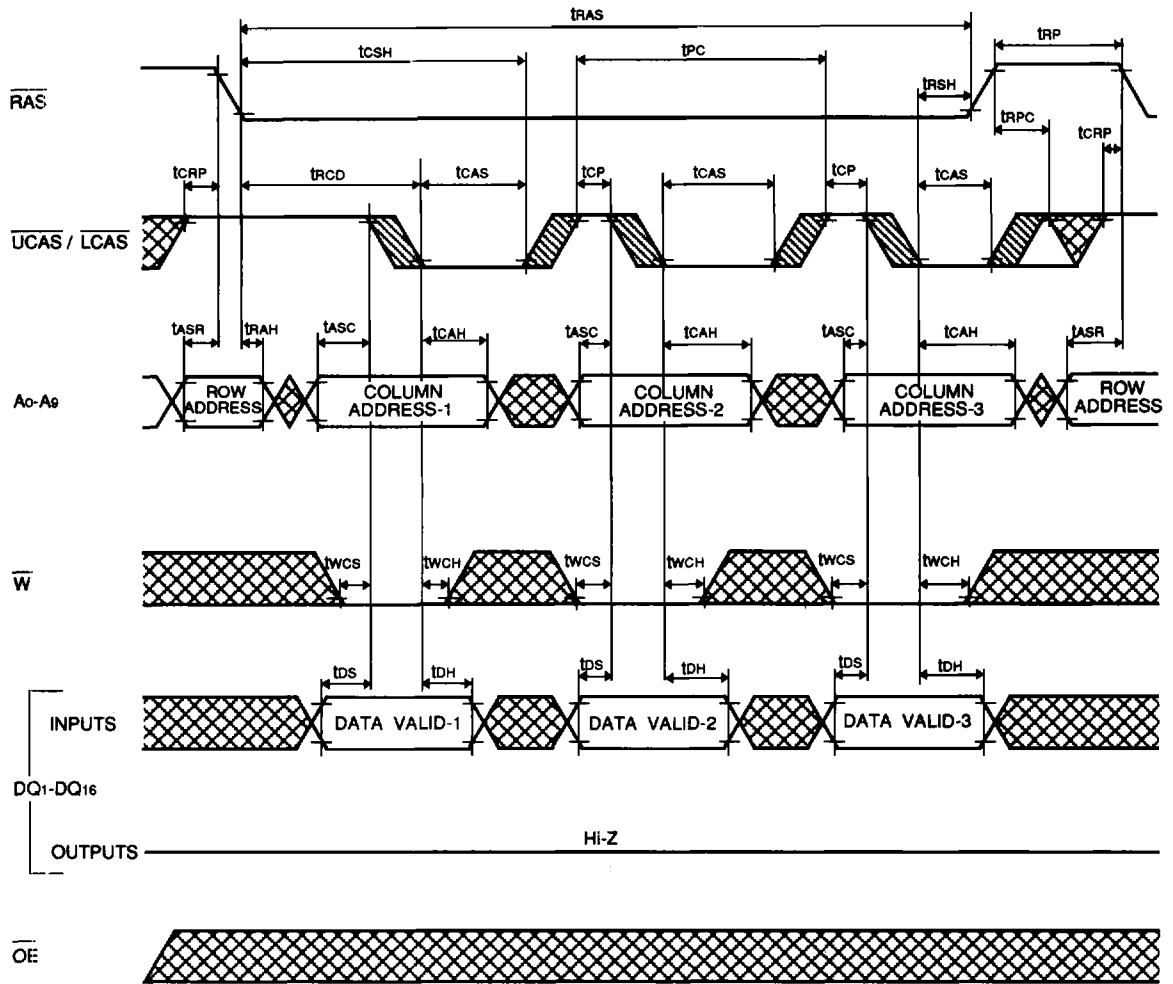
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Fast Page Mode Read Cycle



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

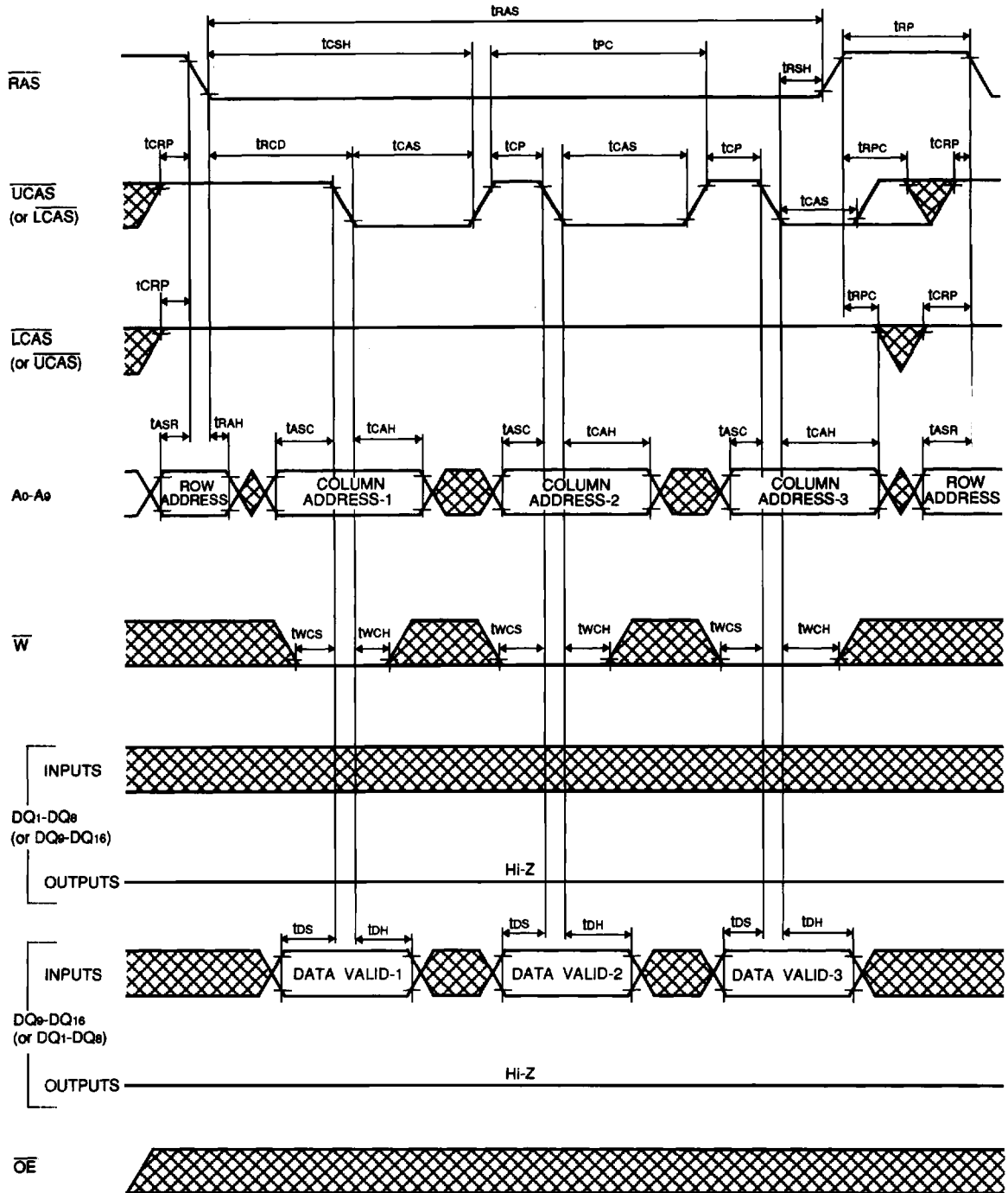
Fast Page Mode Write Cycle (Early Write)



M5M418160BJ,TP,RT-6,-7,-8,-6IS,-7IS,-8IS

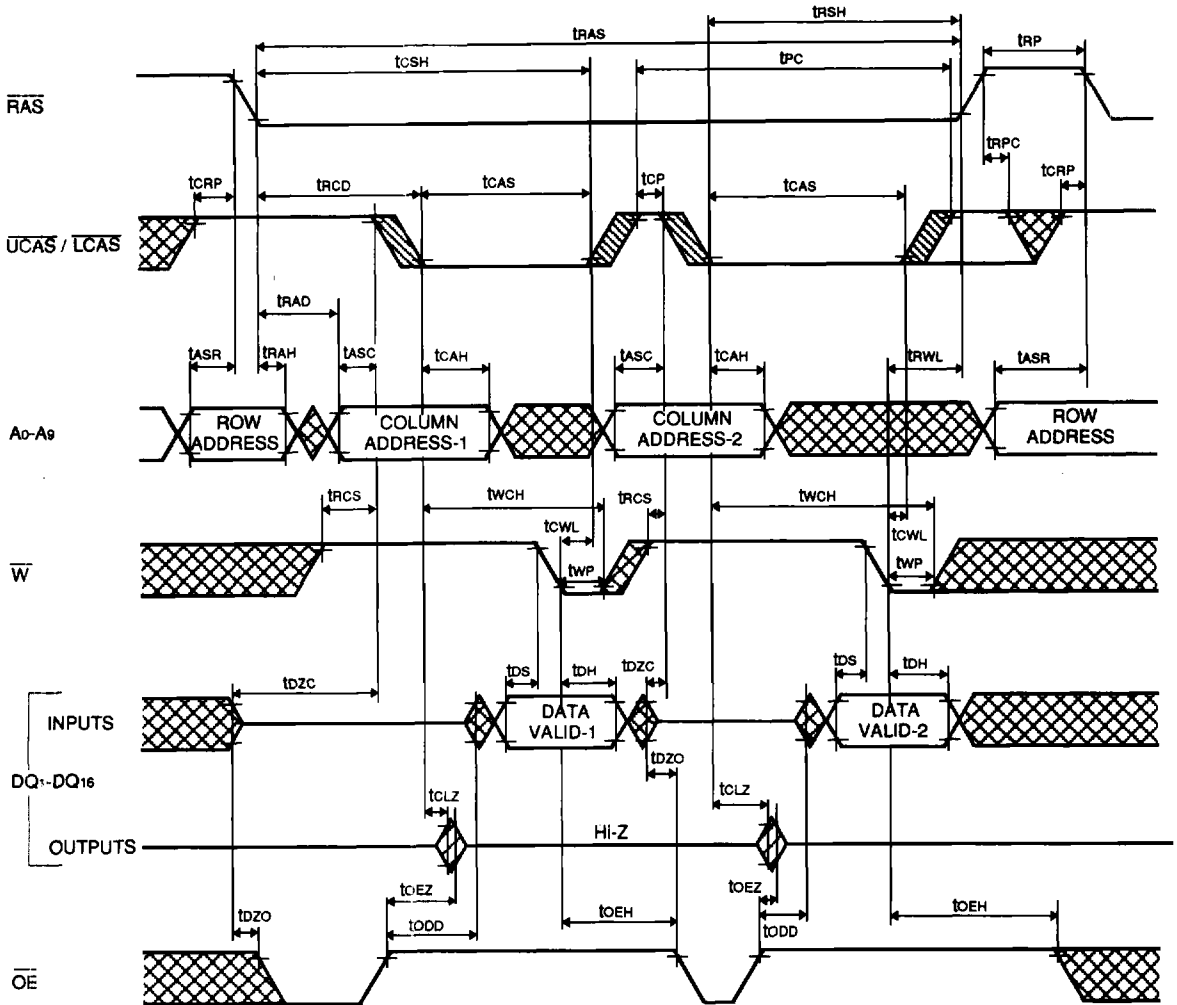
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



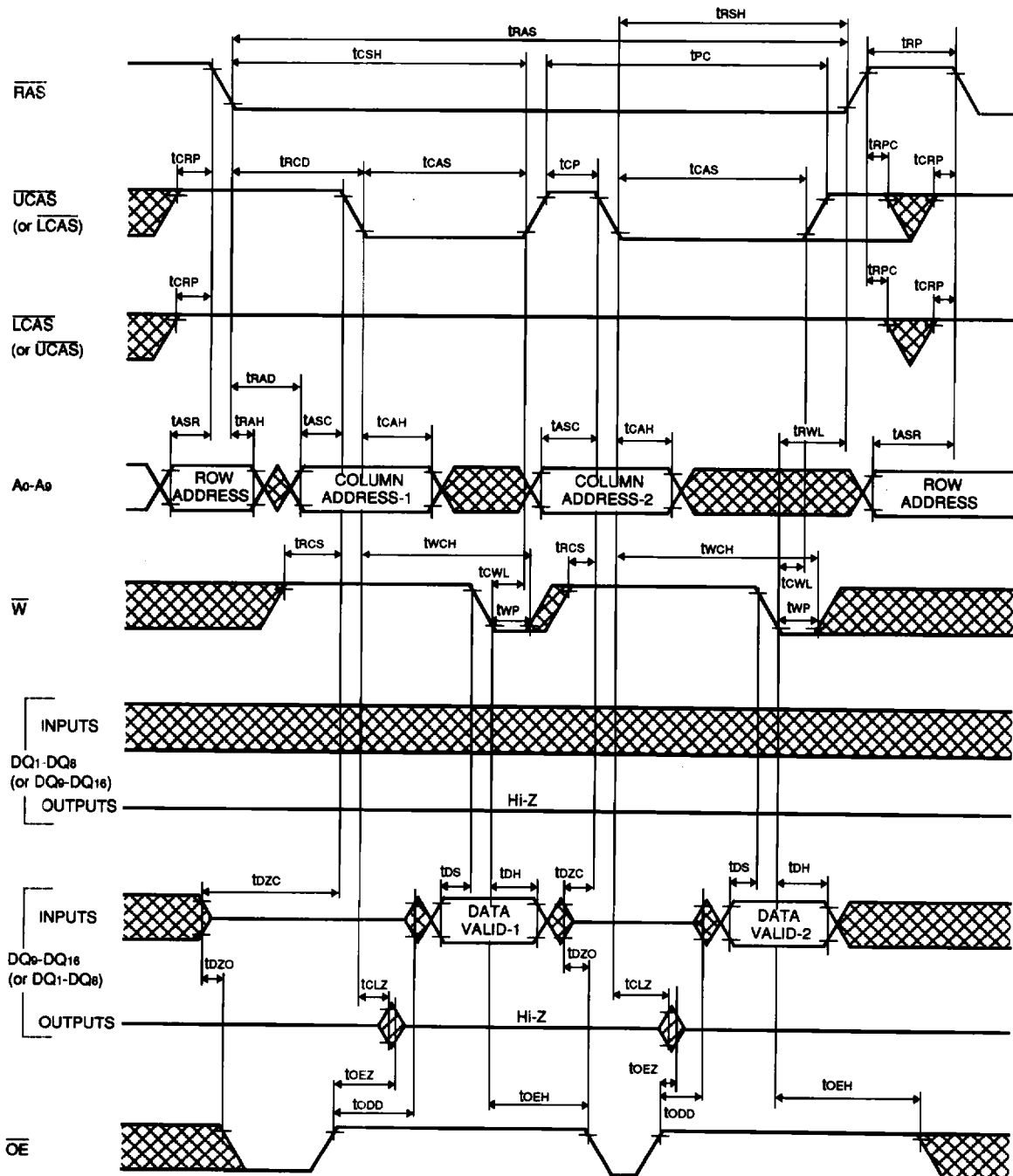
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Write Cycle (Delayed Write)



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

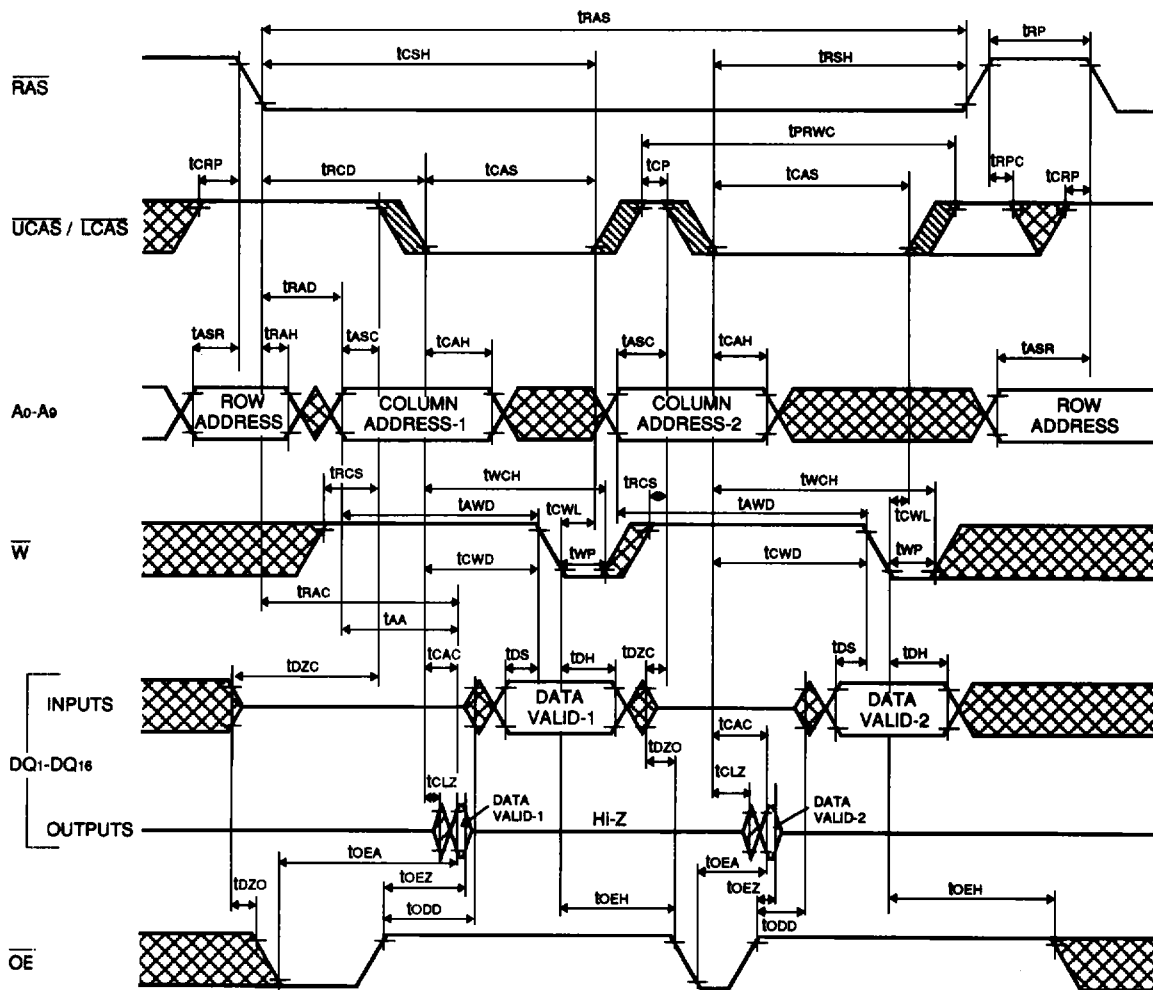
Fast Page Mode Upper / (Lower) Byte Write (Delayed Write)



M5M418160BJ, TP, RT-6, -7, -8, -8S, -7S, -8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

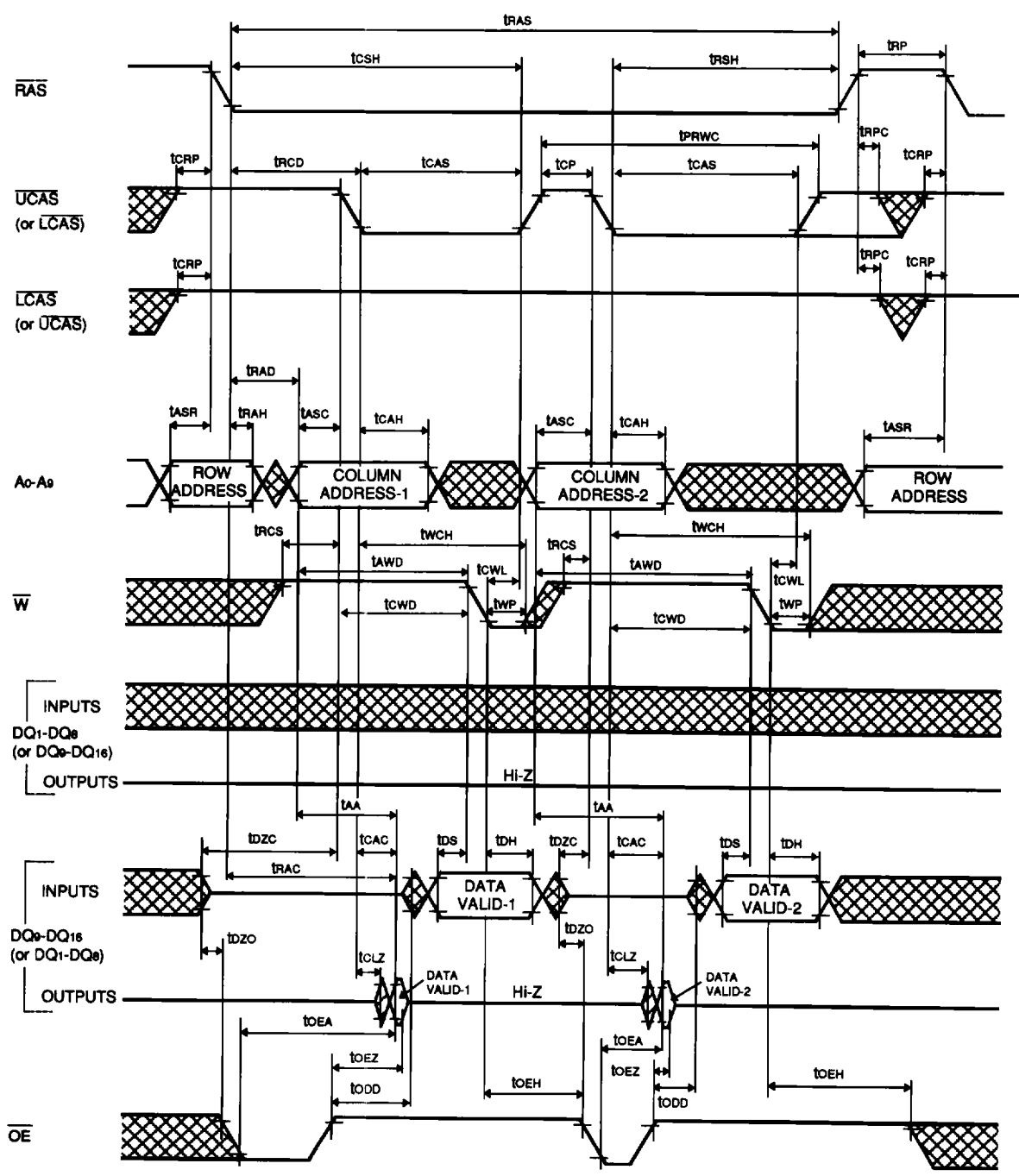
Fast Page Mode Read-Write, Read-Modify-Write Cycle



M5M418160BJ, TP, RT-6, -7, -8, -6S, -7S, -8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S / -8S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I _{CCS} (AV)	Average supply current from V _{CC} Self-Refresh cycle	M5M418160B -6S,-7S,-8S $\overline{RAS} = \overline{CAS} \leq 0.2V$			400	μA

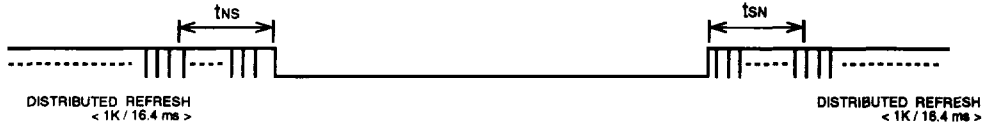
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418160B-6S		M5M418160B-7S		M5M418160B-8S		
		Min	Max	Min	Max	Min	Max	
t _{RAS}	Self Refresh \overline{RAS} low pulse width	100		100		100		μs
t _{RPS}	Self Refresh \overline{RAS} high precharge time	90		110		130		ns
t _{CHS}	Self Refresh \overline{RAS} hold time	-50		-50		-50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

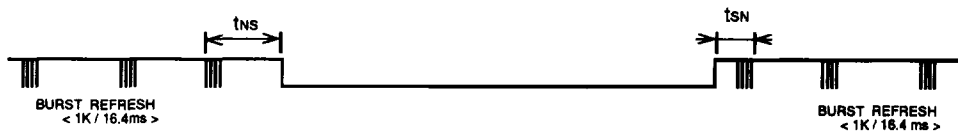
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} ≤ 16.4 ms and t_{SN} ≤ 16.4 ms.



(2) In case of burst refresh

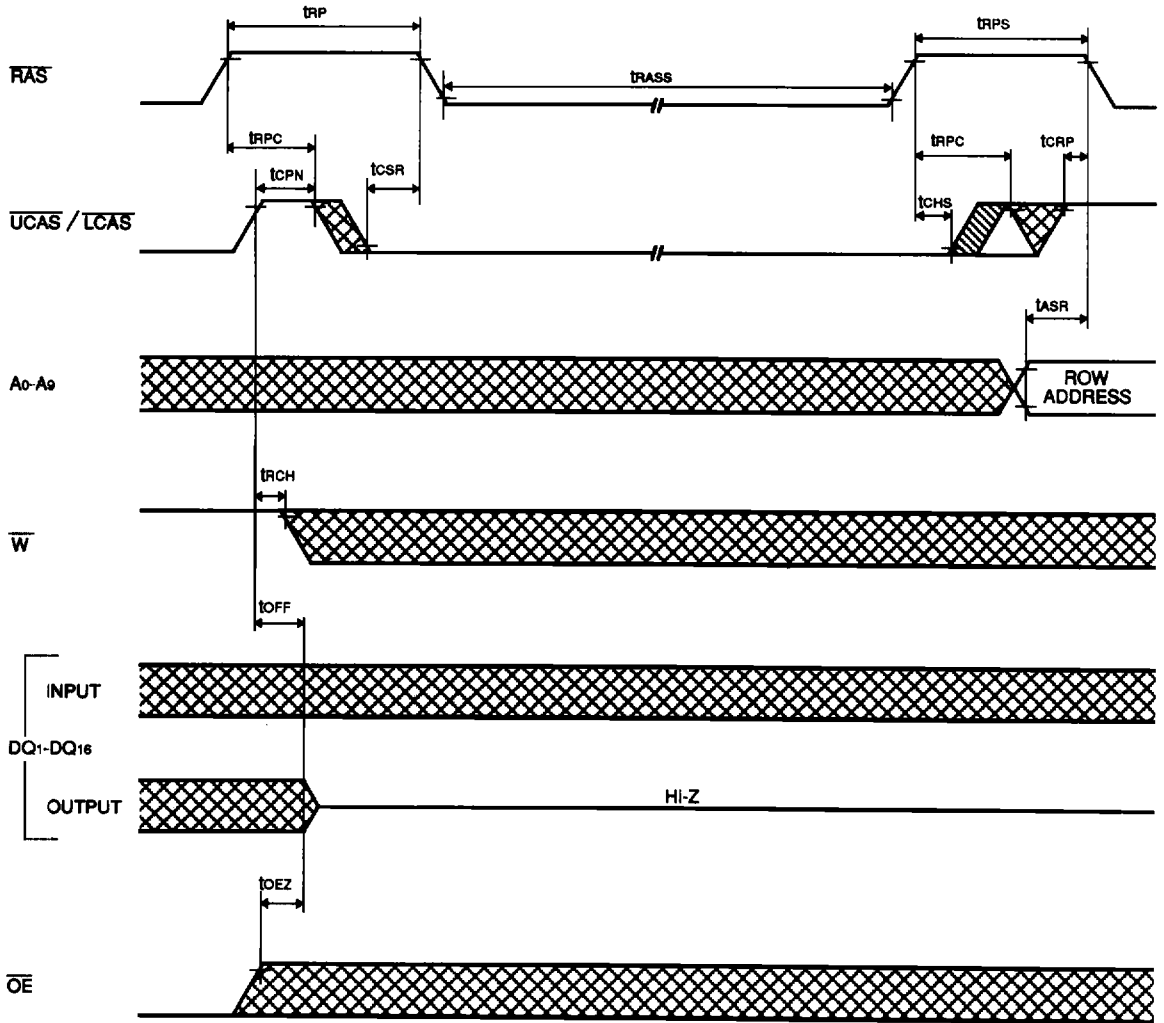
The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} + t_{SN} ≤ 16.4 ms.



M5M418160BJ,TP,RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Self Refresh Cycle



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Self Refresh Cycle*

