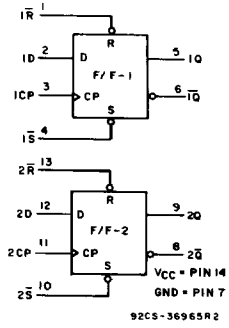
CD54AC74/3A
CD54ACT74/3A

Dual D-type Flip-Flop with Set and Reset

The RCA CD54AC74/3A and CD54ACT74/3A are dual D-type, positive-edge-triggered flip-flops that utilize the new RCA ADVANCED CMOS LOGIC technology. These flip-flops have independent DATA , $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The CD54AC74/3A and CD54ACT74/3A are supplied in 14-lead dual-in-line ceramic packages (F suffix).

Package Specifications
(See Section 11, Fig. 10)



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
					+25		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (FF)	I_{CC}	V_{CC} or GND	0	5.5	—	4•	—	80•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D	0.53
$\overline{R}$, $\overline{S}$	0.58
CP	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT74	5,6,8,9	1-4,7,10-13	14	5,6,9	7	1-4,10-14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	25 kHz
CD54AC/ACT74	—	7	5,6,8,9	1,4,10,13,14	3,11	2,12

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC74/3A
CD54ACT74/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays, CP to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.2 3	125 14 10•	ns
R, S to Q, $\overline{Q}$	t_{PLH}	1.5 3.3 5	— 4.4 3.15	132 14.7 10.5•	ns
	t_{PHL}	1.5 3.3 5	— 4.8 3.4	144 16.1 11.5•	ns
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays, CP to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5†	2.9	9.5•	ns
$\overline{R}$, $\overline{S}$ to Q	t_{PLH}	5	3.5	11.5•	ns
	t_{PHL}	5	3.8	12.5•	
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
For AC, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$
For ACT, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where
f_i = input frequency
f_o = output frequency
C_L = output load capacitance
C = supply voltage

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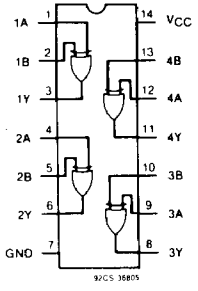
Quad 2-Input Exclusive-OR Gate

CD54AC86/3A
CD54ACT86/3A

The RCA CD54AC86/3A and CD54ACT86/3A are quad 2-input Exclusive-OR gates that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC86/3A and CD54ACT86/3A are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC86/3A and CD54ACT86/3A are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications

See Section 11, Fig. 10