QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS Quad 2-Input Multiplexers

QS54/74FCT157T
QS54/74FCT158T
QS54/74FCT257T
QS54/74FCT2157T
QS54/74FCT2257T

FEATURES/BENEFITS

- Pin and function compatible to the 74FCT257, 74FCT157/8 and 74FCT2157/2257
- Industrial temperature –40°C to 85°C
- CMOS power levels: <7.5mW static
- Available in DIP, SOIC, QSOP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 157T, 158T, 257T

- JEDEC-FCT spec compatible
- A and C speed grades with 4.3ns for C
- I_{OL} = 48mA Ind., 32mA Mil.

FCT-T 2157T, 2257T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades with 4.3ns for C
- I_{OL} = 12mA Ind.

DESCRIPTION

The QSFCT157T/8T and QSFCT257T are high-speed CMOS TTL-compatible, quad, 2-input multiplexers. The 157/257 parts are non-inverting; the 158 is inverting. The 157/8 has TTL outputs; the 257 has 3-state outputs. The QSFCT2157T and QSFCT2257T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

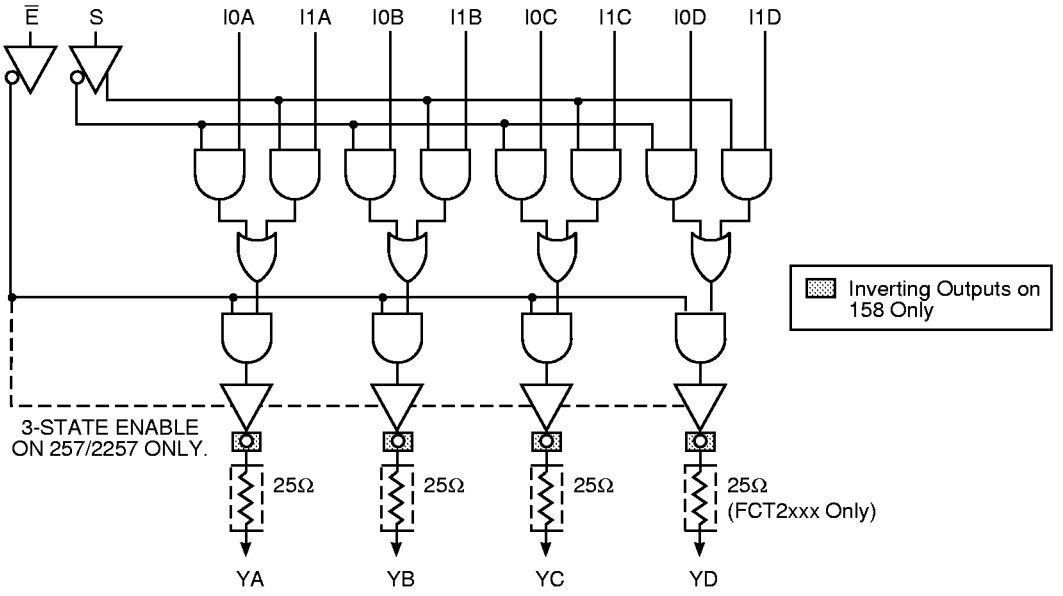
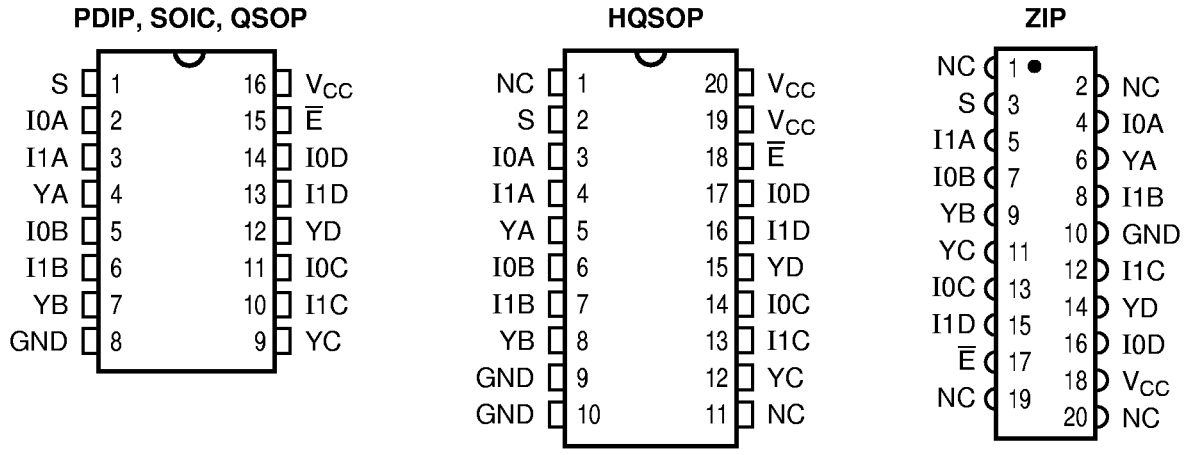


Figure 2. Pin Configurations (All Pins Top View)



Note:
Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

Table 1. Pin Description

Name	I/O	Description
Ixx	I	Data Inputs
S	I	Select Input
$\overline{E}$	I	Enable Input
YA-YD	O	Data Outputs

Table 2. Function Tables

		FCT157/2157				FCT158				
$\overline{E}$	S	YA	YB	YC	YD	YA	YB	YC	YD	Function
H	X	L	L	L	L	H	H	H	H	Disable
L	L	I0A	I0B	I0C	I0D	$\overline{I0A}$	$\overline{I0B}$	$\overline{I0C}$	$\overline{I0D}$	Select 0
L	H	I1A	I1B	I1C	I1D	$\overline{I1A}$	$\overline{I1B}$	$\overline{I1C}$	$\overline{I1D}$	Select 1

		FCT257/2257				
$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	Select 1

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance(1)

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins(2)	SOIC	QSOP	PDIP	ZIP	Unit
1-3, 5, 6, 10, 11, 13-15	4	4	5	7	pF
4, 7, 9, 12	8	8	9	10	pF

Notes:
1. Capacitance is characterized but not tested.
2. Pin reference for 16-pin package.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions(1)	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC}-0.2V ≤ V_{IN} ≤ V_{CC}	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V, freq = 0(2)	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	V_{CC} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC}(3,4)	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z) (257, 2257)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	V_{CC} = Max., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = –12mA (MIL) I_{OH} = –15mA (IND)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	V_{CC} = Min. I_{OL} = 32mA (MIL) I_{OL} = 48mA (IND)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX- 25Ω)	V_{CC} = Min. I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX- 25Ω)	V_{CC} = Min. I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

Table 7. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		2257		157/8A 257A 2157A 2257A		157/8C 257C 2157C 2257C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	Ind	1.5	6.0	1.5	5.0	1.5	4.3	ns
t_{PHL}	In to Y, 157/8/257	Mil	1.5	7.0	1.5	5.8	1.5	5.0	
t_{PLH}	Propagation Delay	Ind	1.5	6.0	1.5	5.0	1.5	4.3	ns
t_{PHL}	In to Y, 2157/2257	Mil	1.5	7.0	1.5	5.8	1.5	5.0	
t_{PLH}	Propagation Delay	Ind	1.5	10.5	1.5	7.0	1.5	5.2	ns
t_{PHL}	S to Y, 157/8/257	Mil	1.5	12	1.5	8.1	1.5	6.0	
t_{PLH}	Propagation Delay	Ind	1.5	10.5	1.5	7.0	1.5	5.2	ns
t_{PHL}	S to Y, 2157/2257	Mil	1.5	12	1.5	8.1	1.5	6.0	
t_{PLH}	Propagation Delay	Ind	1.5	10.5	1.5	6.0	1.5	4.8	ns
t_{PHL}	$\overline{E}$ to Yi, 157/8	Mil	1.5	12	1.5	7.4	1.5	5.9	
t_{PLH}	Propagation Delay	Ind	1.5	10.5	1.5	6.0	1.5	4.8	ns
t_{PHL}	$\overline{E}$ to Yi, 2157	Mil	1.5	12	1.5	7.4	1.5	5.9	
t_{PZH}	Ouput Enable Time	Ind	1.5	8.5	1.5	7.0	1.5	6.0	ns
t_{PZL}	$\overline{E}$ to Yi, 257	Mil	1.5	10	1.5	8.0	1.5	6.8	
t_{PZH}	Output Enable Time	Ind	1.5	8.5	1.5	7.0	1.5	6.0	ns
t_{PZL}	$\overline{E}$ to Yi, 2257	Mil	1.5	10	1.5	8.0	1.5	6.8	
t_{PHZ}	Output Disable Time	Ind[2]	1.5	6.0	1.5	5.5	1.5	5.0	ns
t_{PLZ}	$\overline{E}$ to Yi, 257/2257	Mil[2]	1.5	8.0	1.5	5.8	1.5	5.3	

Notes:
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.