HARRIS Semiconductor

CD74FCT16373T, CD74FCT162373T, CD74FCT162H373T

February 1998

Fast CMOS 16-Bit Transparent Latches

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices Are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16373T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162373T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162H373T**
  - **Bus Hold Retains Last Active Bus State During Three-State**
  - **Eliminates the Need for External Pull-up Resistors**

Description

These devices are 16-bit transparent latches designed with three-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the setup time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74FCT16373T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162373T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H373T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16373ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373DTSM	-40 to585	48 Ld SSOP	M48.300-P
CD74FCT162373ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162H373ATMT	-40 to 85	48 Ld TSSOP	M56.240-P
CD74FCT162H373ATSM	-40 to 85	48 Ld SSOP	M56.300-P
CD74FCT162H373CTMT	-40 to 85	48 Ld TSSOP	M56.240-P
CD74FCT162H373CTSM	-40 to 85	48 Ld SSOP	M56.300-P
CD74FCT162H373DTMT	-40 to 85	48 Ld TSSOP	M56.240-P
CD74FCT162H373DTSM	-40 to 85	48 Ld SSOP	M56.300-P
CD74FCT162H373ETMT	-40 to 85	48 Ld TSSOP	M56.240-P
CD74FCT162H373ETSM	-40 to 85	48 Ld SSOP	M56.300-P
CD74FCT162H373TMT	-40 to 85	48 Ld TSSOP	M56.240-P
CD74FCT162H373TSM	-40 to 85	48 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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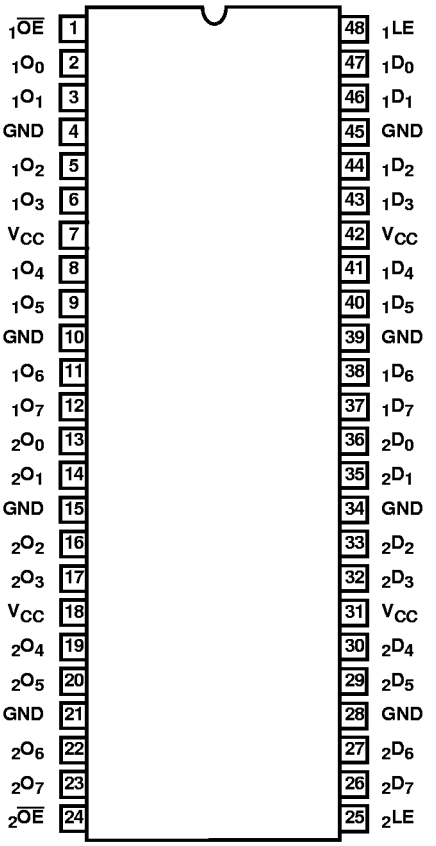
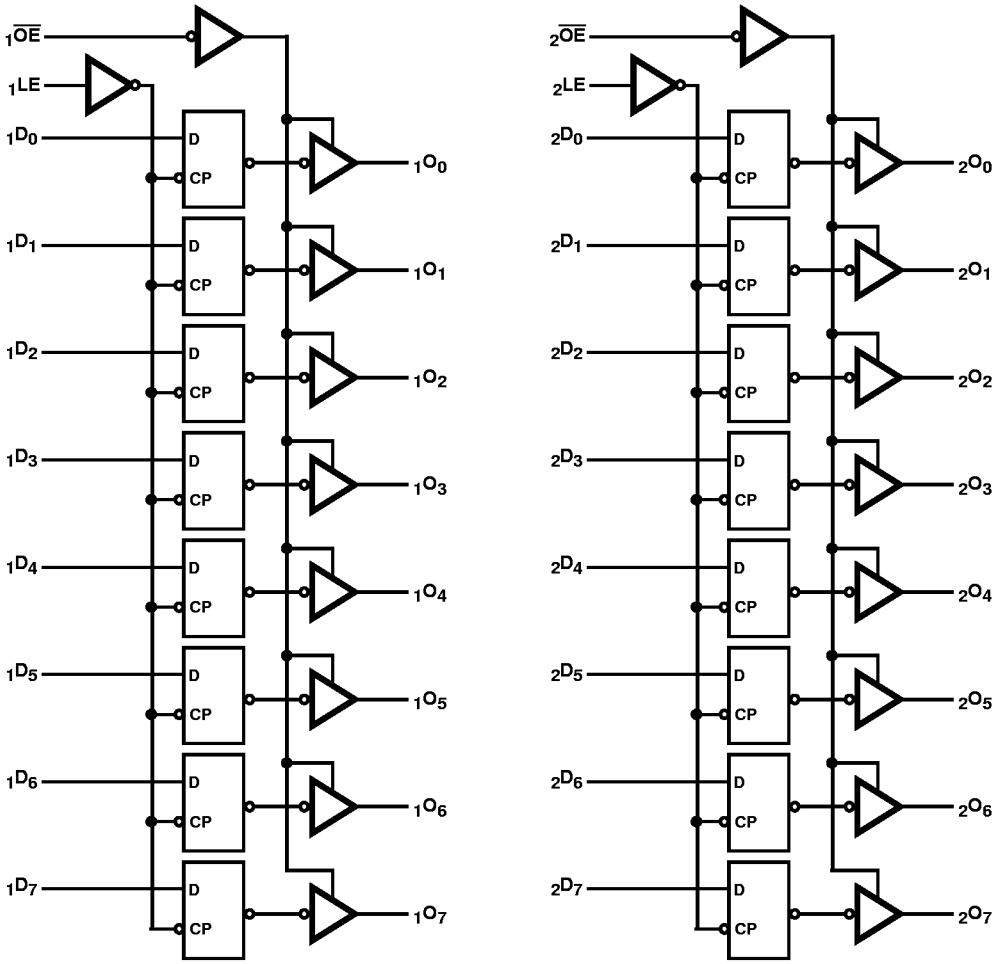
File Number **4182.3**

Pinout

CD74FCT16373T, CD74FCT162373T, CD74FCT162H373T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_XD_X$	$_X\overline{OE}$	$_XLE$	$_XO_X$
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE:
1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$	Output Enable Inputs (Active LOW)
$_XLE$	Latch Enable Inputs (Active HIGH)
$_XD_X$	Inputs (Note 2)
$_XO_X$	Three-State Outputs
GND	Ground
V_{CC}	Power

NOTE:
2. For the CD74FCT162H373T, these pins have “Bus Hold”. All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} ($^oC/W$)
TSSOP Package 94
SSOP Package 76
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16373T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
CD74FCT162373T, CD74FCT162H373T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $_X\overline{OE}$ = GND, $_X$LE = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $_X\overline{OE}$ = GND, $_X$LE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $_X\overline{OE}$ = GND, $_X$LE = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 13)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	
CD74FCT16373T, CD74FCT162373T, CD74FCT162H373T													
Propagation Delay $_XD_X$ to $_XO_X$	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
Propagation Delay $_X$LE to $_XO_X$	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	3.7	ns
Output Enable Time $_X\overline{OE}$ to $_XO_X$	t_{PZH}, t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 17) $_X\overline{OE}$ to $_XO_X$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
Setup Time HIGH or LOW, $_XD_X$ to $_X$LE	t_{SU}		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns

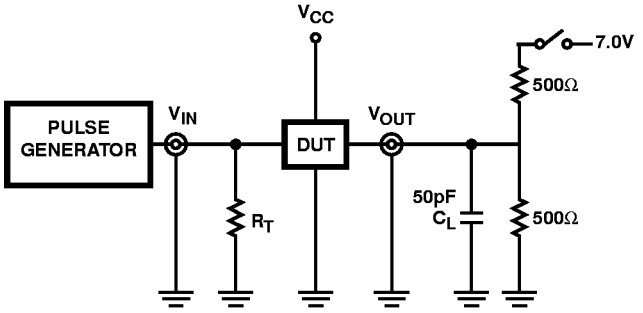
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	
Hold Time HIGH or LOW, $_XD_X$ to $_X$LE	t_H	C_L = 50 pF, R_L = 500Ω	1.5	-	1.5	-	1.5	-	1.0	-	1.0	-	ns
$_X$LE Pulse Width HIGH (Note 17)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 18)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. The test limit for this parameter is ±5μA at T_A = -55°C.
8. Pins with Bus Hold are identified in the pin description.
9. This specification does not apply to bidirectional functionalities with Bus Hold.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

19. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

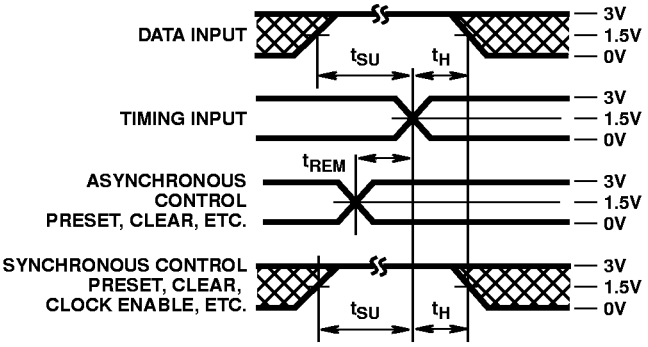


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

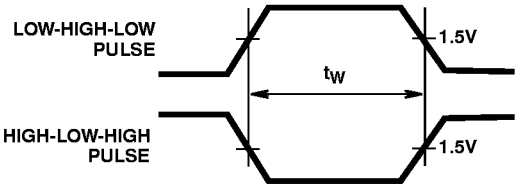


FIGURE 3. PULSE WIDTH

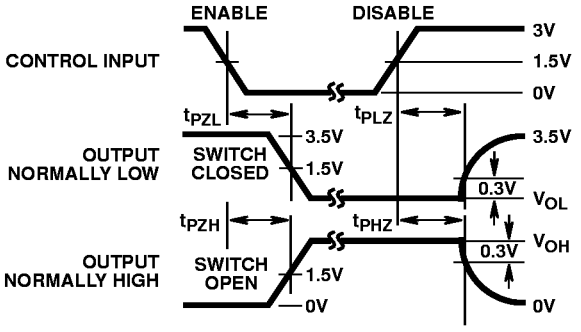


FIGURE 4. ENABLE AND DISABLE TIMING

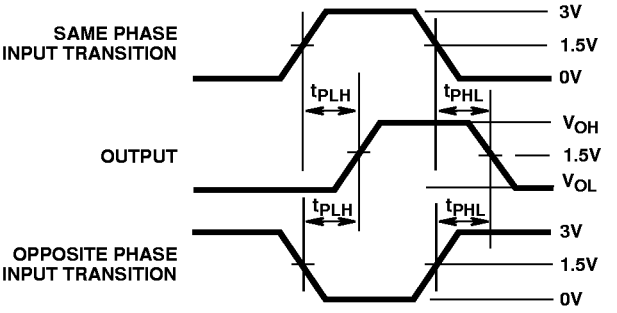


FIGURE 5. PROPAGATION DELAY