CMOS SRAM
1M-BIT(128K X 8) N341024

■ Features

- CMOS SRAM organized as 131,072 X 8bits
- Single+5.0v(± 10%)Power Supply
- High Speed Access time : 15/17/20/25ns
- Low power operation

  N341024 (Standard type)

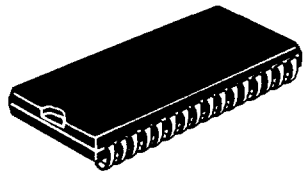
  Active : 185mA (max.)

  Standby : 55mA (max.)

  N341024-L (Low Power type)

  Active : 165mA (max.)

  Standby : 50mA (max.)



32pin Plastic SOJ(300mil/ 400mil)

●Packages

-32pin Plastic SOJ(300mil)

-32pin Plastic SOJ(400mil)

(Corner Pin type)

■ Description

The N341024 is a high performance CMOS static RAM organized as 131,072 X 8bits.

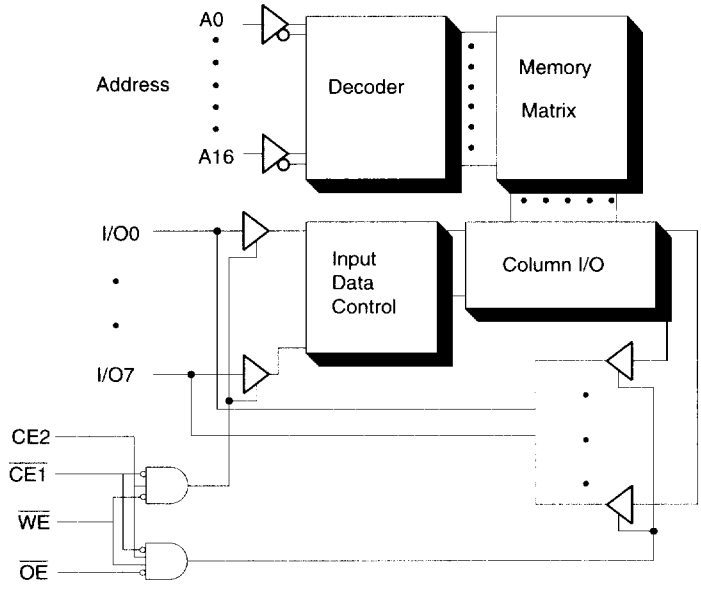
Writing to this device is accomplished when the $\overline{WE}$ and the chip enable ($\overline{CE1}$) inputs are both Low and CE2 is high .

Reading is accomplished when $\overline{WE}$ and CE2 is High and $\overline{CE1}$ and the $\overline{OE}$ are both Low .

The N341024 operates from a single +5.0V power supply and all inputs and outputs are fully TTL compatible.

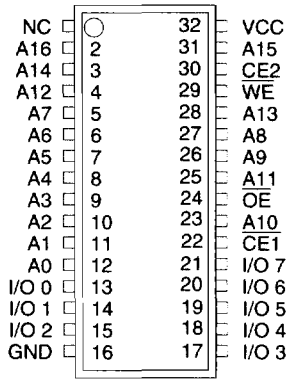
5

■ Functional Block Diagram



■ Pin Configuration

32 pin Plastic SOJ
Corner Pin Type



■ Pin Description

SYMBOL	PIN NAME
A0-A16	Address input
I/O0-I/O7	Data input/output
$\overline{CE1}$	Chip Enable input
CE2	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input
VCC	PowerSupply Pin(+5V)
GND	Ground Pin

■ Mode Selection Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE1}$	CE2	I/O	MODE
X	X	High	X	High impedance	Standby
X	X	X	Low	High impedance	Standby
Low	High	Low	High	Data out	Read
X	Low	Low	High	Data in	Write
High	High	Low	High	High impedance	Output disable

Note : X = don't care.

■ Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	-55 to 125	°C
TSTG	Storage Temperature	-55 to 125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTICE
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Recommended Operating Conditions

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	VCC
0°C to 70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	VCC + 0.5V	V
VIL	Input Low Voltage	-0.5	-	0.8	V

Note : VIL(min) = -3.0V for pulse width less than 20ns.

■ Capacitance

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

5

■ DC Electrical Characteristics

(Vcc=5.0V ± 10%, TA = 0 to +70°C, VLC ≤ 0.2V, VHC ≥ VCC - 0.2V)

Symbol	Parameter	Power	N341024 -15	N341024 -17	N341024 -20	N341024 -25	Unit
ICC	Dynamic Operating Current	Standard type	185	165	155	145	mA
	$\overline{CE1}$ ≤ VIL and CE2 ≥ VIH, VCC = max, f = fmax,	Low Power type	165	155	140	135	mA
	IOUT = 0mA, VIN ≥ VIH or ≤ VIL						
ISB	Standby Power Supply Current (TTL level)	Standard type	55	50	45	40	mA
	$\overline{CE1}$ ≥ VIH and/or CE2 ≤ VIL, VCC = max,	Low Power type	50	45	40	35	mA
	f = fmax, VIN ≥ VIH or ≤ VIL						
ISB1	Full Standby Power Supply Current (CMOS level)	Standard type	10	10	10	10	mA
	$\overline{CE1}$ ≥ VHC and/or CE2 ≤ VLC, VCC = max,	Low Power type	5	5	5	5	mA
	f = 0, VIN ≥ VHC or ≤ VLC						

DC Electrical Characteristics(1)

(Vcc=5.0V ± 10%)

Symbol	Parameter	Test condition	Standard type		Low Power type		Unit
			Min.	Max.	Min.	Max.	
ILI	Input Leakage current	VCC = max, VIN = GND to VCC	-5	5	-2	2	µA
ILO	Output Leakage Current	VCC = max, $\overline{CE1}$ ≥VIH and/or CE2 ≤ VIL,	-5	5	-2	2	µA
		VOUT = GND to VCC					
VOL	Output low voltage	IOL =8mA, VCC = min	-	0.4	-	0.4	V
		IOL =10mA, VCC = min	-	0.5	-	0.5	V
VOH	Output high voltage	IOH =-4mA, VCC = min	2.4	-	2.4	-	V

■ AC Test Conditions

Input pulse levels	GND to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See figure 1 and 2

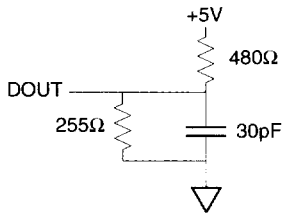


Figure 1. Output Load Equivalent

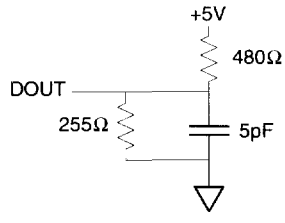


Figure 2. Output Load Equivalent
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE, tHZOE)

■ AC Electrical Characteristics

(Vcc = 5.0V ± 10%, TA=0°C to 70°C)

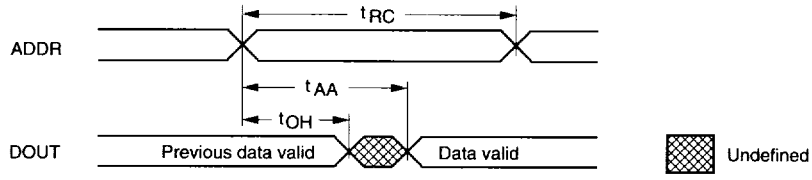
Description	Symbol	N341024-15		N341024-17		N341024-20		N341024-25		Unit
Read Cycle		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle time	t_{RC}	15		17		20		25		ns
Address access time	t_{AA}		15		17		20		25	ns
Chip enable access time	t_{ACE}		15		17		20		25	ns
Output hold from address change	t_{OH}	3		3		3		3		ns
Chip enable to output in low-Z	t_{LZCE}	5		5		5		5		ns
Chip disable to output in high-Z	t_{HZCE}		7		7		8		10	ns
Chip enable to power up time	t_{PU}	0		0		0		0		ns
Chip disable to power down time	t_{PD}		15		17		20		25	ns
Output enable access time	t_{AOE}		6		6		6		8	ns
Output enable to output in low-Z	t_{LZOE}	0		0		0		0		ns
Output disable to output in high-Z	t_{HZOE}		6		6		6		8	ns

(Vcc = 5.0V ± 10%, TA=0°C to 70°C)

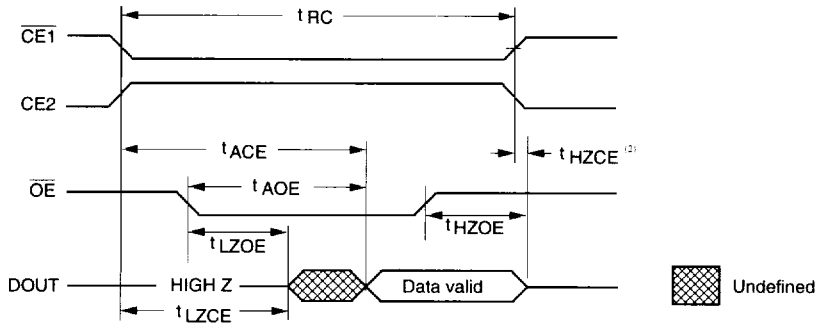
Description	Symbol	N341024-15		N341024-17		N341024-20		N341024-25		Unit
Write Cycle		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle time	t_{WC}	15		17		20		25		ns
Chip enable to end of write	t_{CW}	11		12		13		15		ns
Address valid to end of write	t_{AW}	11		12		13		15		ns
Address set-up time	t_{AS}	0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		ns
Write pulse width ($\overline{OE} \geq VIH$)	t_{WP1}	11		12		13		15		ns
Write pulse width ($\overline{OE} \leq VIL$)	t_{WP2}	12		13		14		15		ns
Data set-up time	t_{DS}	7		8		8		10		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write disable to output in low-Z	t_{LZWE}	0		0		0		0		ns
Write enable to output in high-Z	t_{HZWE}		7		7		8		10	ns

■ AC Timing Waveforms

Read Cycle No.1 [1]

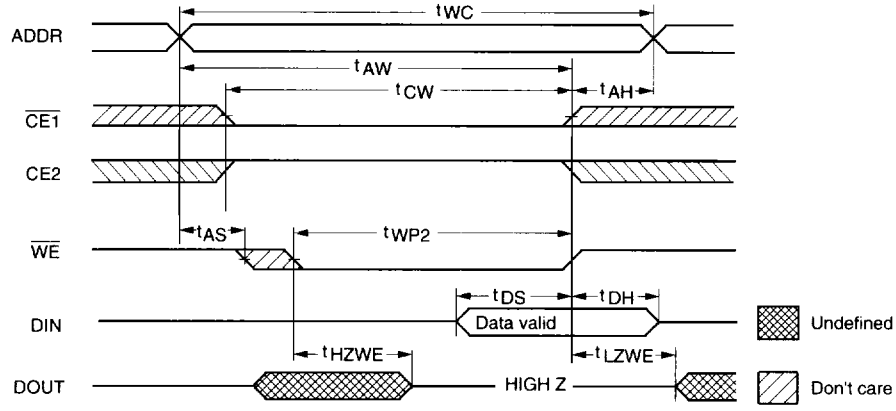


Read Cycle No.2 [1]

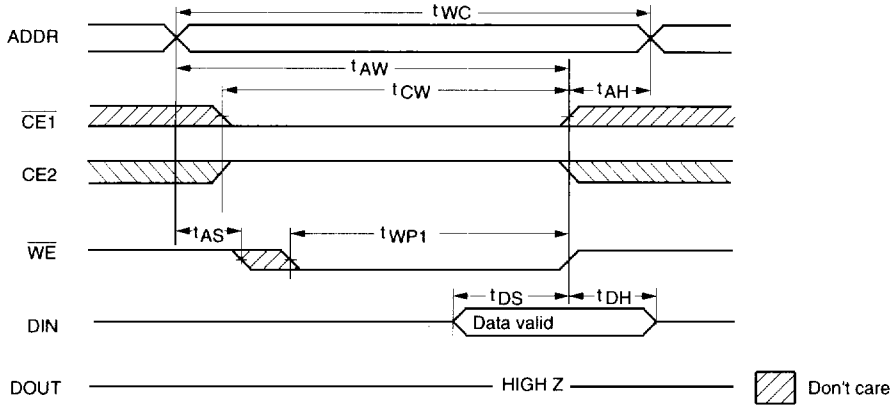


Note : (1) $\overline{WE}$ is High for READ cycle.
(2) At any given temperature and voltage condition, tHZCE is less than tLZCE.

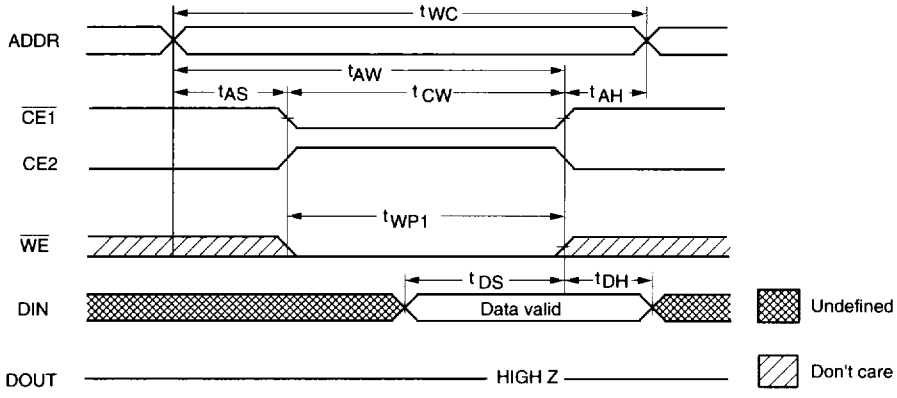
Write Cycle No.1(Write Enable Controlled)



Write Cycle No.2(Write Enable Controlled) [3]



Write Cycle No.3(Chip Enable Controlled)[2]

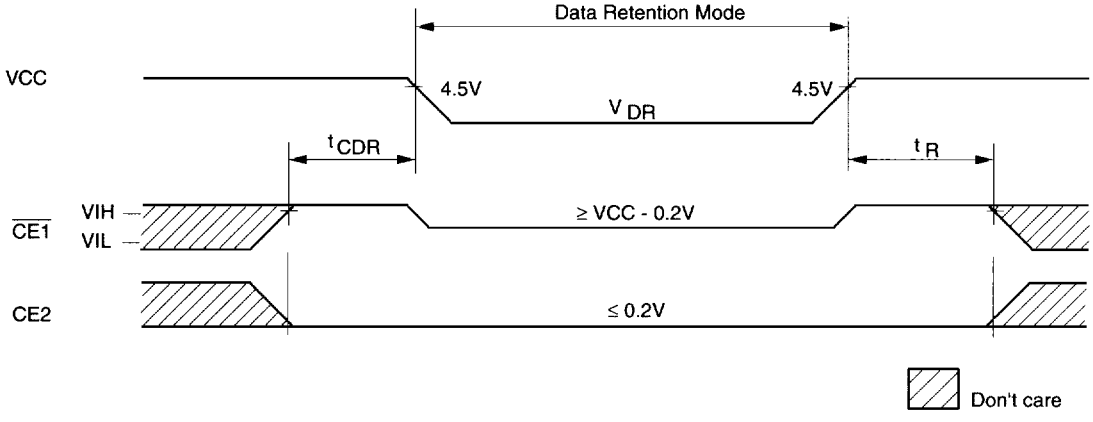


Note : (3) $\overline{OE}$ = High.

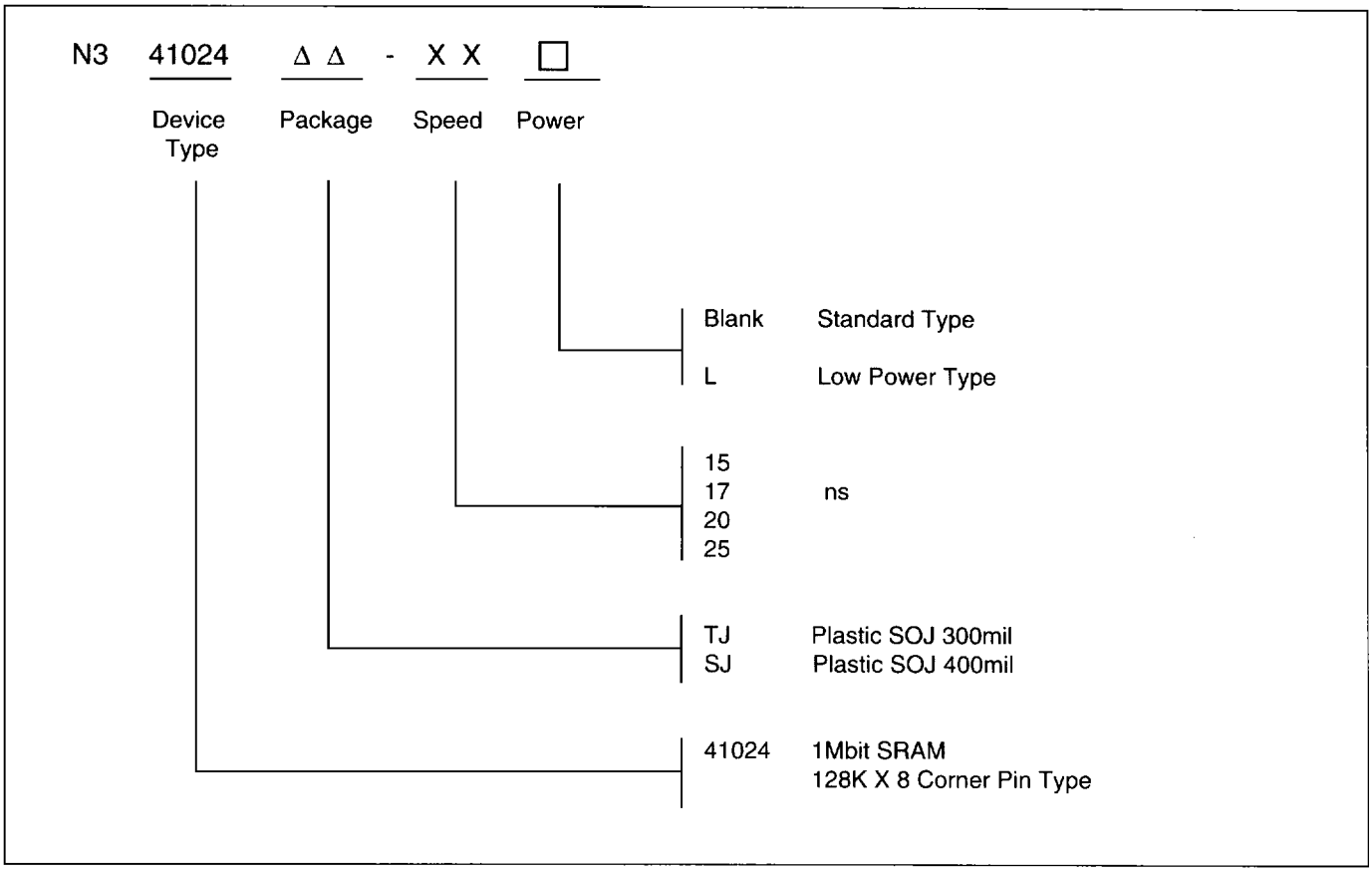
■ Data Retention Electrical Characteristics (Low Power type only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDR	VCC for Retention data			2	-	-	V
ICCDR	Data retention current	$\overline{CE1}$ ≥ VCC - 0.2V and/or CE2 ≤ 0.2V	VCC = 2V	-	-	500	µA
		VIN ≥ VCC - 0.2V or ≤ 0.2V	VCC = 3V	-	-	750	µA
tCDR	Chip deselect to data retention time			0	-	-	ns
tR	Operation recovery time			tRC	-	-	ns

Low VCC Data Retention Waveform



■ Ordering Information



PART NO.	Access Time (ns)	Operating Current (mA)	Power down Standby Current (mA)	Package
N341024TJ-15	15	185	55	32Pin Plastic SOJ (300mil)
N341024SJ-15	15	185	55	32Pin Plastic SOJ (400mil)
N341024TJ-17	17	165	50	32Pin Plastic SOJ (300mil)
N341024SJ-17	17	165	50	32Pin Plastic SOJ (400mil)
N341024TJ-20	20	155	45	32Pin Plastic SOJ (300mil)
N341024SJ-20	20	155	45	32Pin Plastic SOJ (400mil)
N341024TJ-25	25	145	40	32Pin Plastic SOJ (300mil)
N341024SJ-25	25	145	40	32Pin Plastic SOJ (400mil)
N341024TJ-15L	15	165	50	32Pin Plastic SOJ (300mil)
N341024SJ-15L	15	165	50	32Pin Plastic SOJ (400mil)
N341024TJ-17L	17	155	45	32Pin Plastic SOJ (300mil)
N341024SJ-17L	17	155	45	32Pin Plastic SOJ (400mil)
N341024TJ-20L	20	140	40	32Pin Plastic SOJ (300mil)
N341024SJ-20L	20	140	40	32Pin Plastic SOJ (400mil)
N341024TJ-25L	25	135	35	32Pin Plastic SOJ (300mil)
N341024SJ-25L	25	135	35	32Pin Plastic SOJ (400mil)