

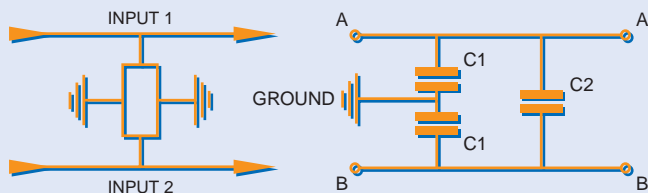
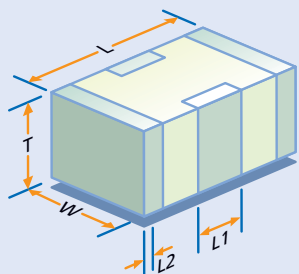
# Integrated Passive Components

## Balanced Line EMI Chip

**X2Y**

The Syfer Balanced Line Chip is a 3 terminal EMI chip device. The revolutionary design provides simultaneous line-to-line and line-to-ground filtering, using a single ceramic chip. In this way, differential and common mode filtering are provided in one device. Capable of replacing 2 or more conventional devices, it is ideal for balanced lines, twisted pairs and dc motors, in automotive, audio, sensor and other applications.

These filters can prove invaluable in meeting stringent EMC demands particularly in automotive applications.



### Specifications

<b>Dielectric</b>	X7R or COG/NP0
<b>Electrical Configuration</b>	Multiple capacitance
<b>Capacitance Measurement</b>	At 1000hr point
<b>Typical Capacitance Matching</b>	Better than 5%
<b>Temperature Rating</b>	-55°C to 125°C
<b>Dielectric Withstand Voltage</b>	2.5 x Rated Volts for 5 secs. Charging current limited to 50mA Max. 100Gohms or 1000s (whichever is the less)
<b>Insulation Resistance</b>	
<b>Termination Material</b>	100% matte tin over nickel

### Advantages

- Replaces 2 or 3 capacitors with one device
- Matched capacitance line to ground on both lines
- Low inductance due to cancellation effect
- Capacitance line to line
- Differential and common mode attenuation
- Effects of temperature and voltage variation eliminated
- Effect of ageing equal on both lines
- High current capability

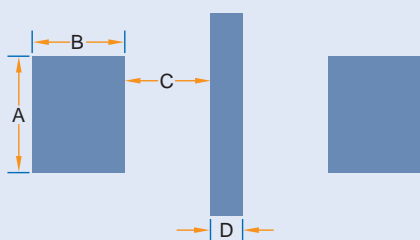
### Applications

- Balanced lines
- Twisted pairs
- EMI Suppression on DC motors
- Sensor/transducer applications
- Wireless communications
- Audio

### Chip Size

Chip Size	L	W	T	L1	L2
0603*	1.6±0.2 (0.063±0.008)	0.8±0.2 (0.03±0.008)	0.5±0.15 (0.02±0.006)	0.3±0.2 (0.012±0.008)	0.2±0.1 (0.008±0.004)
0805	2.0±0.3 (0.08±0.012)	1.25±0.2 (0.05±0.008)	1.0±0.15 (0.04±0.006)	0.5±0.25 (0.02±0.01)	0.3±0.15 (0.012±0.006)
1206	3.2±0.3 (0.126±0.012)	1.60±0.2 (0.063±0.008)	1.1±0.2 (0.043±0.008)	0.95±0.3 (0.037±0.012)	0.5±0.25 (0.02±0.01)
1410	3.6±0.3 (0.14±0.012)	2.5±0.3 (0.1±0.012)	2 max. (0.08 max.)	1.20±0.3 (0.047±0.012)	0.5±0.25 (0.02±0.01)
1812	4.5±0.35 (0.18±0.014)	3.2±0.3 (0.126±0.012)	2 max. (0.08 max.)	1.5±0.35 (0.06±0.014)	0.5±0.25 (0.02±0.01)
2220	5.7±0.4 (0.22±0.016)	5.0±0.4 (0.2±0.016)	2.5 max. (0.1 max.)	2.25±0.4 (0.09±0.016)	0.75±0.25 (0.03±0.01)

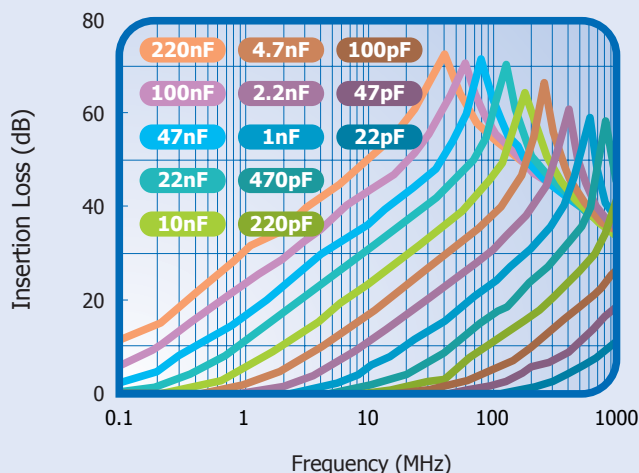
### Recommended Solder Lands



Chip Size	Dimensions mm (inches)			
	A	B	C	D
0603*	0.6 (0.024)	0.6 (0.024)	0.4 (0.016)	0.2 (0.008)
0805	0.95 (0.037)	0.9 (0.035)	0.3 (0.012)	0.4 (0.016)
1206	1.2 (0.047)	0.9 (0.035)	0.6 (0.024)	0.8 (0.03)
1410	2.05 (0.08)	1.0 (0.04)	0.7 (0.028)	0.9 (0.035)
1812	2.65 (0.104)	1.4 (0.055)	0.8 (0.03)	1.4 (0.055)
2220	4.15 (0.163)	1.4 (0.055)	1.2 (0.047)	1.8 (0.071)

### Insertion Loss Characteristics (common mode)

Typical 50 ohm system



notes

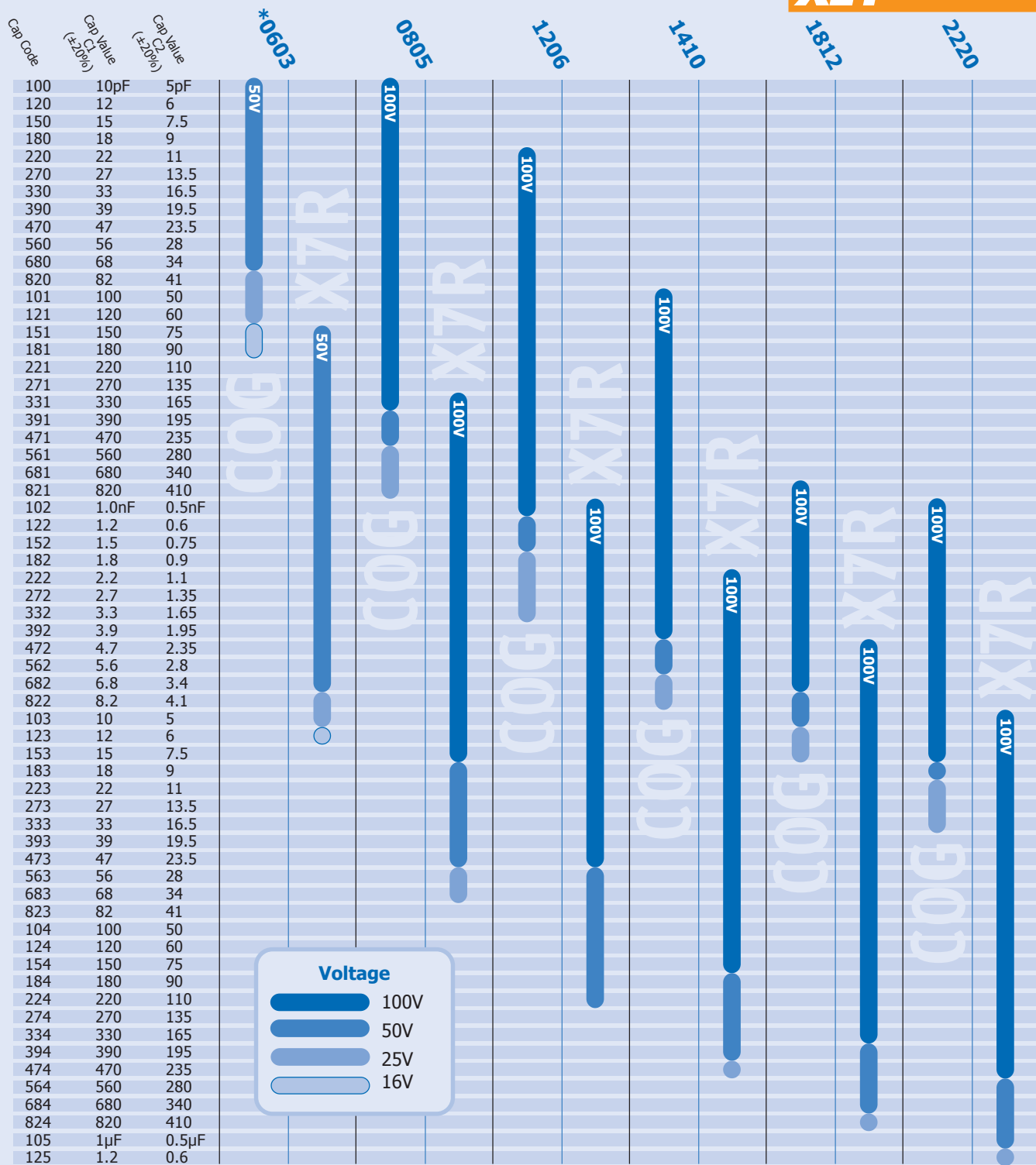
\* The 0603 chip size is a development item. All technical information should be considered provisional and subject to change. Refer to Sales office.

www.syfer.com

# Integrated Passive Components

## Balanced Line EMI Chip

**X2Y**



**Voltage**

- 100V
- 50V
- 25V
- 16V

Reeled Quantity	178mm (7")	330mm (13")	*0603	0805	1206	1410	1812	2220
Quantity	178mm (7")	330mm (13")	4000	3000	2500	2000	1000	1000
			16000	12000	10000	8000	4000	4000

**notes**

\* The 0603 chip size is a development item. All technical information should be considered provisional and subject to change. Refer to Sales office.



# Integrated Passive Components

## Balanced Line EMI Chip

**X2Y**

The Syfer Balanced Line EMI chip has a unique internal architecture which provides unbeatable EMC performance for dual line data transmission.

A typical application for dual line data transmission would see a board layout using decoupling chip capacitors or 3 terminal feedthrough chips as shown in Fig 1.

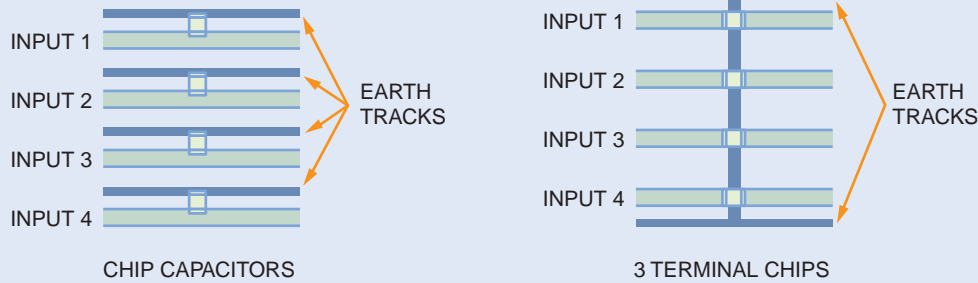


Fig 1

The Balanced Line EMI chip replaces decoupling capacitors or 3 terminal feedthrough chips on a 1 for 2 basis and provides line to line (differential mode) decoupling. Fig 2.

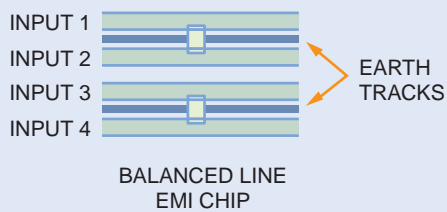


Fig 2

The internal structure furnishes a reduced inductance when compared to that of a conventional capacitor. This is a result of the novel internal electrode structure which inherently reduces the inductance by the cancellation effect of opposing currents in close proximity.

The capacitance line to ground (common mode) is closely matched due to the symmetry within the design. As the device includes line to ground capacitance for both lines, any temperature, ageing and voltage effects will have an equal influence on both lines therefore maintaining balanced decoupling.

The construction also allows a capacitance between lines as well as to ground as shown in Fig 3.

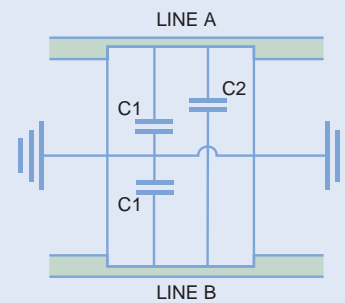


Fig 3

C2, the line to line capacitance, is half the line to ground capacitance thus providing coupling of high frequency interference between balanced lines.

Because the part acts as a decoupling device, the current limitations of a standard 3 terminal chip do not apply. The single line 3 terminal feedthrough chip carries the signal current through the very thin feedthrough electrodes within the device which have limited DC resistance and so can cause excessive heating, hence the maximum permissible current is often limited to around 300 mA for a 1206 device. The dual line 3 terminal chip is in by-pass across two lines and so is unaffected by high signal currents.

Table 1 offers a comparison of decoupling devices and demonstrates how the Balanced Line EMI chip extends the options for EMC circuit protection.

Component	Advantages	Disadvantages	Applications
Chip capacitor	<ul style="list-style-type: none"> <li>Industry standard</li> </ul>	<ul style="list-style-type: none"> <li>Requires 1 per line</li> <li>High inductance</li> <li>Capacitance matching problems</li> </ul>	<ul style="list-style-type: none"> <li>By-pass</li> <li>Low frequency</li> </ul>
3 terminal feedthrough	<ul style="list-style-type: none"> <li>Feedthrough</li> <li>Lower Inductance</li> </ul>	<ul style="list-style-type: none"> <li>Current limited</li> </ul>	<ul style="list-style-type: none"> <li>Feedthrough</li> <li>Unbalanced lines</li> <li>High frequency</li> </ul>
Balanced line EMI chip	<ul style="list-style-type: none"> <li>Very low inductance</li> <li>Replaces 2 (or 3) components</li> <li>Negates the effects of temperature, voltage and ageing</li> <li>Provides both common mode and differential mode attenuation</li> </ul>	<ul style="list-style-type: none"> <li>Not for unbalanced signal lines</li> </ul>	<ul style="list-style-type: none"> <li>By-pass</li> <li>Balanced lines</li> <li>High frequency</li> <li>DC electric motors</li> </ul>

Table 1

# Integrated Passive Components

## Balanced Line EMI Chip

**X2Y**

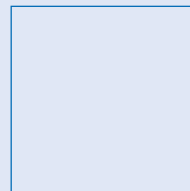
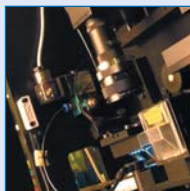
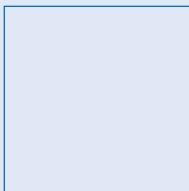
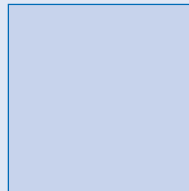
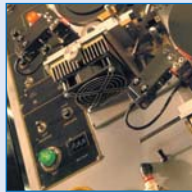
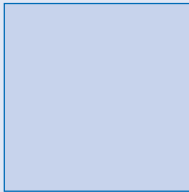
### Application Note

One of the significant features of this product is its extremely low inductance, making it particularly suitable for high speed digital applications and for reduction of common mode currents for power line applications. Inductance cancellation, due to the effect of opposing current flow across the device, results in a typical line to line inductance of around 100pH, with a corresponding line to ground inductance of 50pH.

The Balanced Line EMI chip satisfies the need for high speed communications systems using balanced lines or twisted pairs offering low inductance (therefore high frequency operation), reduced board space, reduced component count and an unparalleled performance.

### Ordering Information

1206	J	100	0222	M	X	T	E03
<b>Chip Size Reference</b>	<b>Termination</b>	<b>Voltage</b>	<b>Capacitance</b>	<b>Tolerance</b>	<b>Dielectric</b>	<b>Packaging</b>	
	J = Nickel Barrier Y = FlexiCap™	016 = 16 volts 025 = 25 volts 050 = 50 volts 100 = 100 volts	Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0222=2200pF.	M = ±20%	C = COG X = X7R	T = 178mm (7") reel R = 330mm (13") reel B = Bulk	Balanced Line EMI Chip



- Syfer Technology are able to provide comprehensive applications and design in support.
- Technical and application papers are available on request from the Sales Office.

Manufactured in the UK by Syfer Technology Limited under licence from X2Y attenuators LLC.