

8 Megabit (1Meg x 8) UV EPROM and OTP EPROM

- FAST ACCESS TIME: 90ns
- LOW POWER "CMOS" CONSUMPTION:
 - Active Current 35mA
 - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 52sec. (PRESTO IIB ALGORITHM)

DESCRIPTION

The M27C801 is an high speed 8 Megabit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 1,048,576 by 8 bits.

The Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C801 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

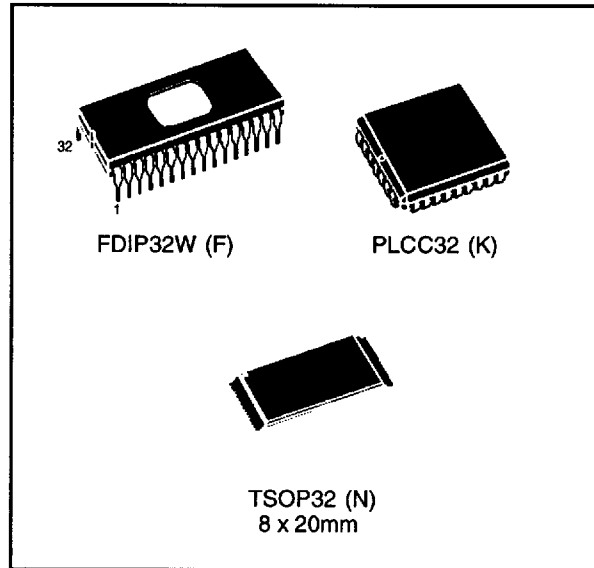


Figure 1. Logic Diagram

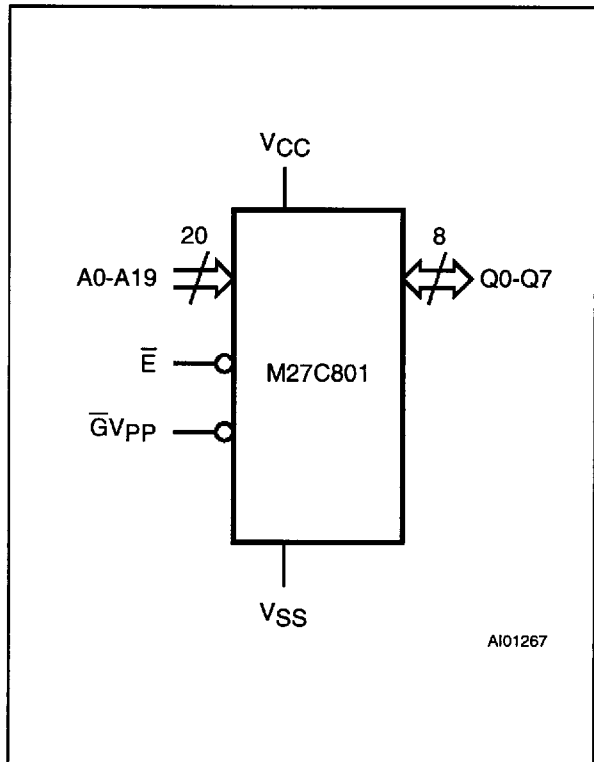


Table 1. Signal Names

| | |
|-----------------|--------------------------------|
| A0 - A19 | Address Inputs |
| Q0 - Q7 | Data Outputs |
| \bar{E} | Chip Enable |
| $\bar{G}V_{PP}$ | Output Enable / Program Supply |
| V_{CC} | Supply Voltage |
| V_{SS} | Ground |

Figure 2A. DIP Pin Connections

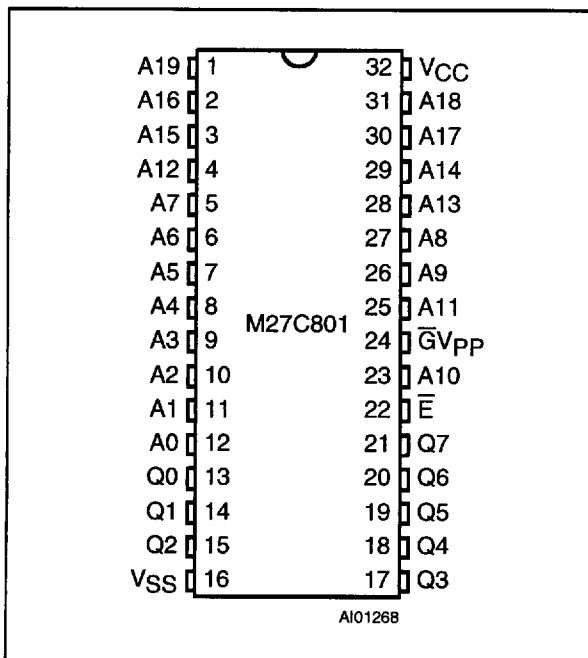


Figure 2B. PLCC Pin Connections

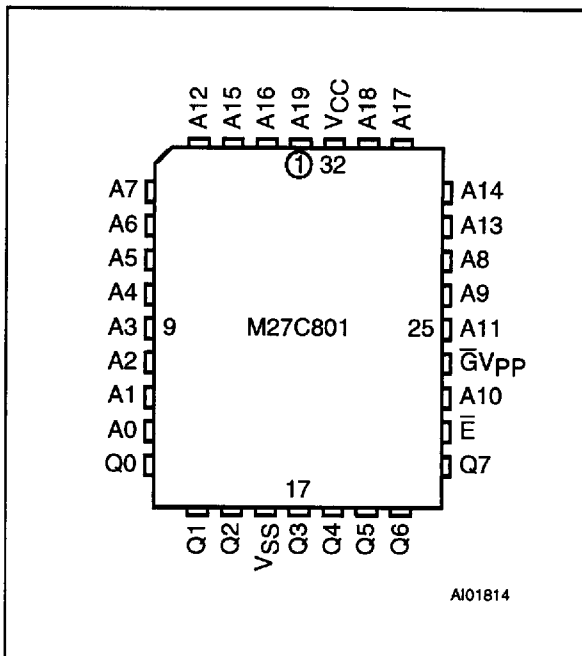
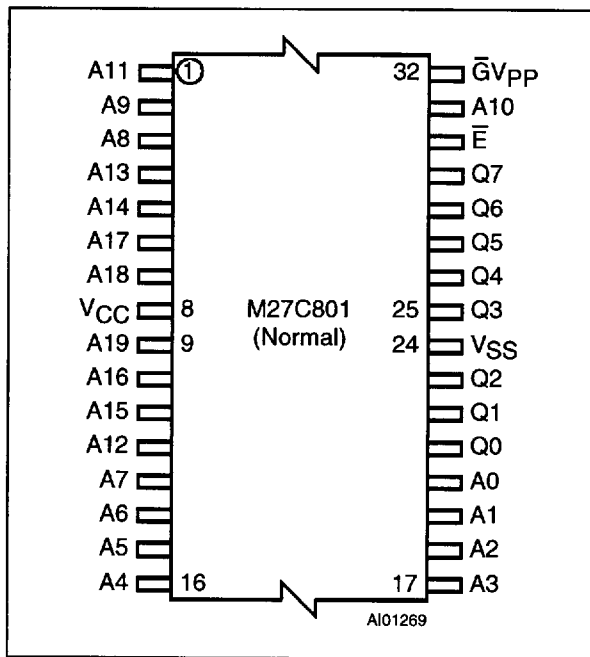


Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C801 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for GVPP and 12V on A9 for Electronic Signature and Margin Mode Set or Reset.

Read Mode

The M27C801 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\bar{E}) is the power control and should be used for device selection. Output Enable (\bar{G}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from \bar{E} to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of \bar{G} , assuming that \bar{E} has been low and the addresses have been stable for at least $t_{AVQV} - t_{GLQV}$.

Standby Mode

The M27C801 has a standby mode which reduces the active current from 35mA to 100µA. The M27C801 is placed in the standby mode by applying a CMOS high signal to the \bar{E} input. When in the standby mode, the outputs are in a high impedance state, independent of the GVPP input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- a. the lowest possible memory power dissipation,
- b. complete assurance that output bus contention will not occur.

Table 2. Absolute Maximum Ratings ⁽¹⁾

| Symbol | Parameter | Value | Unit |
|--------------------------------|--------------------------------------|------------|------|
| T _A | Ambient Operating Temperature | -40 to 125 | °C |
| T _{BIAS} | Temperature Under Bias | -50 to 125 | °C |
| T _{STG} | Storage Temperature | -65 to 150 | °C |
| V _{IO} ⁽²⁾ | Input or Output Voltages (except A9) | -2 to 7 | V |
| V _{CC} | Supply Voltage | -2 to 7 | V |
| V _{A9} ⁽²⁾ | A9 Voltage | -2 to 13.5 | V |
| V _{PP} | Program Supply Voltage | -2 to 14 | V |

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is -0.5V with possible undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

| Mode | \bar{E} | \bar{G}_{PP} | A9 | Q0 - Q7 |
|----------------------|-----------------------|-----------------|-----------------|----------|
| Read | V _{IL} | V _{IL} | X | Data Out |
| Output Disable | V _{IL} | V _{IH} | X | Hi-Z |
| Program | V _{IL} Pulse | V _{PP} | X | Data In |
| Program Inhibit | V _{IH} | V _{PP} | X | Hi-Z |
| Standby | V _{IH} | X | X | Hi-Z |
| Electronic Signature | V _{IL} | V _{IL} | V _{ID} | Codes |

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 4. Electronic Signature

| Identifier | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|---------------------|-----------------|----|----|----|----|----|----|----|----|----------|
| Manufacturer's Code | V _{IL} | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device Code | V _{IH} | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42h |

For the most efficient use of these two control lines, \bar{E} should be decoded and used as the primary device selecting function, while \bar{G} should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of \bar{E} . The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

Table 5. AC Measurement Conditions

| | High Speed | Standard |
|---------------------------------------|------------|--------------|
| Input Rise and Fall Times | ≤ 10ns | ≤ 20ns |
| Input Pulse Voltages | 0 to 3V | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V | 0.8V and 2V |

Figure 3. AC Testing Input Output Waveform

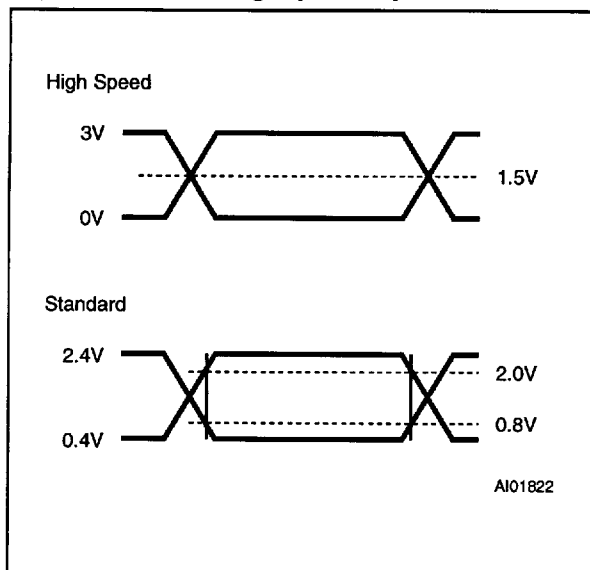


Figure 4. AC Testing Load Circuit

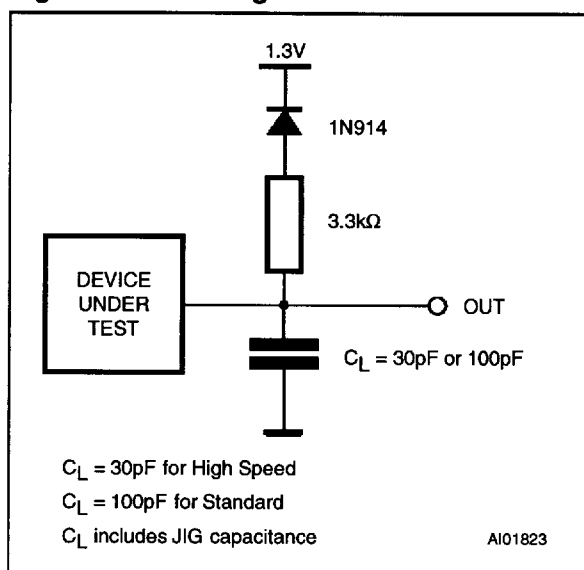


Table 6. Capacitance⁽¹⁾ (TA = 25 °C, f = 1 MHz)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|------------------|--------------------|-----------------------|-----|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | | 12 | pF |

Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode DC Characteristics ⁽¹⁾
 (T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 5V ± 10%)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|--------------------------------|-------------------------------|---|------------------------|---------------------|------|
| I _{LI} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | | ±10 | μA |
| I _{LO} | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{CC} | | ±10 | μA |
| I _{CC} | Supply Current | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL},$ I _{OUT} = 0mA, f = 5MHz | | 35 | mA |
| I _{CC1} | Supply Current (Standby) TTL | $\bar{E} = V_{IH}$ | | 1 | mA |
| I _{CC2} | Supply Current (Standby) CMOS | $\bar{E} > V_{CC} - 0.2V$ | | 100 | μA |
| I _{PP} | Program Current | V _{PP} = V _{CC} | | 10 | μA |
| V _{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| V _{IH} ⁽²⁾ | Input High Voltage | | 2 | V _{CC} + 1 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1mA | | 0.4 | V |
| V _{OH} | Output High Voltage TTL | I _{OH} = -1mA | 3.6 | | V |
| | Output High Voltage CMOS | I _{OH} = -100μA | V _{CC} - 0.7V | | V |

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
 2. Maximum DC voltage on Output is V_{CC} + 0.5V.

Table 8A. Read Mode AC Characteristics ⁽¹⁾
 (T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

| Symbol | Alt | Parameter | Test Condition | M27C801 | | | | | | Unit |
|----------------------------------|------------------|---|--|--------------------|-----|------|-----|------|-----|------|
| | | | | -90 ⁽³⁾ | | -100 | | -120 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| t _{AVQV} | t _{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL}$ | | 90 | | 100 | | 120 | ns |
| t _{ELQV} | t _{CE} | Chip Enable Low to Output Valid | $\bar{G}V_{PP} = V_{IL}$ | | 90 | | 100 | | 120 | ns |
| t _{GLQV} | t _{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 45 | | 50 | | 60 | ns |
| t _{EHQZ} ⁽²⁾ | t _{DF} | Chip Enable High to Output Hi-Z | $\bar{G}V_{PP} = V_{IL}$ | 0 | 30 | 0 | 30 | 0 | 40 | ns |
| t _{GHQZ} ⁽²⁾ | t _{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 30 | 0 | 30 | 0 | 40 | ns |
| t _{AXQX} | t _{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
 2. Sampled only, not 100% tested.
 3. In case of 90ns speed see High Speed AC measurement conditions.

M27C801

Table 8B. Read Mode AC Characteristics (1)

($T_A = 0$ to 70 °C or -40 to 85 °C; $V_{CC} = 5V \pm 10\%$; $V_{PP} = V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27C801 | | | | Unit |
|------------------|-----------|---|--|---------|-----|------|-----|------|
| | | | | -150 | | -200 | | |
| | | | | Min | Max | Min | Max | |
| t_{AVQV} | t_{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL}$ | | 150 | | 200 | ns |
| t_{ELQV} | t_{CE} | Chip Enable Low to Output Valid | $\bar{G}V_{PP} = V_{IL}$ | | 150 | | 200 | ns |
| t_{GLQV} | t_{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 60 | | 70 | ns |
| $t_{EHQZ}^{(2)}$ | t_{DF} | Chip Enable High to Output Hi-Z | $\bar{G}V_{PP} = V_{IL}$ | 0 | 50 | 0 | 50 | ns |
| $t_{GHQZ}^{(2)}$ | t_{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 50 | 0 | 50 | ns |
| t_{AXQX} | t_{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL}$ | 0 | | 0 | | ns |

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .
 2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

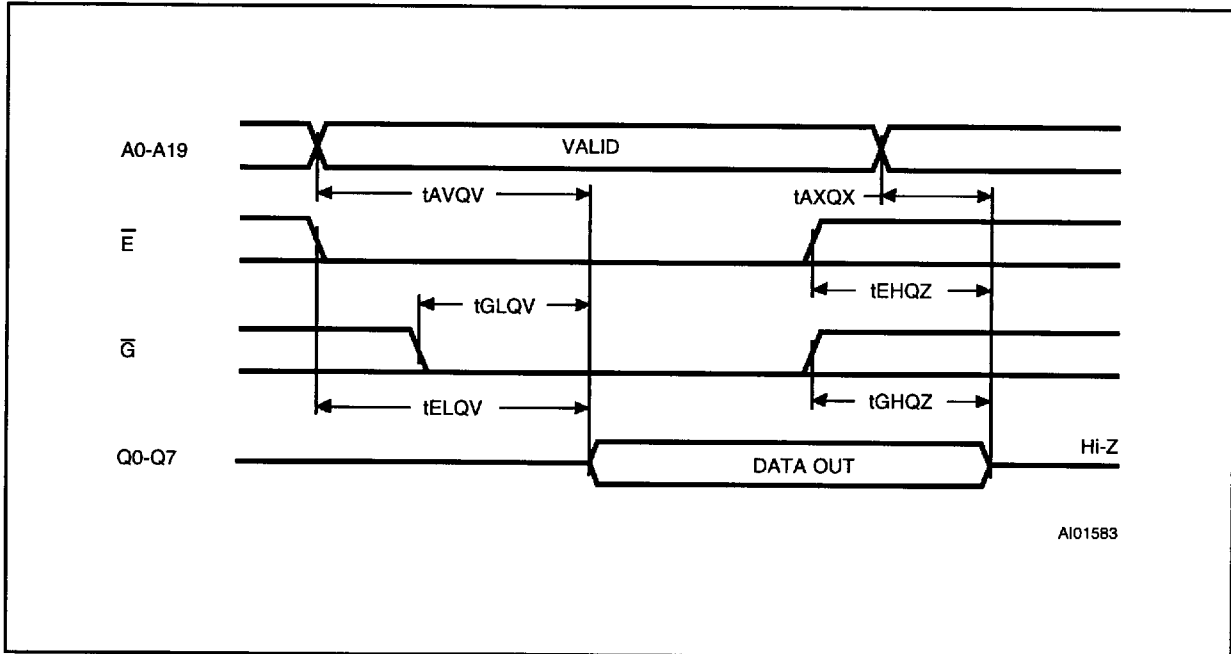


Table 9. Programming Mode DC Characteristics ⁽¹⁾
 (T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|-----------------|-------------------------|---|------|-----------------------|------|
| I _{LI} | Input Leakage Current | V _{IL} ≤ V _{IN} ≤ V _{IH} | | ±10 | μA |
| I _{CC} | Supply Current | | | 50 | mA |
| I _{PP} | Program Current | $\bar{E} = V_{IL}$ | | 50 | mA |
| V _{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2 | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1mA | | 0.4 | V |
| V _{OH} | Output High Voltage TTL | I _{OH} = -1mA | 3.6 | | V |
| V _{ID} | A9 Voltage | | 11.5 | 12.5 | V |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. MARGIN MODE AC Characteristics ⁽¹⁾
 (T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

| Symbol | Alt | Parameter | Test Condition | Min | Max | Unit |
|---------------------|-------------------|--|----------------|-----|-----|------|
| t _{A9HVPH} | t _{AS9} | VA9 High to V _{PP} High | | 2 | | μs |
| t _{VPHEL} | t _{VPS} | V _{PP} High to Chip Enable Low | | 2 | | μs |
| t _{A10HEH} | t _{AS10} | VA10 High to Chip Enable High (Set) | | 1 | | μs |
| t _{A10LEH} | t _{AS10} | VA10 Low to Chip Enable High (Reset) | | 1 | | μs |
| t _{EXA10X} | t _{AH10} | Chip Enable Transition to VA10 Transition | | 1 | | μs |
| t _{EXVPX} | t _{VPH} | Chip Enable Transition to V _{PP} Transition | | 2 | | μs |
| t _{VPA9X} | t _{AH9} | V _{PP} Transition to VA9 Transition | | 2 | | μs |

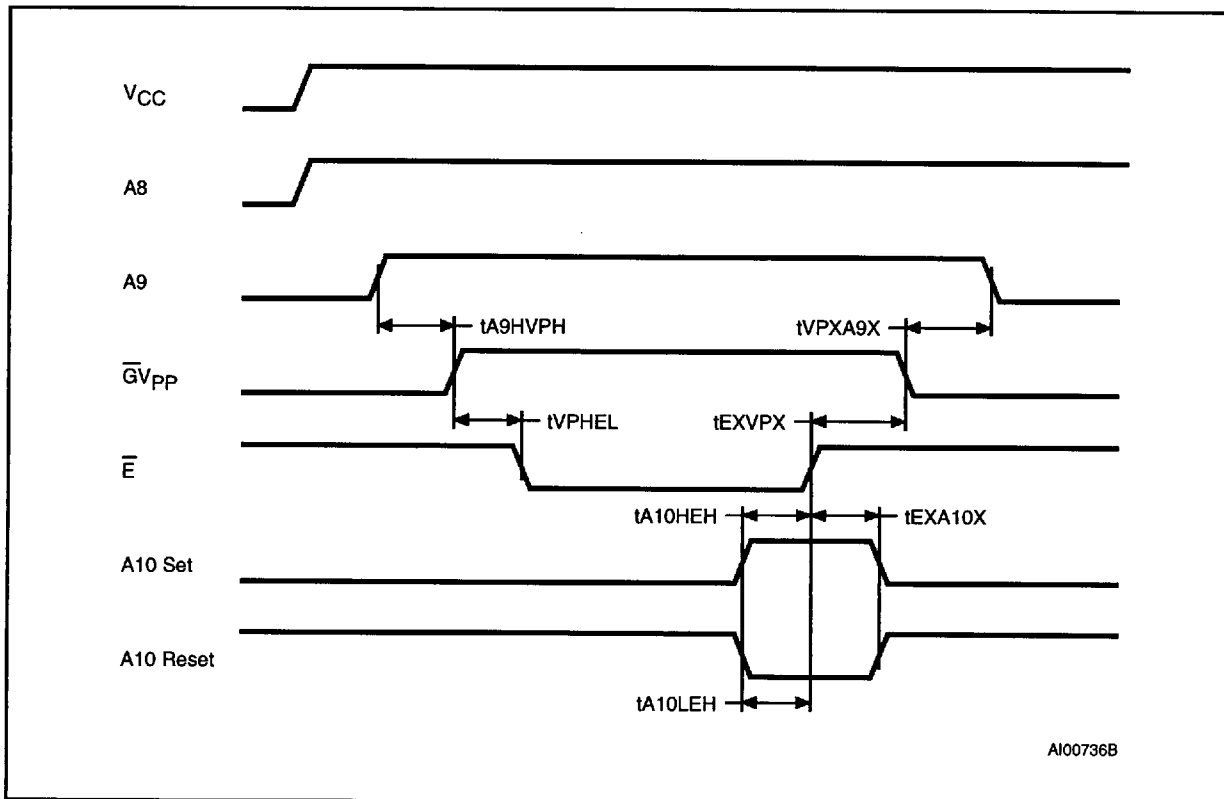
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 11. Programming Mode AC Characteristics ⁽¹⁾
 (T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

| Symbol | Alt | Parameter | Test Condition | Min | Max | Unit |
|----------------------------------|------------------|--|----------------|-----|-----|------|
| t _{AVEL} | t _{AS} | Address Valid to Chip Enable Low | | 2 | | μs |
| t _{QVEL} | t _{DS} | Input Valid to Chip Enable Low | | 2 | | μs |
| t _{VCHL} | t _{VCS} | V _{CC} High to Chip Enable Low | | 2 | | μs |
| t _{VPHEL} | t _{OES} | V _{PP} High to Chip Enable Low | | 2 | | μs |
| t _{VPLVPH} | t _{PRT} | V _{PP} Rise Time | | 50 | | ns |
| t _{LELH} | t _{PW} | Chip Enable Program Pulse Width (Initial) | | 45 | 55 | μs |
| t _{EHQX} | t _{DH} | Chip Enable High to Input Transition | | 2 | | μs |
| t _{EHVPX} | t _{OEH} | Chip Enable High to V _{PP} Transition | | 2 | | μs |
| t _{VPLEL} | t _{VR} | V _{PP} Low to Chip Enable Low | | 2 | | μs |
| t _{ELQV} | t _{DV} | Chip Enable Low to Output Valid | | | 1 | μs |
| t _{EHQZ} ⁽²⁾ | t _{DFP} | Chip Enable High to Output Hi-Z | | 0 | 130 | ns |
| t _{EHAX} | t _{AH} | Chip Enable High to Address Transition | | 0 | | ns |

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
 2. Sampled only, not 100% tested.

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

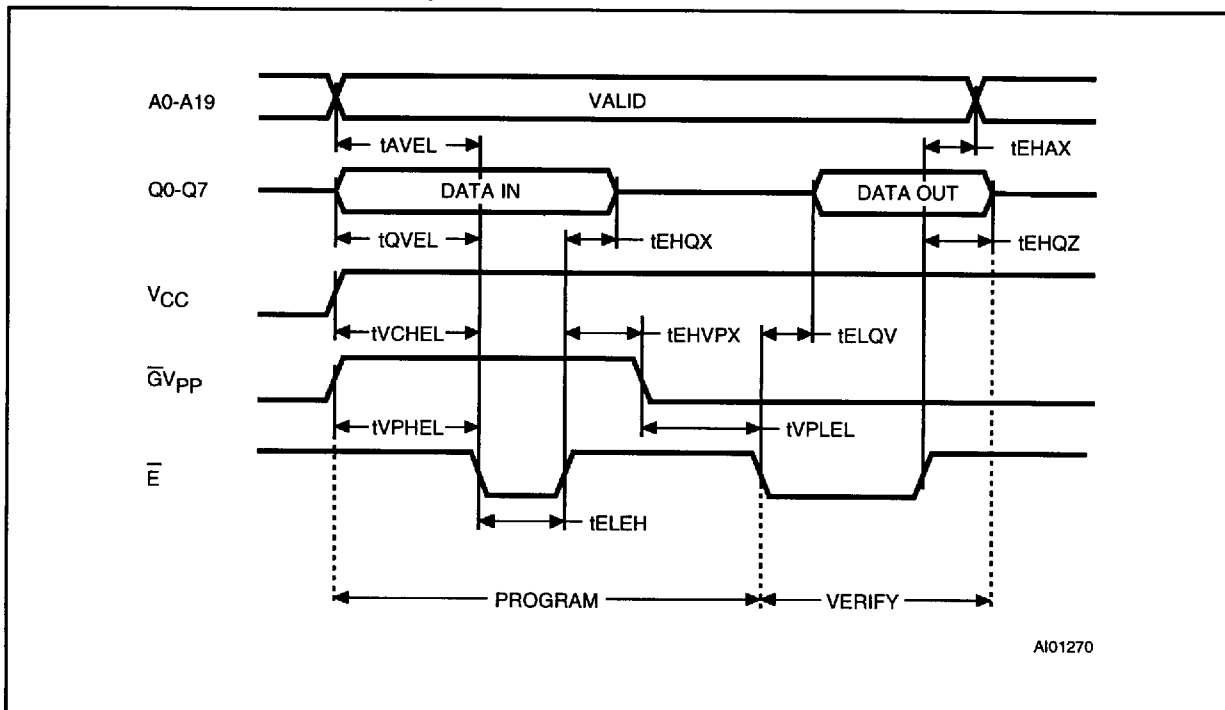
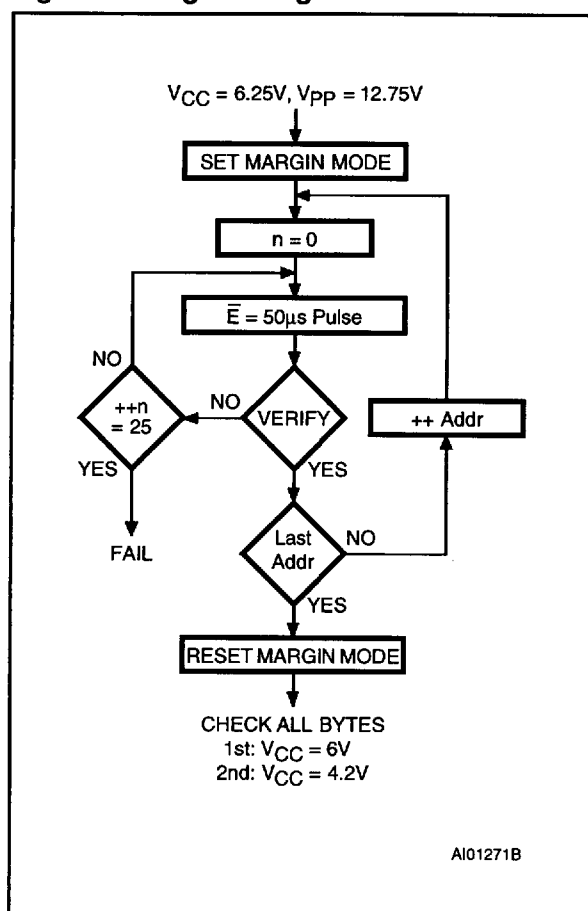


Figure 8. Programming Flowchart



DEVICE OPERATION (cont'd)

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a $0.1\mu F$ ceramic capacitor be used on every device between V_{CC} and V_{SS} . This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a $4.7\mu F$ bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C801 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only '0' will be programmed, both "1" and "0" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C801 is in the programming mode when V_{PP} input is at 12.75V and \bar{E} is pulsed to V_{IL} . The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be $6.25V \pm 0.25V$.

The M27C801 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically 52 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. This can be achieved with SGS-THOMSON M27C801 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of $50\mu s$ program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27C801s in parallel with different data is also easily accomplished. Except for \bar{E} , all like inputs including $\bar{G}V_{PP}$ of the parallel M27C801 may be common. A TTL low level pulse applied to a M27C801's \bar{E} input, with V_{PP} at 12.75V, will program that M27C801. A high level \bar{E} input inhibits the other M27C801s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with \bar{G} at V_{IL} . Data should be verified with t_{ELQV} after the falling edge of \bar{E} .

On-Board Programming

The M27C801 can be directly programmed in the application circuit. See the relevant Application Note AN620.

Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the M27C801. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C801. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during Electronic Signature mode.

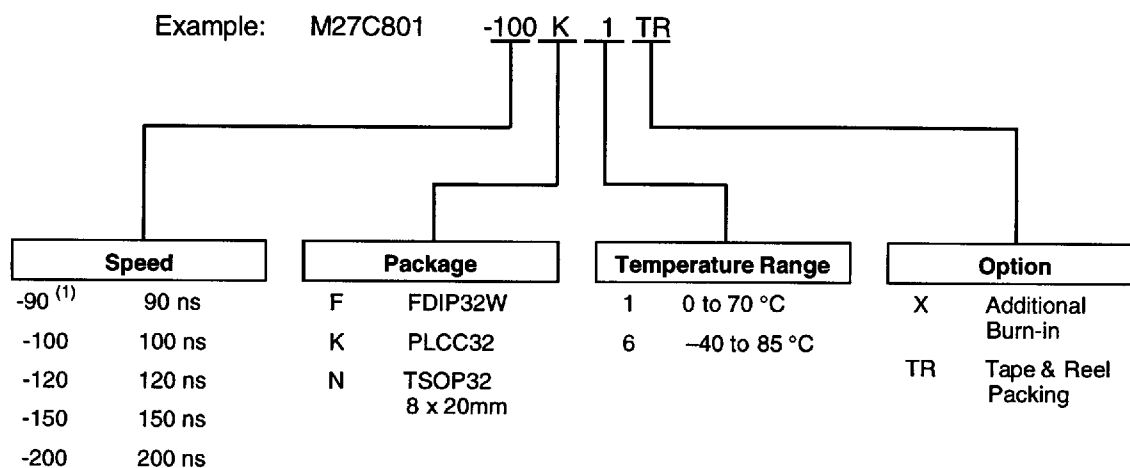
Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C801, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C801 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range.

Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C801 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C801 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C801 window to prevent unintentional erasure. The recommended erasure procedure for the M27C801 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm². The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000 µW/cm² power rating. The M27C801 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME



Note: 1. High Speed, see AC Characteristics section for further information.

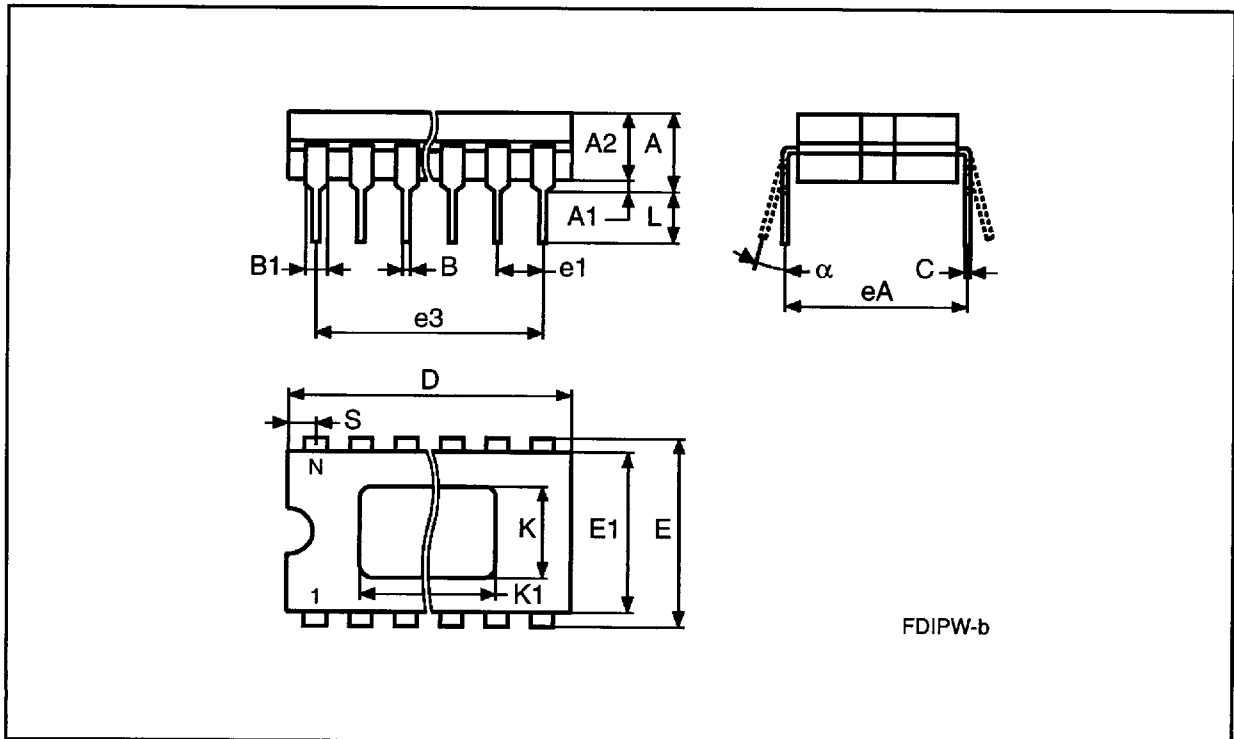
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

FDIP32W - 32 pin Ceramic Frit-seal DIP, with window

| Symb | mm | | | inches | | |
|----------|-------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 5.71 | | | 0.225 |
| A1 | | 0.50 | 1.78 | | 0.020 | 0.070 |
| A2 | | 3.90 | 5.08 | | 0.154 | 0.200 |
| B | | 0.40 | 0.55 | | 0.016 | 0.022 |
| B1 | | 1.27 | 1.52 | | 0.050 | 0.060 |
| C | | 0.22 | 0.31 | | 0.009 | 0.012 |
| D | | | 42.78 | | | 1.684 |
| E | | 15.40 | 15.80 | | 0.606 | 0.622 |
| E1 | | 14.50 | 14.90 | | 0.571 | 0.587 |
| e1 | 2.54 | - | - | 0.100 | - | - |
| e3 | 38.10 | - | - | 1.500 | - | - |
| eA | | 16.17 | 18.32 | | 0.637 | 0.721 |
| L | | 3.18 | 4.10 | | 0.125 | 0.161 |
| S | | 1.52 | 2.49 | | 0.060 | 0.098 |
| K | | 8.79 | 8.99 | | 0.346 | 0.354 |
| K1 | | 9.30 | 9.50 | | 0.366 | 0.374 |
| α | | 4° | 15° | | 4° | 15° |
| N | | 32 | | | 32 | |

FDIP32W

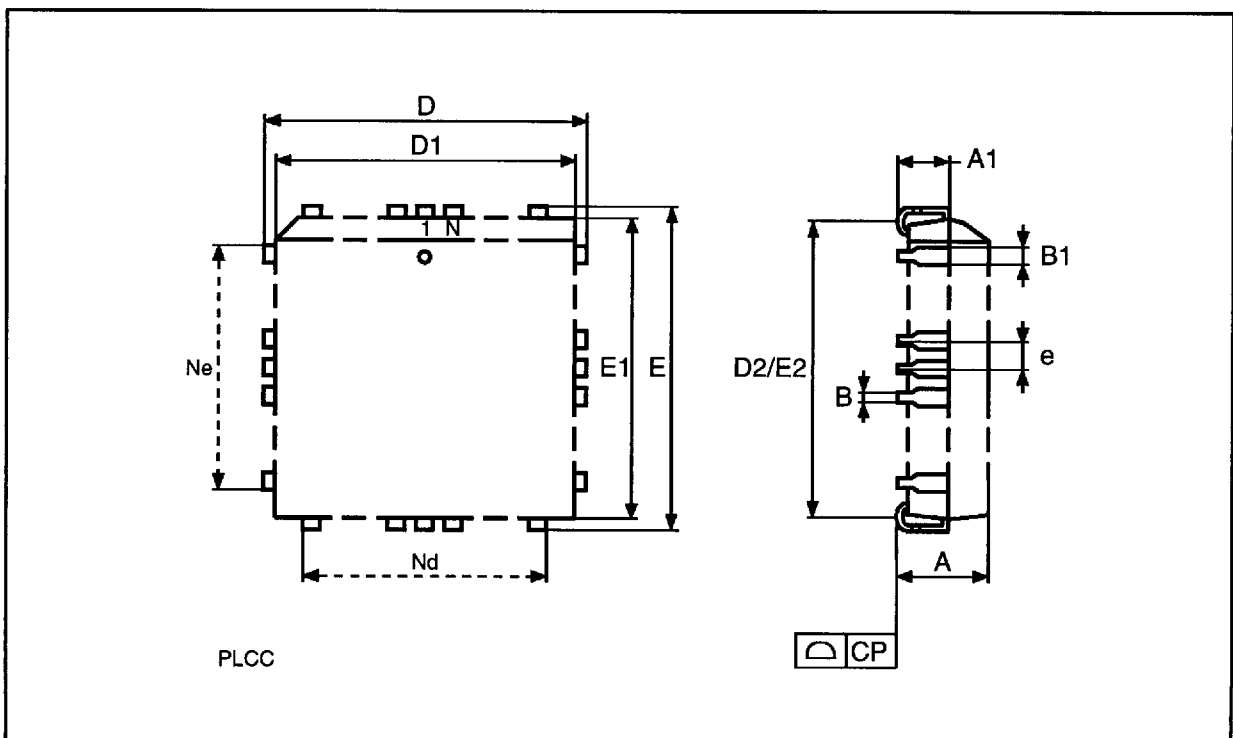


Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

| Symb | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 2.54 | 3.56 | | 0.100 | 0.140 |
| A1 | | 1.52 | 2.41 | | 0.060 | 0.095 |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| D | | 12.32 | 12.57 | | 0.485 | 0.495 |
| D1 | | 11.35 | 11.56 | | 0.447 | 0.455 |
| D2 | | 9.91 | 10.92 | | 0.390 | 0.430 |
| E | | 14.86 | 15.11 | | 0.585 | 0.595 |
| E1 | | 13.89 | 14.10 | | 0.547 | 0.555 |
| E2 | | 12.45 | 13.46 | | 0.490 | 0.530 |
| e | 1.27 | - | - | 0.050 | - | - |
| N | | 32 | | | 32 | |
| Nd | | 7 | | | 7 | |
| Ne | | 9 | | | 9 | |
| CP | | | 0.10 | | | 0.004 |

PLCC32

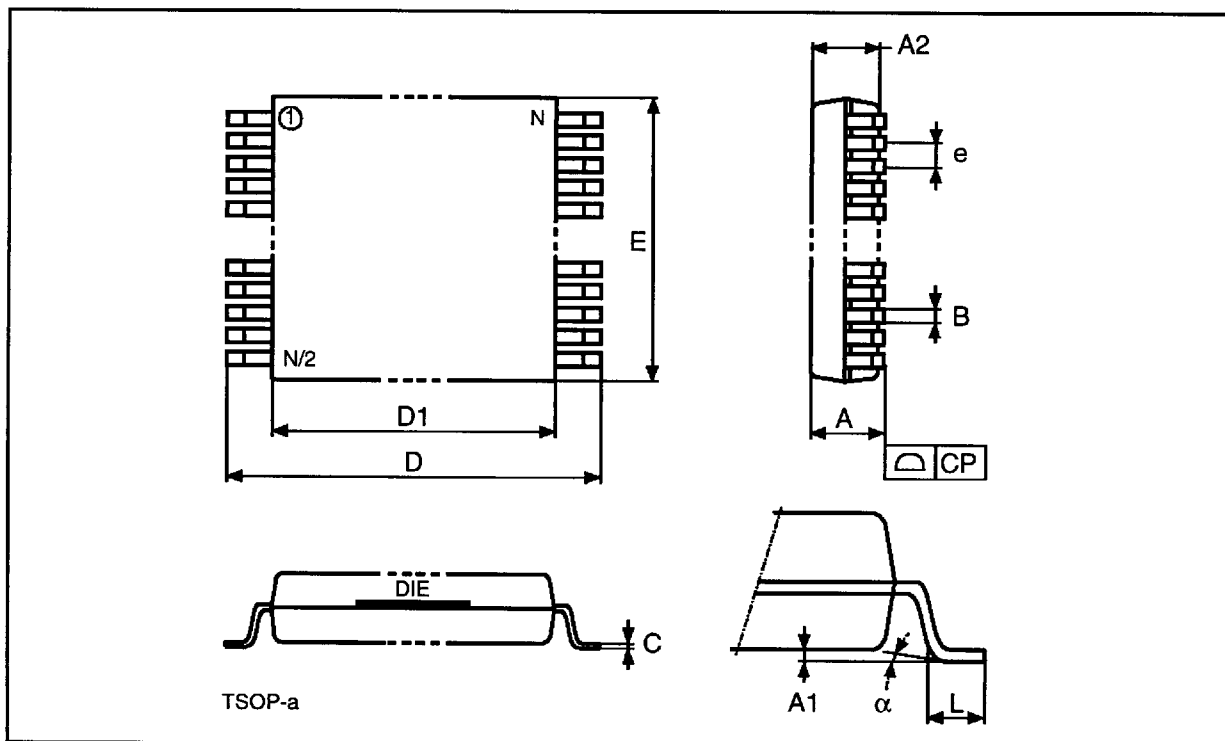


Drawing is not to scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

| Symb | mm | | | inches | | |
|----------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.05 | 0.17 | | 0.002 | 0.006 |
| A2 | | 0.95 | 1.50 | | 0.037 | 0.059 |
| B | | 0.15 | 0.27 | | 0.006 | 0.011 |
| C | | 0.10 | 0.21 | | 0.004 | 0.008 |
| D | | 19.80 | 20.20 | | 0.780 | 0.795 |
| D1 | | 18.30 | 18.50 | | 0.720 | 0.728 |
| E | | 7.90 | 8.10 | | 0.311 | 0.319 |
| e | 0.50 | - | - | 0.020 | - | - |
| L | | 0.50 | 0.70 | | 0.020 | 0.028 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |
| CP | | | 0.10 | | | 0.004 |

TSOP32



Drawing is not to scale