Winbond Electronics Corp.

256K × 8 CMOS STATIC RAM

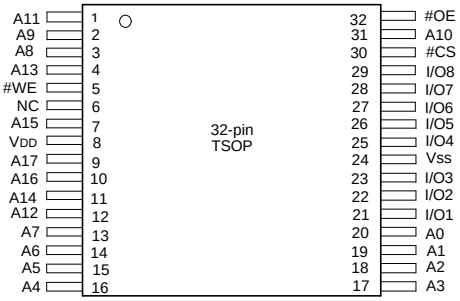
GENERAL DESCRIPTION

The W24B02 is a normal-speed, very low-power CMOS static RAM organized as 262144 x 8 bits that operates on a wide voltage range from 2.7V to 3.6V power supply. The W24B02, W24B02-LE and W24B02-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

FEATURES

- Low power consumption
- Access time: 55/70 nS
- 2.7V to 3.6V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Available packages: TFBGA and 32-pin Type one TSOP (8 x 13.4 mm and 8 x 20 mm)

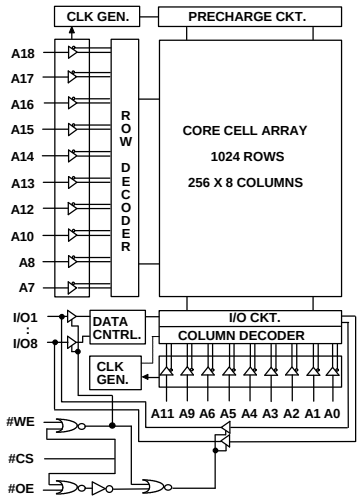
PIN CONFIGURATIONS



TFBGA TOP VIEW

	1	2	3	4	5	6
A	A0	A1	NC	A3	A6	A8
B	I/O5	A2	#WE	A4	A7	I/O1
C	I/O6		NC	A5		I/O2
D	VSS					VDD
E	VDD					VSS
F	I/O7		NC	A17		I/O3
G	I/O8	#OE	#CS	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A17	Address Inputs
I/O1 – I/O8	Data Inputs/Outputs
#CS	Chip Select Input
#WE	Write Enable Input
#OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

#CS	#OE	#WE	MODE	I/O1 - I/O8	VDD CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	2 Bytes Read	DOUT	IDD
L	L	H	Lower Byte Read	DOUT	IDD
L	L	H	Upper Byte Read	High Z	IDD
L	X	L	2 Bytes Write	DIN	IDD
L	X	L	Lower Byte Write	DIN	IDD
L	X	L	Upper Byte Write	High Z	IDD
X	X	X	Not Selected	High Z	ISB, ISB1

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to VSS Potential		-0.5 to +4.6	V
Input/Output to VSS Potential		-0.5 to VDD +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VSS = 0V; TA (°C) = -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	W24B02		UNIT
			MIN.	MAX.	
Operating Power Voltage	VDD	-	2.7	3.6	V
Input Low Voltage	VIL	-	-0.2	+0.4	V
Input High Voltage	VIH	-	+2.2	VDD +0.3	V
Input Leakage Current	ILI	VIN = VSS to VDD	-1	+1	µA
Output Leakage Current	ILO	VI/O = VSS to VDD; #CS = VIH (min.) or #OE = VIH (min.) or #WE = VIL (max.)	-1	+1	µA
Output Low Voltage	VOL	IOL = +0.1 mA	-	0.4	V

Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	W24B02		UNIT
			MIN.	MAX.	
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4	-	V
Operating Power Supply Current	I_{DD}	#CS = V_{IL} (max.), I/O = 0 mA; Cycle = min. Duty = 100%	-	20	mA
Standby Power Supply Current	I_{SB}	#CS = V_{IH} (min.)	-	0.3	mA
	I_{SB1}	#CS ≥ V_{DD} -0.2V	-	5	µA

CAPACITANCE

(T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

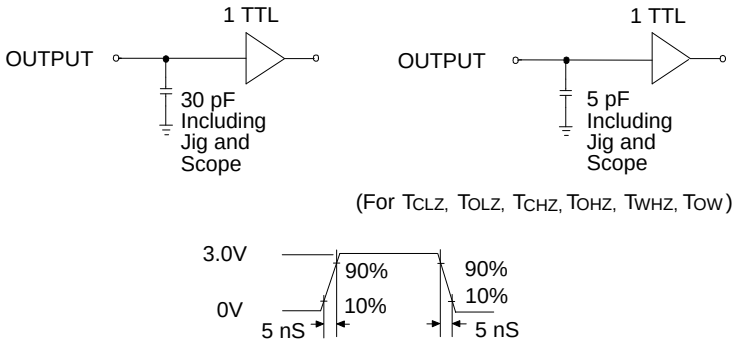
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



AC Characteristics, continued

(V_{SS} = 0V; T_A (°C) = -20 to 85 for LE, -40 to 85 for LI)

Read Cycle

PARAMETER	SYM.	W24B02-55		W24B02-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	55	-	70	-	nS
Address Access Time	T_{AA}	-	55	-	70	nS
Chip Select Access Time	T_{ACS}	-	55	-	70	nS
Output Enable to Output Valid	T_{AOE}	-	35	-	35	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	10	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	25	-	30	nS
Output Disable to Output in High Z	T_{OHZ}*	-	25	-	30	nS
Output Hold from Address Change	T_{OH}	10	-	10	-	nS

∗These parameters are sampled but not 100% tested

Write Cycle

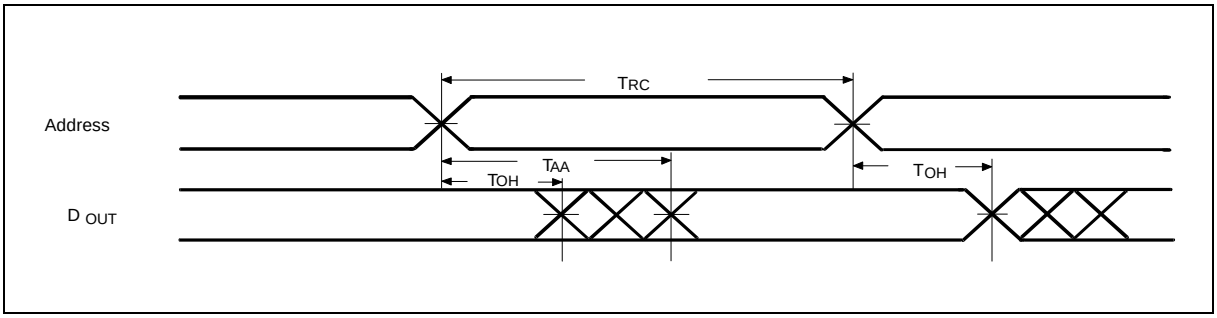
PARAMETER		SYM.	W24B02-55		W24B02-70		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	55	-	70	-	nS
Chip Selection to End of Write		T_{CW}	45	-	60	-	nS
Address Valid to End of Write		T_{AW}	45	-	60	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	45	-	55	-	nS
Write Recovery Time	#CS, #WE	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	40	-	40	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	25	-	30	nS
Output Disable to Output in High Z		T_{OHZ}*	-	25	-	30	nS
Output Active from End of Write		T_{OW}	5	-	5	-	nS

∗These parameters are sampled but not 100% tested

TIMING WAVEFORMS

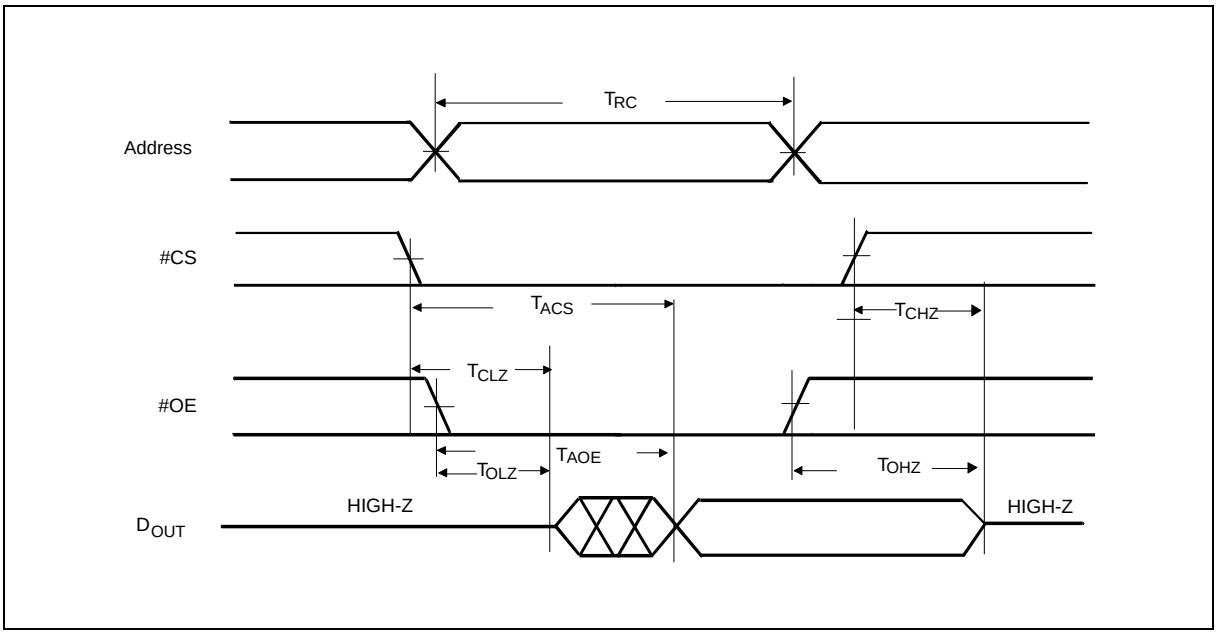
Read Cycle 1

(Address Controlled)



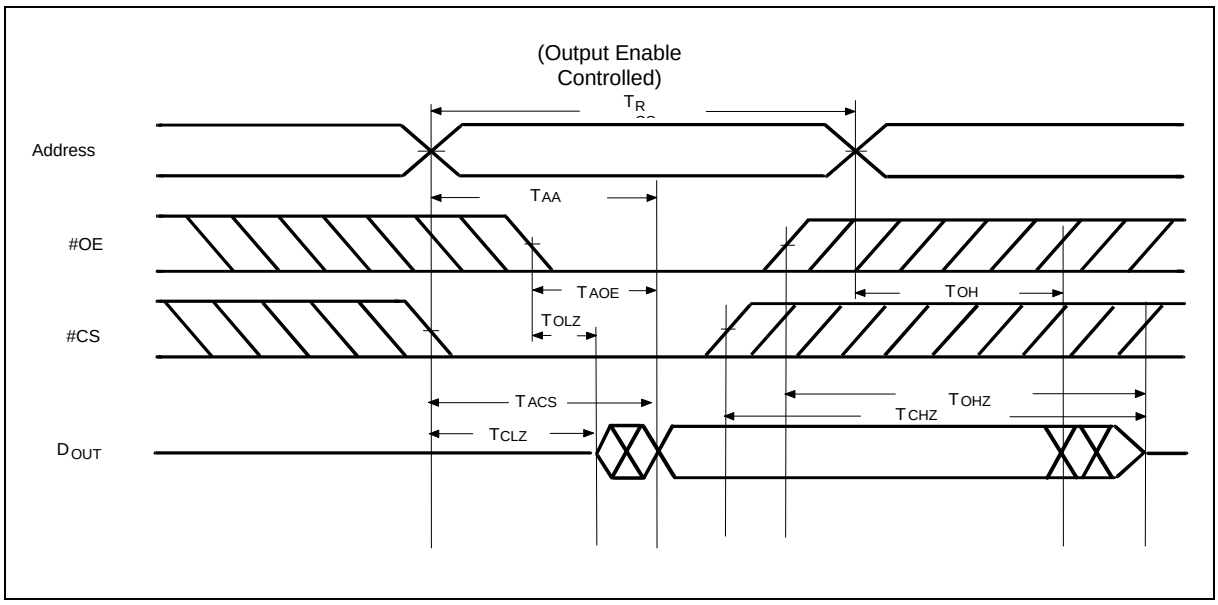
Read Cycle 2

(Chip Select Controlled, #OE = VIL, **#WE**= VIH**)**



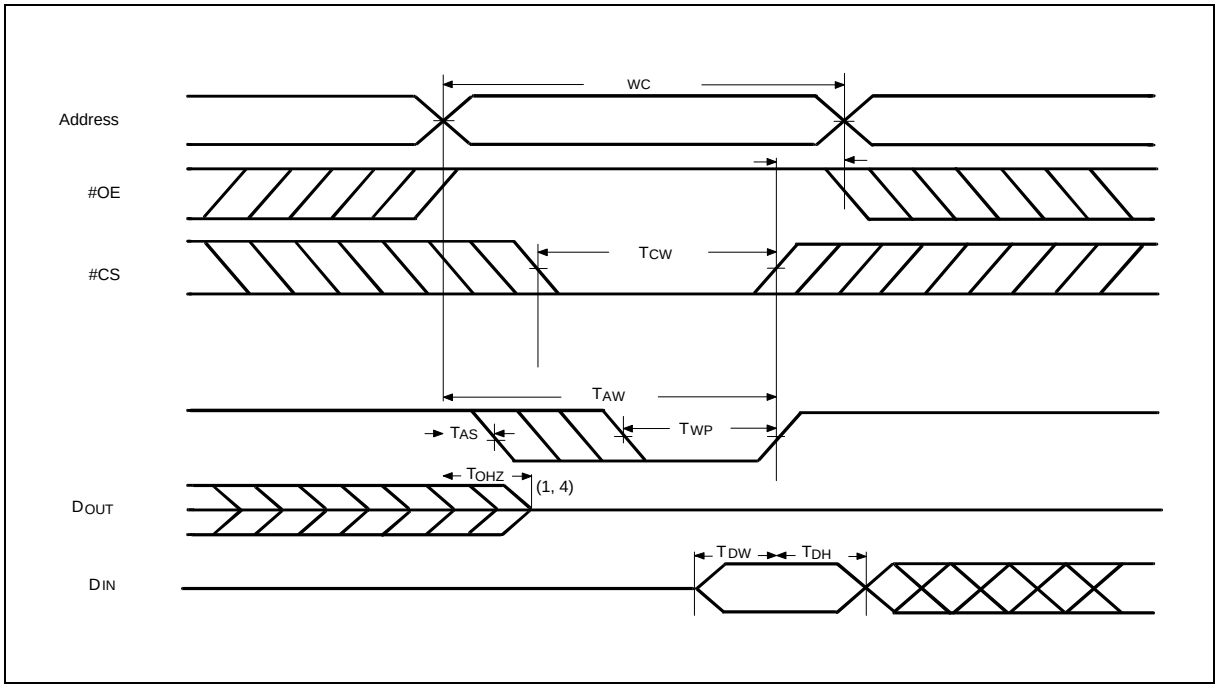
Timing Waveforms, continued

Read Cycle 3



Write Cycle 1

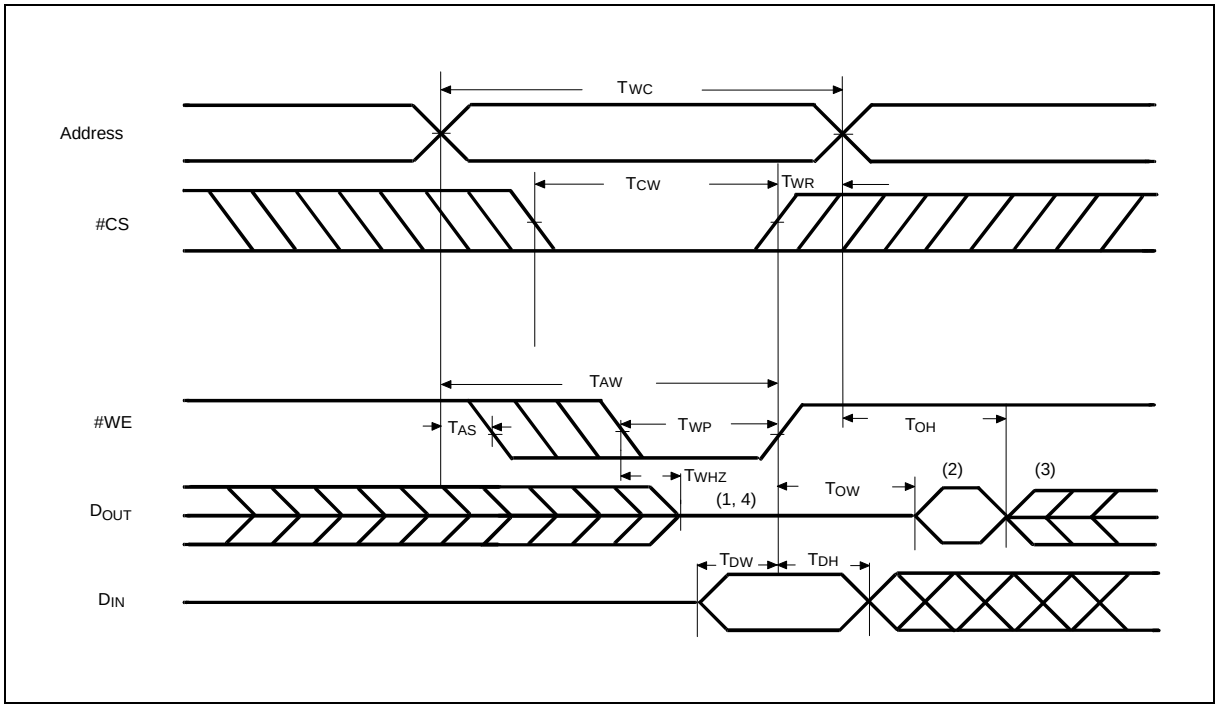
(#OE Clock)



Timing Waveforms, continued

Write Cycle 2

(#OE = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

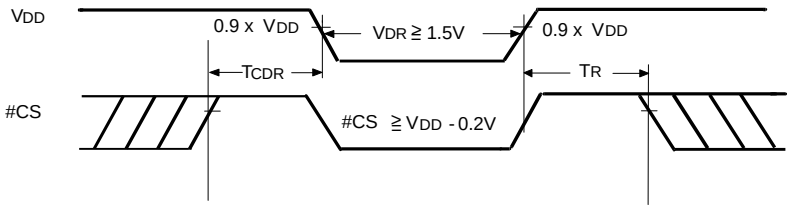
DATA RETENTION CHARACTERISTICS

(T_A (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	#CS ≥ V_{DD} -0.2V	1.5	-	-	V
Data Retention Current	I_{DDDR}	#CS ≥ V_{DD} -0.2V, V_{DD} = 3.0V	-	-	5	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T_R		T_{RC}*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

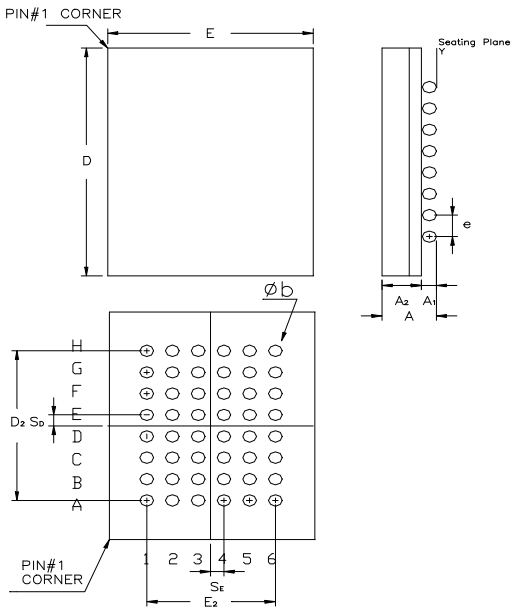
PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V) STANDBY CURRENT (µA)	OPERATING TEMPERATURE (°C)	PACKAGE
W24B02B-70LE	70	3V/5 µA	-20 to 85	TFBGA
W24B02Q-70LE	70	3V/5 µA	-20 to 85	TSOP I (8 x 13.4 mm)
W24B02T-70LE	70	3V/5 µA	-20 to 85	TSOP I (8 x 20 mm)
W24B02B-70LI	70	3V/5 µA	-40 to 85	TFBGA
W24B02Q-70LI	70	3V/5 µA	-40 to 85	TSOP I (8 x 13.4 mm)
W24B02T-70LI	70	3V/5 µA	-40 to 85	TSOP I (8 x 20 mm)
W24B02B-55LE	55	3V/5 µA	-20 to 85	TFBGA
W24B02Q-55LE	55	3V/5 µA	-20 to 85	TSOP I (8 x 13.4 mm)
W24B02T-55LE	55	3V/5 µA	-20 to 85	TSOP I (8 x 20 mm)
W24B02B-55LI	55	3V/5 µA	-40 to 85	TFBGA
W24B02Q-55LI	55	3V/5 µA	-40 to 85	TSOP I (8 x 13.4 mm)
W24B02T-55LI	55	3V/5 µA	-40 to 85	TSOP I (8 x 20 mm)

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

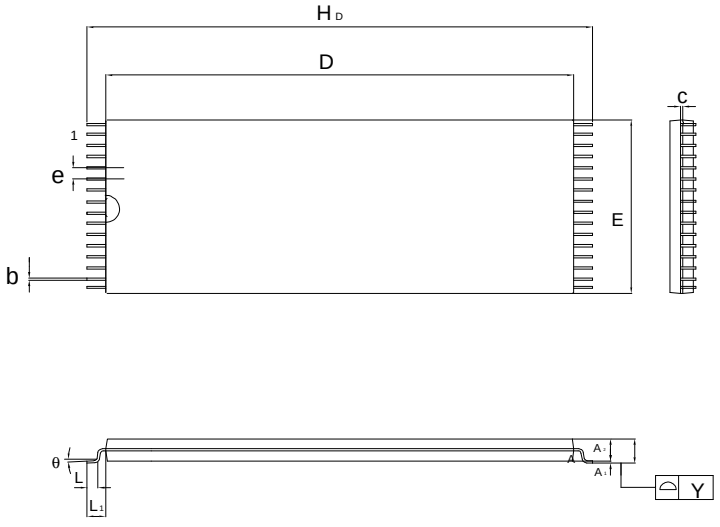
TFBGA



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	inch			millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.035	0.039	0.043	0.9	1.0	1.10
A1	0.008	0.011	0.012	0.20	0.27	0.30
A2	0.025	0.028	0.031	0.64	0.72	0.8
Øb	0.012	0.014	0.016	0.30	0.35	0.40
D	0.313	0.315	0.317	7.95	8.00	8.05
E	0.234	0.236	0.238	5.95	6.00	6.05
e	–	0.030	–	–	0.75	–
E2	0.148 BASIC			3.75 BASIC		
D2	0.207 BASIC			5.25 BASIC		
SD	0.015 BASIC			0.375 BASIC		
SE	0.015 BASIC			0.375 BASIC		
y	–	–	0.004	–	–	0.10

32-Lead Small Type One TSOP (8x13.4)

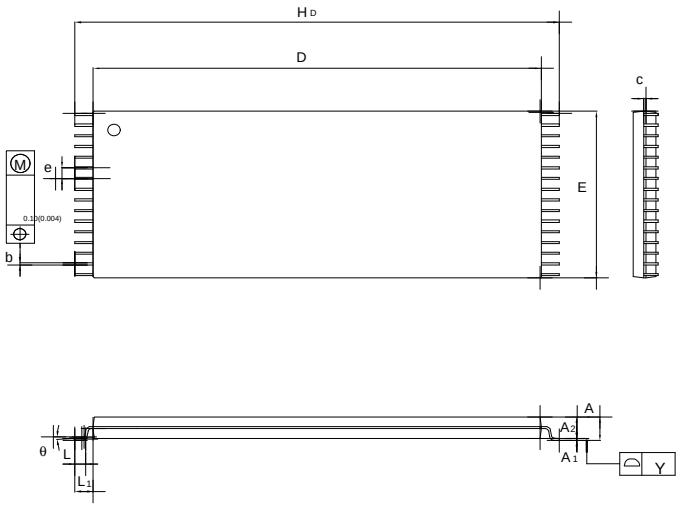


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.049	—	—	1.25
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.27
c	0.0056	0.0059	0.0062	0.14	0.15	0.16
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
HD	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.020	—	—	0.50	—
L	0.012	0.020	0.028	0.30	0.50	0.70
L1	0.027	—	—	0.675	—	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

Package Dimensions, continued

32-Lead TSOP (8 x 20 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 6, 2002	-	Initial Issued

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