MICRON

MT4(L)C1M16C3/5/6/7
1 MEG x 16 WIDE DRAM

WIDE DRAM

1 MEG x 16 DRAM

5.0V FAST-PAGE-MODE (MT4C1M16C3/5/6/7)
3.0/3.3V, FAST-PAGE-MODE (MT4LC1M16C3/5/6/7)

WIDE DRAM

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V only or +3.0/+3.3V only ±10% power supply
- Low-power, 5mW standby; 500mW active, typical (5V)
- All device pins are TTL-compatible
- 1,024-cycle refresh in 16ms (ten rows and ten columns)
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C1M16C3/5 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1M16C5/7 only)

OPTIONS   MARKING

- Timing
  - 60ns access   -6
  - 70ns access   -7
  - 80ns access   -8

- Power Supply
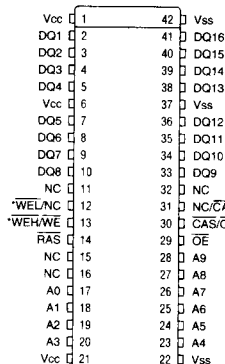 - +5V ±10% only   4C
  - +3.0/3.3V ±10% only   4LC

- Refresh Rate
  - 1,024 rows   None
  - 4,096 rows   Contact Factory

- WRITE Cycle Access
  - BYTE or WORD via CAS (nonmaskable)   16C3
  - BYTE or WORD via CAS (maskable)   16C5
  - BYTE or WORD via WE (nonmaskable)   16C6
  - BYTE or WORD via WE (maskable)   16C7

- Packages
  - Plastic SOJ (400 mil)   DJ
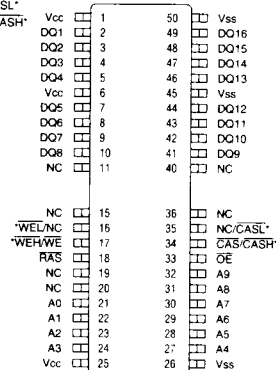 - Plastic TSOP (400 mil)   TG

- Part Number Example: MT4C1M16C3DJ-7

PIN ASSIGNMENT (Top View)

42-Pin SOJ (DC-7)

Vcc	1	42	Vss
DQ1	2	41	DQ16
DQ2	3	40	DQ15
DQ3	4	39	DQ14
DQ4	5	38	DQ13
Vcc	6	37	Vss
DQ5	7	36	DQ12
DQ6	8	35	DQ11
DQ7	9	34	DQ10
DQ8	10	33	DQ9
NC	11	32	NC
*WEL/NC	12	31	NC/CASL*
*WEH/WE	13	30	CAS/CASH*
RAS	14	29	OE
NC	15	28	A9
NC	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
Vcc	21	22	Vss

44-Pin TSOP (DD-6)

Vcc	1	50	Vss
DQ1	2	49	DQ16
DQ2	3	48	DQ15
DQ3	4	47	DQ14
DQ4	5	46	DQ13
Vcc	6	45	Vss
DQ5	7	44	DQ12
DQ6	8	43	DQ11
DQ7	9	42	DQ10
DQ8	10	41	DQ9
NC	11	40	NC
NC	15	36	NC
*WEL/NC	16	35	NC/CASL*
*WEH/WE	17	34	CAS/CASH*
RAS	18	33	OE
NC	19	32	A9
NC	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
Vcc	25	26	Vss

*MT4C1M16C6/7 / MT4C1M16C3/5

GENERAL DESCRIPTION

The MT4C1M16C3/5/6/7 and MT4LC1M16C3/5/6/7 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x16 configuration. The MT4C1M16C3/5/6/7 and the MT4LC1M16C3/5/6/7 are the same DRAM versions except that the MT4LC1M16C3/5/6/7 is the low-voltage version of MT4C1M16C3/5/6/7. The MT4LC1M16C3/5/6/7 is designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C1M16C3/5/6/7 also apply to the MT4LC1M16C3/5/6/7, unless specifically stated otherwise. The MT4C1M16C6 and MT4C1M16C7 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C1M16C3 and MT4C1M16C5 have both BYTE WRITE and WORD WRITE access cycles

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via two $\overline{CAS}$ pins. The MT4C1M16C5 and MT4C1M16C7 are also able to perform WRITE-PER-BIT accesses.
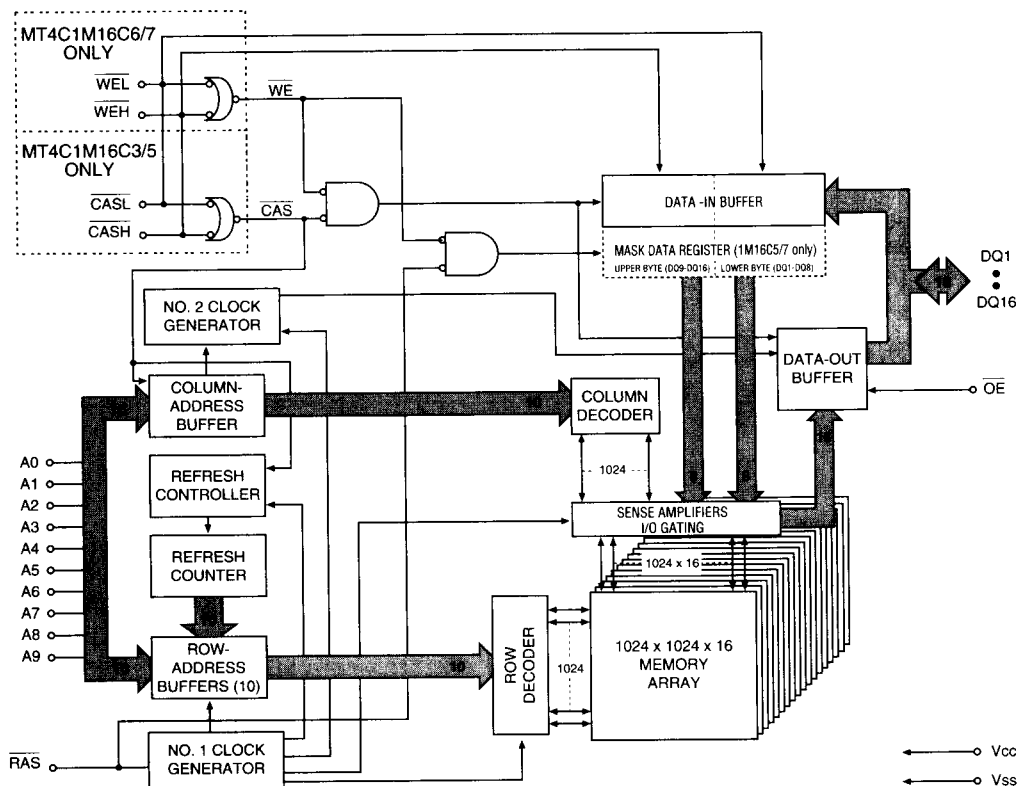
The MT4C1M16C3 and MT4C1M16C6 function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C1M16C6 and $\overline{CASL}$ and $\overline{CASH}$ on MT4C1M16C3 control the selection of BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C1M16C6 $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8), and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1M16C3 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C1M16C3.

The MT4C1M16C5 and MT4C1M16C7 function in the same manner as MT4C1M16C3 and MT4C1M16C6, respectively and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C1M16C5 and MT4C1M16C7 to operate with either normal WRITE cycles or NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
14	18	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C1M16C5 and MT4C1M16C7 only).
30	34	$\overline{CAS}/\overline{CASH}$	Input	Column-Address Strobe: $\overline{CAS}$ (MT4C1M16C6/7) is used to latch-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles $\overline{CAS}$ controls DQ1 through DQ16. Column-Address Strobe Upper Byte: $\overline{CASH}$ (MT4C1M16C3/5) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
29	33	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C1M16C6/7) or $\overline{CASL}/\overline{CASH}$ (MT4C1M16C3/5) must be LOW and $\overline{WEL}/\overline{WEH}$ (MT4C1M16C6/7) or $\overline{WE}$ (MT4C1M16C3/5) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	17	$\overline{WEH}/\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C1M16C6/7) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C1M16C7, it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C1M16C3/5) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C1M16C5/7 also use $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
12	16	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C1M16C6/7) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C1M16C3, it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
31	35	NC/$\overline{CASL}$	Input	Column-Address Strobe Lower Byte: $\overline{CASL}$ (MT4C1M16C3/5) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
17-20, 23-28	21-24, 27-32	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}/\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 1 Meg available words.

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PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 33-36, 38-41	2-5, 7-10, 41-44, 46-49	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/7) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C1M16C6/7). The MT4C1M16C3/5 allow for BYTE READ cycles.
11, 15, 16, 30-32	11, 15, 36, 40	NC	-	No Connect: These pins should be left either unconnected or tied to ground.
1, 6, 21	1, 6, 25	Vcc	Supply	Power Supply: +5V ±10% (C) or 2.7V to 3.6V (LC)
22, 37, 42	26, 45, 50	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C1M16C6 and MT4C1M16C7 each have one $\overline{CAS}$ control while the MT4C1M16C3 and MT4C1M16C5 have two, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 1 Meg x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tri-state logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C1M16C3 and MT4C1M16C5 $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C1M16C3 and MT4C1M16C5 both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C1M16C3 or MT4C1M16C5 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the $\overline{WE}$ on the MT4C1M16C6 or MT4C1M16C7. The MT4C1M16C6 and MT4C1M16C7 $\overline{WE}$ function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1M16C6 and MT4C1M16C7) or $\overline{WE}$ (MT4C1M16C3 and MT4C1M16C5).

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8). Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C1M16C3, MT4C1M16C5, MT4C1M16C6 and MT4C1M16C7 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C1M16C6 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C1M16C3 BYTE WRITE and WORD WRITE cycles.

The MT4C1M16C3 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C1M16C3 BYTE READ and WORD READ cycles.

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MASKED WRITE ACCESS CYCLE
### (MT4C1M16C5/7 ONLY)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1M16C3 and MT4C1M16C6 do not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that

bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSISTENT MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same.

Figure 4 illustrates the MT4C1M16C7 MASKED WRITE operation and Figure 5 illustrates the MT4C1M16C5 MASKED WRITE operation.
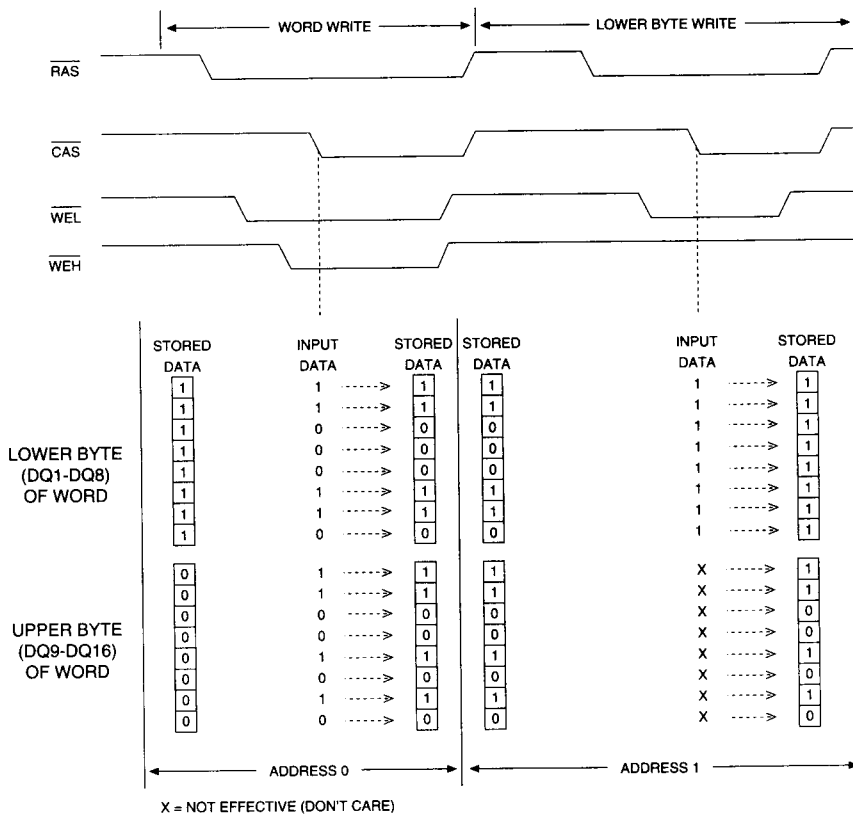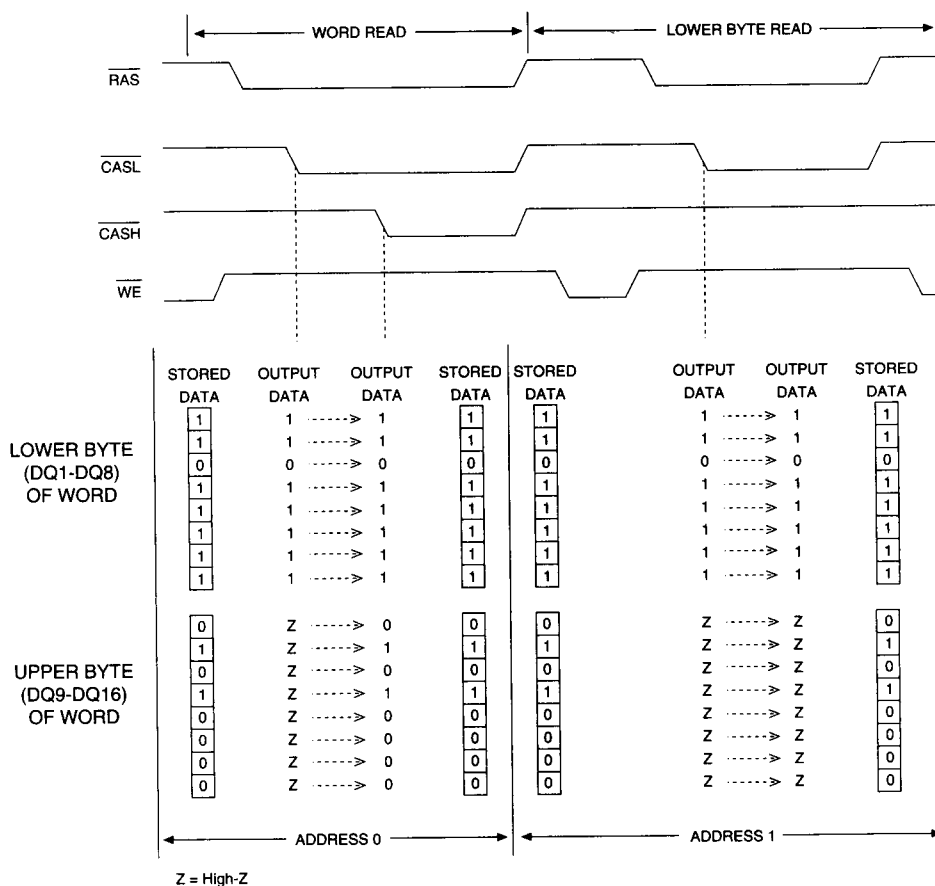

Figure 1
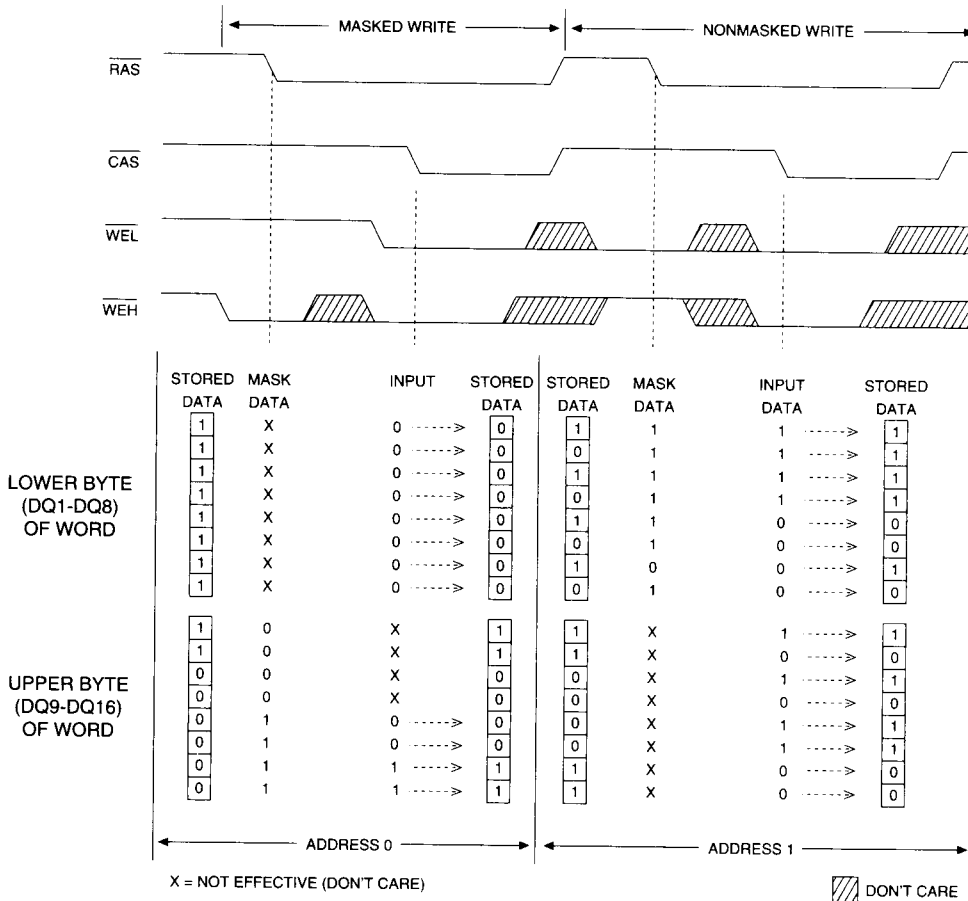**MT4C1M16C6/7 WORD AND BYTE WRITE EXAMPLE**
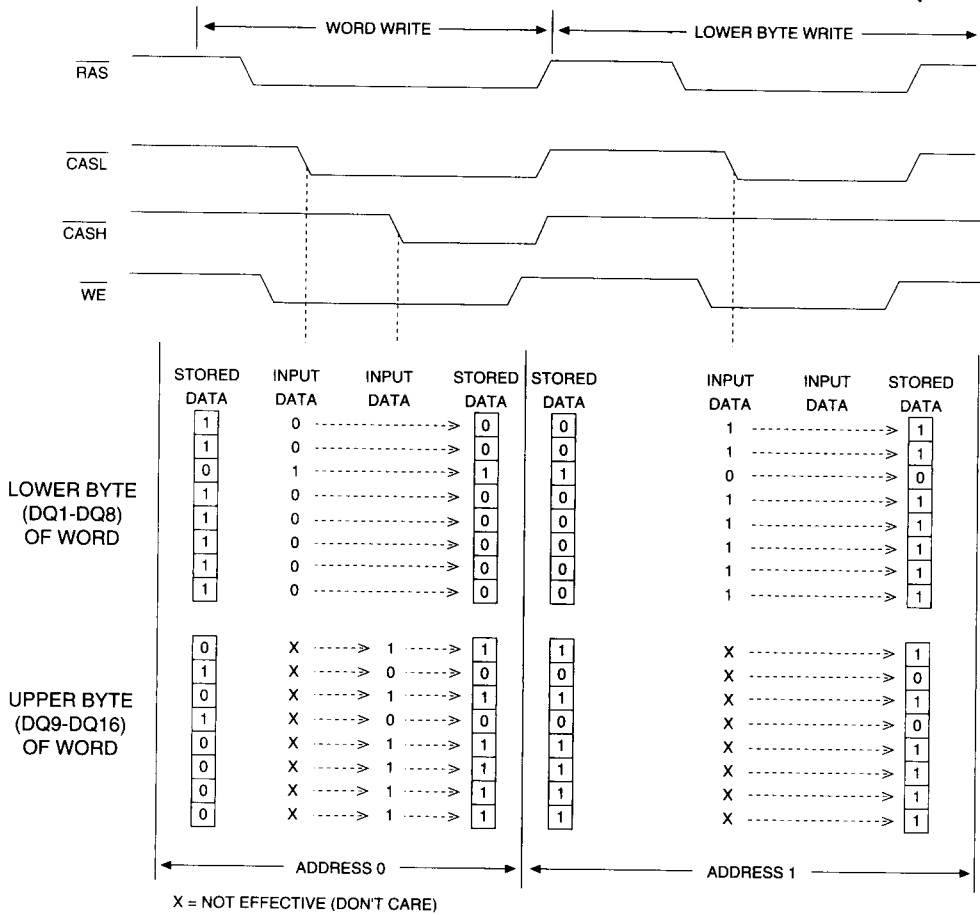
Figure 2
MT4C1M16C3/5 WORD AND BYTE WRITE EXAMPLE

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Figure 3
MT4C1M16C3/5 WORD AND BYTE READ EXAMPLE

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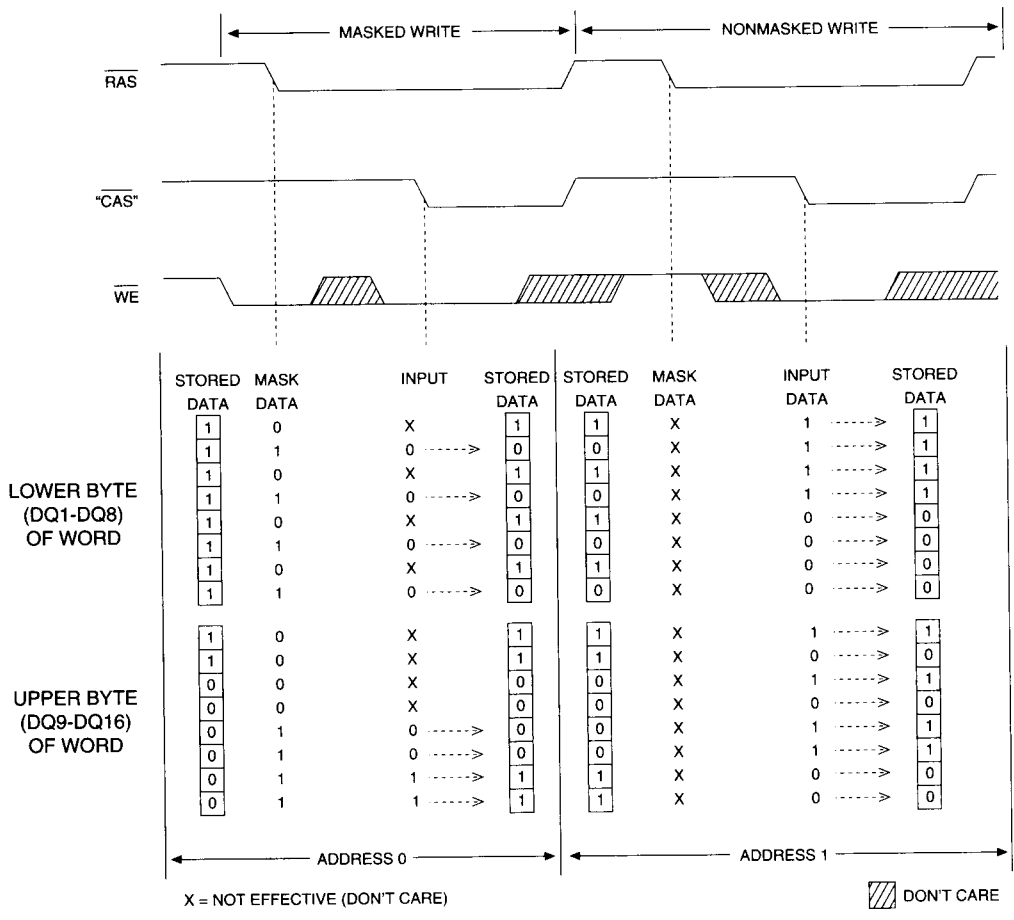SEMICONDUCTOR, INC.

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Figure 4
MT4C1M16C7 MASKED WRITE EXAMPLE

NOTE: If $\overline{WEL}$ is LOW and $\overline{WEH}$ is HIGH when $\overline{RAS}$ goes LOW, then only DQs 1-8 will be masked. If $\overline{WEL}$ is HIGH and $\overline{WEH}$ is LOW when $\overline{RAS}$ goes LOW, then only DQs 9-16 will be masked.

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Figure 5
MT4C1M16C5 MASKED WRITE EXAMPLE

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TRUTH TABLE: MT4C1M16C6/7

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES		DQs	NOTES
							^IR	^IC		
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C1M16C7 only). Refer to Figure 4.

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TRUTH TABLE: MT4C1M16C3/5

FUNCTION		RAS̅	CAS̅L̅	CAS̅H̅	WE̅	OE̅	ADDRESSES tR	tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
READ	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
WRITE	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS̅-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CAS̅L̅ or CAS̅H̅ active).
2. These READ cycles may also be BYTE READ cycles (either CAS̅L̅ or CAS̅H̅ active).
3. EARLY-WRITE only.
4. Only one CAS̅ must be active (CAS̅L̅ or CAS̅H̅).
5. Data-in will be dependent on the mask provided (MT4C1M16C5 only). Refer to Figure 5.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss (5V) .... -1V to +7V
Voltage on Vcc supply relative to Vss (3V) .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C $\leq T_A \leq$ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 44
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	Ii	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	Ioz	-10	10	μA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.1mA)	VOL		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C $\leq T_A \leq$ 70°C; Vcc = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 44
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	Ii	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	Ioz	-10	10	μA	
OUTPUT LEVELS Output High Voltage (IOUT = -1.0mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 1.0mA)	VOL		0.4	V	

WIDE DRAM

WIDE DRAM

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	Icc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS} = \overline{CAS} = Vcc$ -0.2V)	Icc2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	Icc3	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $^tPC = {}^tPC$ [MIN]; ^tCP, ^tASC = 10ns)	Icc4	130	120	110	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $^tRC = {}^tRC$ [MIN])	Icc5	170	160	140	mA	3, 5, 44
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	Icc6	170	160	140	mA	3, 5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C ≤ T_A ≤ 70°C; Vcc = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	Icc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS} = \overline{CAS} = Vcc$ -0.2V)	Icc2	1	1	1	μA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	Icc3	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $^tPC = {}^tPC$ [MIN]; ^tCP, ^tASC = 10ns)	Icc4	130	120	110	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $^tRC = {}^tRC$ [MIN])	Icc5	170	160	140	mA	3, 4, 44
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	Icc6	170	160	140	mA	3, 4

MICRON

WIDE DRAM

CAPACITANCE
(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$)

AC CHARACTERISTICS PARAMETER	SYM	-6 MIN	-6 MAX	-7 MIN	-7 MAX	-8 MIN	-8 MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable	^tOE		15		15		15	ns	23
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	32
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	31
Column-address hold time	^tCAH	10		15		15		ns	31
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	33

MICRON

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T$_A$ ≤ +70°C; Vcc = 5V or 3.0/3.3V ±10%)

AC CHARACTERISTICS PARAMETER	SYM	-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Output buffer turn-off delay	^{t}OFF	3	15	3	20	3	20	ns	20, 29, 33
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	21, 26, 31
Write command hold time	^{t}WCH	10		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	26
Write command pulse width	^{t}WP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	26, 32
Data-in setup time	^{t}DS	0		0		0		ns	22, 33
Data-in hold time	^{t}DH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		45		45		ns	21, 31
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		5		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		15		ns	5, 32
$\overline{WE}$ hold time (MASKED WRITE and CBR REFRESH)	^{t}WRH	15		15		15		ns	26, 27
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	^{t}WRS	10		10		10		ns	26, 27
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
Output disable	^{t}OD	3	15	3	15	3	15	ns	29, 41
$\overline{OE}$ hold time from $\overline{WE}$ during HIDDEN REFRESH cycle	^{t}OEH	15		15		15		ns	28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^{t}CLCH	10		10		10		ns	34
Mask data to $\overline{RAS}$ setup time	^{t}MS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^{t}MH	15		15		15		ns	26, 27

WIDE DRAM

WIDE DRAM

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V or 3.0/3.3V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100μs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.

19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.*
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE and READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1M16C6/7. Write command is defined as $\overline{WE}$ going LOW on the MT4C1M16C3/5.
27. MT4C1M16C5/7 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

*The 3ns minimum is a parameter guaranteed by design.

NOTES (continued)

30. Notes 31 through 41 apply to MT4C1M16C3/5 only.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.

39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. The 5V version is restricted to operate between 4.5 V and 5.5V only.
43. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only. The -6 speed version is only valid for Vcc = 3.0V to 3.6 V whereas the -7 and -8 speed versions are valid for Vcc = 2.7V to 3.6V.
44. Column-address changed once while $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
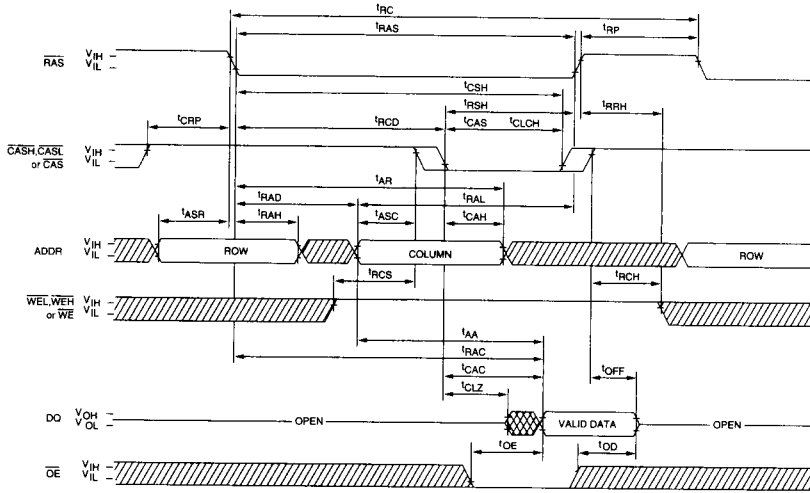
READ CYCLE

EARLY-WRITE CYCLE
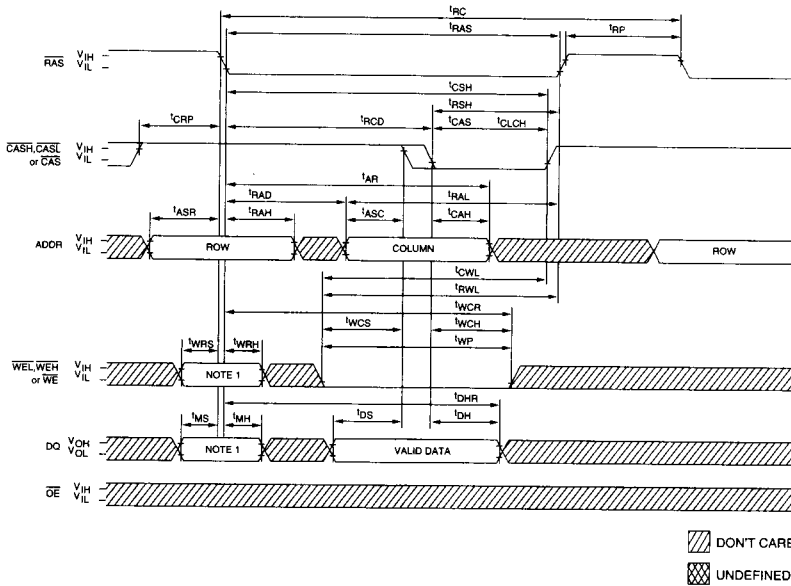
WIDE DRAM

▨ DON'T CARE

▨ UNDEFINED
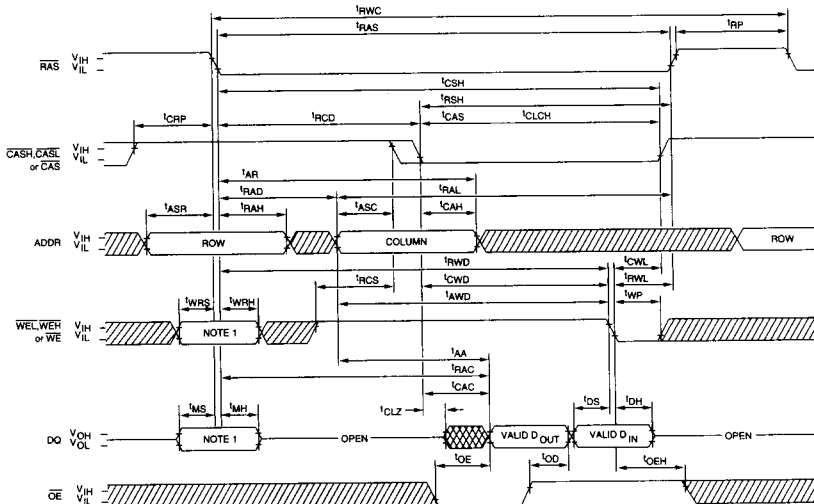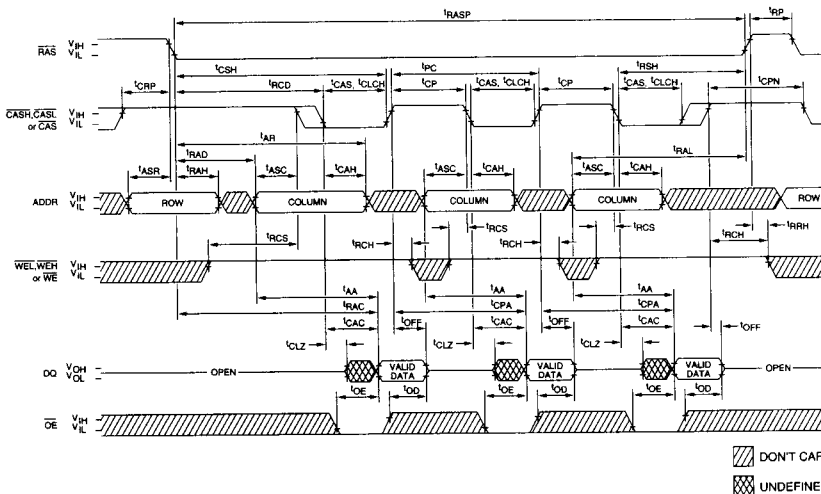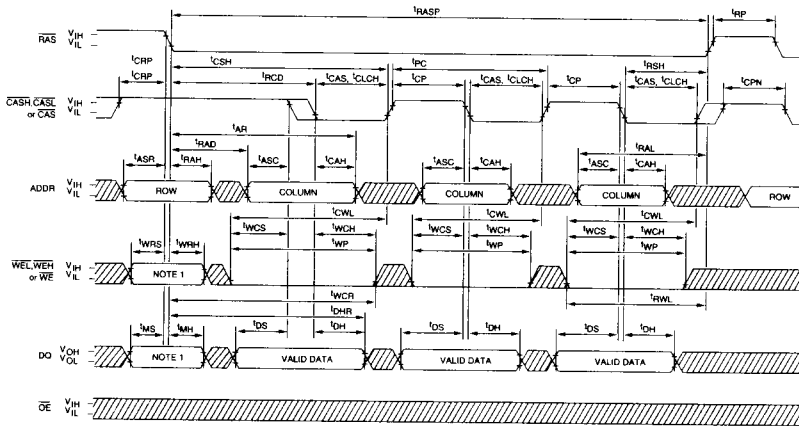
NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at $\overline{RAS}$ time.

WIDE DRAM

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

FAST-PAGE-MODE READ CYCLE

▨ DON'T CARE

▧ UNDEFINED

NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

DON'T CARE

UNDEFINED

NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at RAS time.

WIDE DRAM

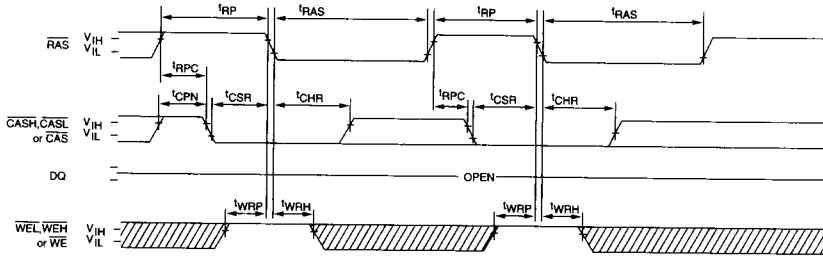## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)
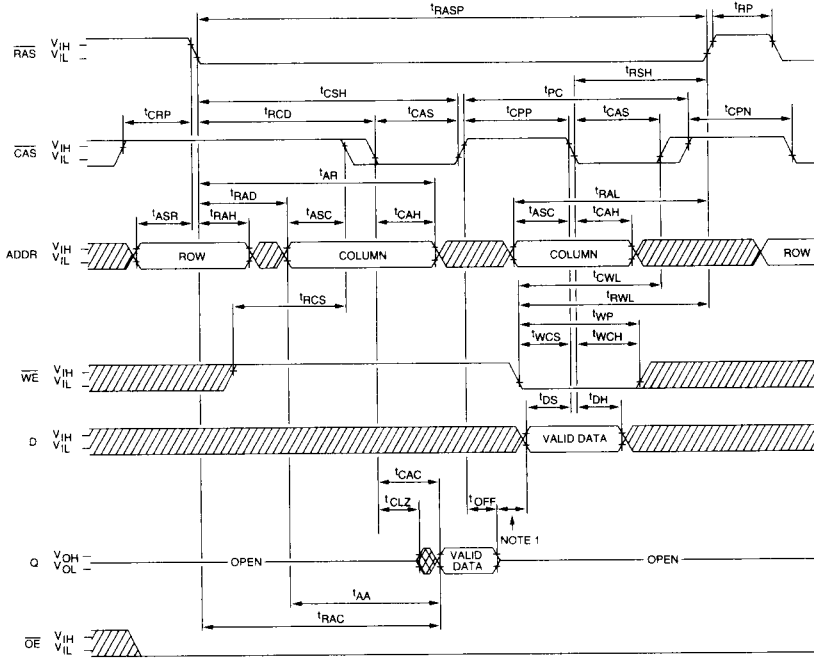
NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

RAS-ONLY REFRESH CYCLE
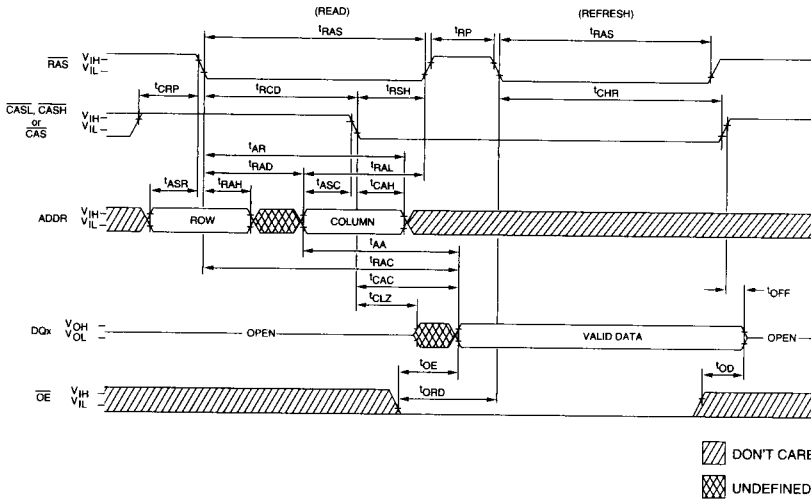### (ADDR = A0-A9, OE; WEL, WEH or WE = DON'T CARE)
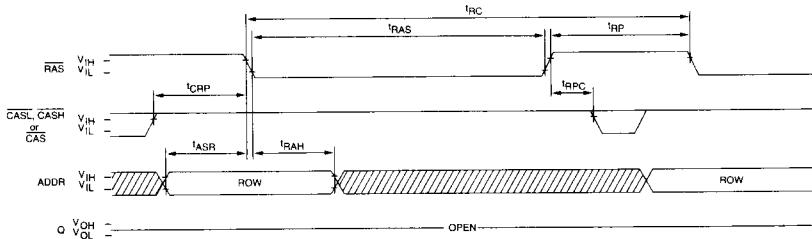
DON'T CARE

UNDEFINED

WIDE DRAM

CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)

HIDDEN REFRESH CYCLE [24]
($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)

▨ DON'T CARE

▨ UNDEFINED