Advance Information

MPA17000 Serial EEPROM

MPA17C256

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The MPA17C256 is an easy to use and cost effective serial configuration memory ideally suited for use with today's popular SRAM based FPGAs. The MPA17C256 is available in 8–pin PDIP and 20–pin SOIC and PLCC packages, adhering to industry standard pinouts. The device interfaces downstream FPGA(s) with a very simple enable, clock and data interface. The MPA17C256 is reprogrammable with no need for a higher programming "super voltage"; it may even be reprogrammed on board. The MPA17C256 also has user programmable RESET/$\overline{OE}$ polarity.

- EE Programmable 262,144 x 1 bit Serial Memories Designed to Store Configuration Programs for FPGAs
- Simple Interface to SRAM FPGAs
- Cascadable to Support Additional Configurations or Future Higher Density FPGAs
- Low Power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in Space Efficient 8–Pin PDIP, 20–Pin SOIC and 20–Pin PLCC Packages
- In–System Programmable via 2–Wire Bus

P SUFFIX
8–LEAD PLASTIC PACKAGE
CASE 626–05

DW SUFFIX
20–LEAD PLASTIC SOIC WIDE PACKAGE
CASE 751D–04

FN SUFFIX
20–LEAD PLCC PACKAGE
CASE 775–02

Controlling the MPA17C256 Serial EEPROM

Most connections between the FPGA device and the Serial EEPROM are simple and self–explanatory:

- The DATA output of the MPA17C256 drives DIN of the FPGA devices
- The master FPGA DCLK output drives the CLK input of the MPA17C256
- The $\overline{CEO}$ output of the first MPA17C256 drives the $\overline{CE}$ input of the next MPA17C256 in a cascade chain of EEPROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC}
- $\overline{CE}$ enables the chip and is required to enable the DATA output pin
- RESET/$\overline{OE}$ is chip reset and is part of the DATA output enable structure

PIN NAMES

Pins	Function
DATA	Data I/O
CLK	Clock
RESET/$\overline{OE}$	Reset Input and Output Enable
$\overline{CE}$	Chip Enable Input
V_{SS}	Ground
$\overline{CEO}$	Chip Enable Output
$\overline{SER\_EN}$	Programming Enable
V_{CC}	+4.5 to 6.0V Power Supply
NC	Not Connected

The simplest connection to a Motorola Programmable array (MPA) is shown below. In this configurations, the $\overline{MEMCE}$ output of the MPA enables the MPA17C256 and takes it out of reset. Shortly after, the first bit of configuration data will appear on DATA. Subsequent rising edges of DCLK bring out the next bits. For more complex connections, including cascading of EEPROMs and cascading of MPA devices, please consult the MPA databook (DL201/D).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

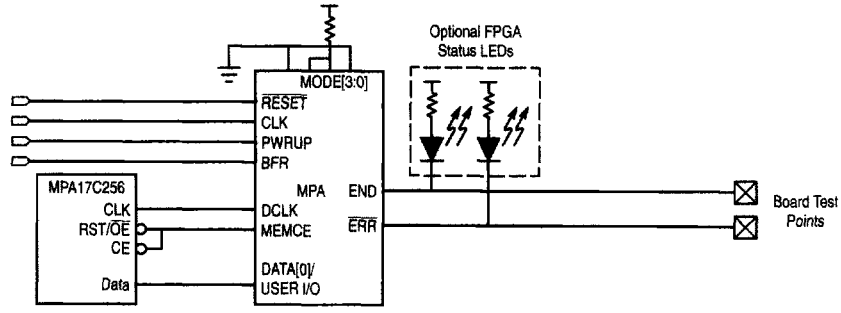

Figure 2–57. BFR Mode 2: 1–Bit (Serial) Data, External Address, External Clock

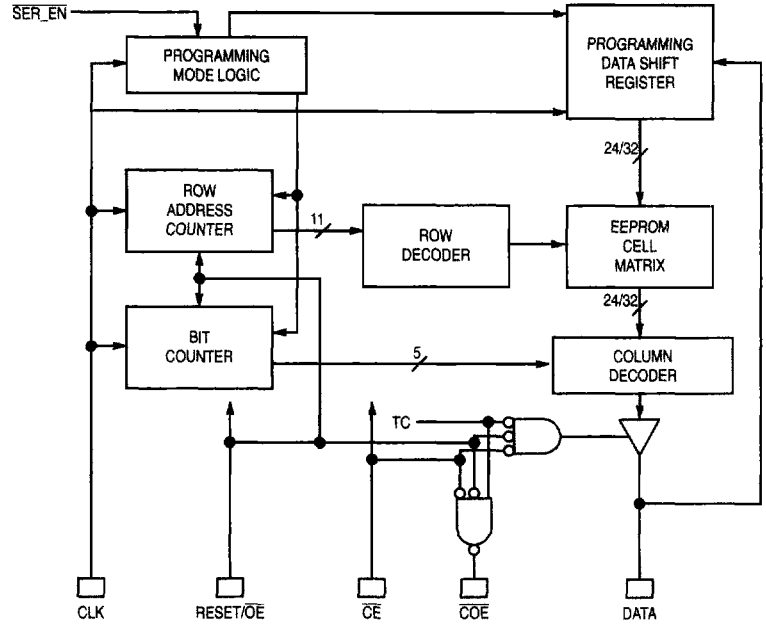

Figure 2–58. Block Diagram

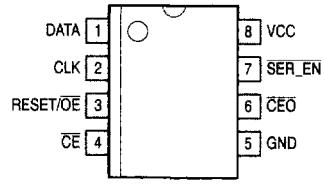

Figure 2–59. 8–Lead DIP Pinout

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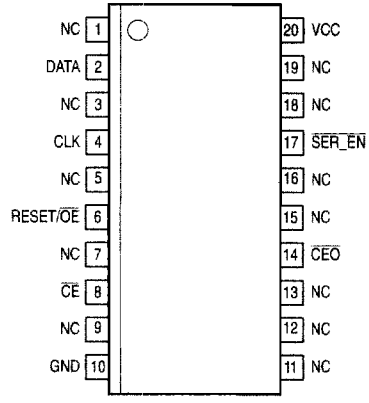

Figure 2–60. 20–Lead SOIC Pinout

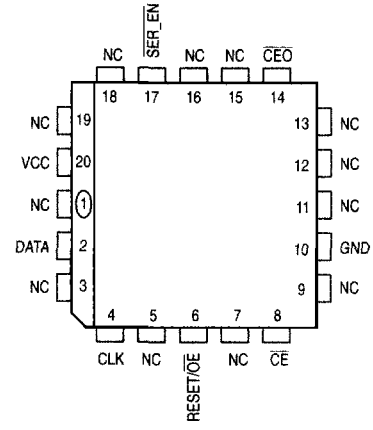

Figure 2–61. 20–Lead PLCC Pinout

Table 2–23. PIN DESCRIPTIONS

PLCC/ SOIC	DIP	Name	I/O	Description
2	1	DATA	I/O	Three–State DATA output for reading. Input/Output pin for programming
4	2	CLK	I	Clock Input. Rising edge used to increment the internal address and bit counter for reading and programming
6	3	RESET/$\overline{OE}$	I	RESET/Output Enable input (when $\overline{SER\_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
		RESET Polarity Selected	I	RESET Polarity Select Input. During programming, when $\overline{CE}$ is High, this input is used to determine the polarity of the pin when $\overline{SER\_EN}$ is High.
		WP	I	Write Protect (WP) input. When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest 1/4 of the memory cannot be written; i.e., 64K in MPA17C256. Note that when WP is High, the chip will still acknowledge the receipt of data, but it will not write it into memory.
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection only when $\overline{SER\_EN}$ is High. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode. Note this pin will not enable/disable the device in 2–wire Serial mode (i.e., when $\overline{SER\_EN}$ is Low). During programming, and when $\overline{CE}$ is Low, the main array is read and written. When $\overline{CE}$ is High, the main array is deselected and a Serial WRITE operation will change the polarity of the RESET pin.
10	5	GND	–	Ground Pin
14	6	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
		A2	I	Device selection input, A2. Used to enable (select) the device during programming. When $\overline{SER\_EN}$ is Low, this pin MUST be at either a logic level '1' or '0' (i.e., not 3–state) and the A2 contents of the Device Address must match the condition of the pin for the device to be selected.
17	7	$\overline{SER\_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low, enables the two wire serial interface mode for programming.
20	8	V_{CC}	–	+5V Power Supply input

Table 2–24. MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
	Voltage Applied to Output in High Output State	–0.1 to V_{CC}+0.5V	V
T_A	Operating Temperature Range (In Free-Air)	–55 to +125	°C
T_{STG}	Storage Temperature Range	–65 to +150	°C
T_{SOL}	Maximum Soldering Temperature (10s @ 1/16in)	260	°C
ESD	R_{ZAP} = 1.5K, C_{ZAP} = 100pF	2000	V

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Table 2–25. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage Relative to Ground	Commercial (–0 to +70°C)	4.75	5.25	V
		Industrial (–40 to +85°C)	4.50	5.50	

Table 2–26. DC CHARACTERISTICS OVER OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{IH}	High Level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
V_{OH}	High Level Output Voltage	Commercial Industrial	3.86 3.76		V
V_{OL}	Low Level Output Voltage	Commercial Industrial		0.32 0.37	V
I_{CCA}	Supply Current, Active Mode			10	mA
I_{IL}	Input/Output Leakage Current (V_{in} = V_{CC} or GND)		–10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial Industrial		1 2	mA

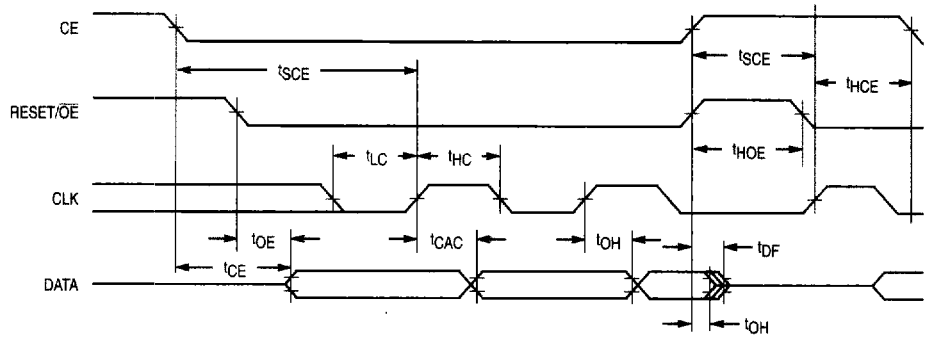

Figure 2–62. AC Characteristics Over Operating Conditions

Table 2–27. AC CHARACTERISTICS OVER OPERATING CONDITIONS (Note 1.)

Symbol	Parameter	Commercial		Industrial		Unit
		Min	Max	Min	Max	
t_{OE}	$\overline{OE}$ to Data Delay		110		150	ns
t_{CE}	$\overline{CE}$ to Data Delay		50		50	ns
t_{CAC}	CLK to Data Delay		50		55	ns
t_{OH}	Data Hold from $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
t_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay (Note 2.)		50		50	ns
t_{LC}	CLK Low Time	30		35		ns
t_{HC}	CLK High Time	30		35		ns
t_{SCE}	$\overline{CE}$ Setup Time to CLK (To Guarantee Proper Counting)	45		50		ns
t_{HCE}	$\overline{CE}$ Hold Time to CLK (To Guarantee Proper Counting)	0		5		ns
t_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	50		60		ns
f_{max}	Maximum Input Clock Frequency		10		10	MHz

1. AC test load = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ±500mV from steady state active levels.

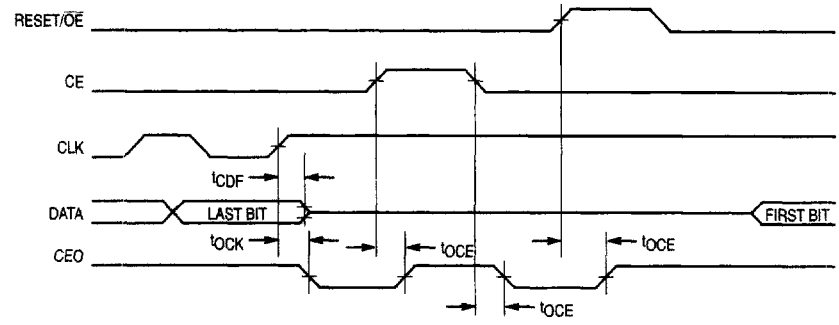

Figure 2–63. AC Characteristics Over Operating Conditions When Cascading

Table 2–28. AC CHARACTERISTICS OVER OPERATING CONDITIONS WHEN CASCADING

Symbol	Parameter	Commercial		Industrial		Unit
		Min	Max	Min	Max	
t_{CDF}	CLK to Data Float Delay		50		50	ns
t_{OCK}	CLK to $\overline{CEO}$ Delay		65		75	ns
t_{OCE}	CE to $\overline{CEO}$ Delay		55		60	ns
t_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		55		55	ns

Table 2–29. DC CHARACTERISTICS (V_{CC} = 5.0V ±5%)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}	Supply Voltage	4.75	5.00	5.25	V	
I_{CC}	Supply Current		2.0	5.0	mA	V_{CC} = 5V
I_{LL}	Input Leakage Current		0.10	3.00	µA	V_{in} = V_{CC} or V_{SS}
I_{LO}	Output Leakage Current		0.05	3.00	µA	V_{out} = V_{CC} or V_{SS}
V_{IH}	High Level Input Voltage	V_{CC} × 0.7		V_{CC} + 0.5	V	
V_{IL}	Low Level Input Voltage	–0.5		0.4	V	
V_{OL}	Output Low Level Voltage			0.4	V	I_{OL} = 3mA

Table 2–30. DC CHARACTERISTICS (V_{CC} = 3.3V ±10%)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
I_{CC}	Supply Current		2.0	3.0	mA	V_{CC} = 3.6V
I_{LL}	Input Leakage Current		0.10	3.00	µA	V_{in} = V_{CC} or V_{SS}
I_{LO}	Output Leakage Current		0.05	3.00	µA	V_{out} = V_{CC} or V_{SS}
V_{IH}	High Level Input Voltage	V_{CC} × 0.7		V_{CC} + 0.5	V	
V_{IL}	Low Level Input Voltage	–0.5		0.2	V	
V_{OL}	Output Low Level Voltage			0.4	V	I_{OL} = 2.1mA

Table 2–31. AC CHARACTERISTICS (V_{CC} = 5.0V ±5%)

Symbol	Parameter	Min	Max	Unit
f_{Clock}	Clock Frequency, Clock		400	kHz
t_{Low}	Clock Pulse Width Low	1.2		µs
t_{High}	Clock Pulse Width High	0.8		µs
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{Buf}	Time the Bus Must Be Free Before a New Transmission Can Start	1.2		µs
t_{HST}	Start Hold Time	0.6		µs
t_{SST}	Start Setup Time	0.6		µs
t_{HDA}	Data In Hold Time	0		µs
t_{SDA}	Data In Setup Time	100		ns
t_r	Input Rise Time		0.3	µs
t_f	Input Fall Time		300	ns
t_{SSTP}	Stop Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		10	ms

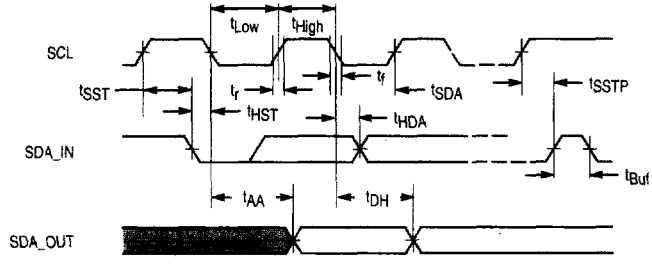

Figure 2–64. Serial Data Timing Diagram

Table 2–32. AC CHARACTERISTICS (V_{CC} = 3.3V ±10%)

Symbol	Parameter	Min	Max	Unit
f_{Clock}	Clock Frequency, Clock		100	kHz
t_{Low}	Clock Pulse Width Low	4.0		µs
t_{High}	Clock Pulse Width High	4.0		µs
t_{AA}	Clock Low to Data Out Valid	0.1	1.0	µs
t_{Buf}	Time the Bus Must Be Free Before a New Transmission Can Start	4.5		µs
t_{HST}	Start Hold Time	2.0		µs
t_{SST}	Start Setup Time	2.0		µs
t_{HDA}	Data In Hold Time	0		µs
t_{SDA}	Data In Setup Time	200		ns
t_r	Input Rise Time		0.3	µs
t_f	Input Fall Time		300	ns
t_{SSTP}	Stop Setup Time	2.0		µs

Table 2–32. AC CHARACTERISTICS (V_{CC} = 3.3V ±10%)

Symbol	Parameter	Min	Max	Unit
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		20	ms

Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy–chain, or for future FPGAs requiring larger configuration memories, cascading MPA17C256s provides additional memory.

After the last bit from the first MPA17C256 is read, the next clock signal asserts its $\overline{CEO}$ output LOW and disables its DATA line. The second MPA17C256 recognizes the LOW level on its $\overline{CE}$ input and enables its DATA output.

Standby Mode

The MPA17C256 enters a low power standby mode whenever $\overline{CE}$ is asserted HIGH. In this mode, it consumes less than 1.0mA of current. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

MPA17C256 Reset Polarity

The MPA17C256 lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE.

Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ LOW. In this mode, the chip can be programmed by a 2–wire interface. The programming is done at V_{CC} supply only. Programming (high) voltages are generated inside the chip. For additional programming information, see the Programmer's Guide section on page 2–71.

2

Programmer's Guide

Serial Bus Overview

The serial bus is a two wire bus; one wire (CLOCK) functions as a clock and is provided by the programmer, the second wire (DATA) is a bi–directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a START BIT and is ended with a STOP BIT. The message consists of an integer number of bytes, each byte consists of 8 bits of data and is followed by a ninth ACKNOWLEDGE BIT. This ACKNOWLEDGE BIT is provided by the recipient of the data, This is possible because devices only drive DATA low, the system (in the programming case the Programmer) provides a small pull–up current (1k Ohm equivalent) for the Data Pin.

The MESSAGE FORMAT consists of the bytes shown in the Message Bytes table below. The MESSAGE FORMAT is preceded by a start bit and ended by a stop bit.

The programmer provides all the bytes except for the data bytes when the device is being read. Note that each byte is individually acknowledged. This acknowledgment is provided by the MPA17C256 in all cases except for the data bytes in the read mode, in which case the acknowledge is provided by the programmer.

Bit Format

Data on the DATA pin may change only during CLOCK low times.

Figure 2–65. Message Bytes

DEVICE ADDRESS	1ST ADDRESS WORD	2ND ADDRESS WORD	DATA BYTE(S)

Figure 2–66. Message Format

START BIT	DEVICE ADDRESS	1ST ADDRESS WORD	2ND ADDRESS WORD	DATA BYTE(S)	STOP BIT

Start and Stop Bits

The START BIT is indicated by a high–to–low transition of DATA when CLOCK is high. Similarly, the STOP BIT is generated by a low–to–high transition of DATA when CLOCK is high, as shown below.

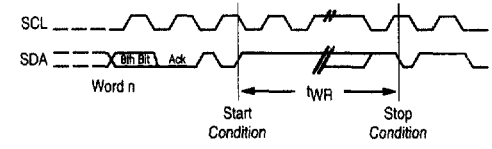

Figure 2–67. Start and Stop Bits

Acknowledge Bit

The ACKNOWLEDGE BIT is shown in the above figure. Note that the ACKNOWLEDGE BIT is provided by the device receiving the byte. The receiving device can accept the byte, by asserting a low value, on DATA or it can refuse the byte by asserting (not driving the signal) a 1 on DATA. All bytes must be terminated by either the ACKNOWLEDGE BIT or a STOP BIT.

Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on DATA for the DEVICE ADDRESS BYTE and the EEPROM ADDRESS BYTES. It is followed by the lesser significant bits until the eighth bit, the least significant bit is transmitted. This is followed by the acknowledge bit. However, for DATA BYTES (both writing and reading) the first bit transmitted is the least significant bit. This protocol is shown in the tables below.

Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device. The A2 bit is provided to allow 2 devices to share a common bus; when programming a single device, the A2 bit must be forced to a logic '0' or '1' level. It is recommended that this pin be connected to 0V using a 4.7K ohm resistor pulldown

Figure 2–68. Device Address Byte

MSB							LSB
1	0	1	0	A_2	1	1	R/$\overline{W}$
1ST	2ND	3RD	4TH	5TH	6TH	7TH	8TH

Where: R/$\overline{W}$ = 1 Read
= 0 Write
A2 = 1 if $\overline{CEO}$ pin is at VCC
= 0 if $\overline{CEO}$ pin is at GROUND

EEPROM Address

The EEPROM address consists of two bytes, each of which is followed by an acknowledge bit. These two bytes define a 15–bit address AE14 – AE0. The order in which each byte is clocked into the device is also indicated. AE14 is MSB for 17C256.

Figure 2–69.

MSB							LSB		MSB							LSB	
0	0/A_{E14}	0/A_{E13}	A_{E12}	A_{E11}	A_{E10}	A_{E9}	A_{E8}	Ack	A_{E7}	A_{E6}	A_{E5}	A_{E4}	A_{E3}	A_{E2}	A_{E1}	A_{E0}	Ack
1ST	2ND	3RD	4TH	5TH	6TH	7TH	8TH		1ST	2ND	3RD	4TH	5TH	6TH	7TH	8TH	

Data Byte

The organization of the Data Byte is shown below. Note that in this case, the data byte is clocked into the device LSB first and MSB last.

Writing

All writing takes place in pages. A page is 64–bytes long and the page boundaries are addresses where A5–A0 are all zero. Writing can start at any address within a page and the number of bytes written must be 64. The first byte is written at the transmitted address. The address is incremented in the device following the receipt of each data word received, Only the lower six bits of the address are incremented and if the address is incremented after the 64th byte in the page is sent, then the next byte to be written is the first byte of the page.

Figure 2–70.

LSB							MSB
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
1ST	2ND	3RD	4TH	5TH	6TH	7TH	8TH

```
A write action consists of
     a Start Bit
     a Device Address with R/W = 0
            An Acknowledge Bit From the device
     First Word of the Address
            An Acknowledge Bit From the device
     Second Word of the Address
            An Acknowledge Bit From the device
     One or more data bytes (sent to the device)
            Each followed by an Acknowledge Bit From the device
     a Stop Bit
```

WRITE POLLING: On receipt of the stop bit, the device enters an internally timed write cycle. While the device is busy with this write cycle it will not acknowledge any transfers. Thus the programmer can start the next page write by sending the Start Bit followed by the Device Address. If this is not acknowledged, then the programmer should abandon the transfer without asserting a stop bit. The programmer can then repeat this until an acknowledge is received. When this is received the write action can proceed, i.e., the next byte to be sent is the device address.

Reading

Read operations are initiated the same way as write operations with the exception that the R/$\overline{W}$ bit in the device address is set to one. There are three read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation. incremented by one. This address stays valid between operations as long as the chip

power is maintained and the device remains in 2–wire access mode. If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the 64th byte address in the page, the incremented address n + 1 would "roll over" to the first byte address on the next page.

Once the device address with the R/$\overline{W}$ select bit set is clocked in and acknowledged by the device the current address word is serially clocked out. The programmer does not acknowledge the read but does generate a following stop condition.

2

```
A current address read action consists of
     a Start Bit
     a Device Address with R/W = 1
            An Acknowledge Bit From the device
     a data byte from the device
     a Stop Bit from the programmer
```

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the device, the programmer must generate another start condition. The programmer now initiates a current address read by sending a device address with the R/$\overline{W}$ bit high. The device acknowledges the device address and serially clocks out the data word. The programmer does not acknowledge the read but does generate a following stop condition.

```
A random address read action consists of
     a Start Bit
     a Device Address with R/W = 0
            An Acknowledge Bit From the device
     First Word of the Address
            An Acknowledge Bit From the device
     Second Word of the Address
            An Acknowledge Bit From the device
     a Start Bit
     a Device Address with R/W = 1
            An Acknowledge Bit From the device
     a data byte from the device
     a stop bit from the programmer
```

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the programmer receives a data word, it responds with an acknowledge. As long as the device receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over". The sequential read operation is terminated when the programmer does not respond with an acknowledge but generates a stop condition.

Programming Pins

Eight pins are used to program the devices. These eight pins, and their mapping to the package pins are shown in the following table:

Table 2–33. Programming Pins

Pin	8–Pin Device	20–Pin Device
DATA	1	2
CLOCK	2	4
RESET/$\overline{OE}$	3	6
$\overline{CE}$	4	8
GROUND	5	10
A2 ($\overline{CEO}$)	6	14
$\overline{SER\_EN}$	7	17
V_{CC}	8	20

Programmer Functions

The programmer needs to perform the following functions:

1. Check the Manufacturers Code and the Device Code (Not necessary for In–System Programming)
2. Program the device
3. Verify the device
4. Set the Reset Polarity option

In the order given above. They are performed in the following manner.

Reading Manufacturers and Device Code

These two bytes are read from addresses 0 and 1, respectively, by performing a "read' as specified in this spec, with the following DC voltages set:

```
RESET/CE      =    0V
CE            =    11.5 ± 0.5V
A2 (CEO)      =    (Same as applied to A2 Pin,
                   usually 0V)
SER_EN        =    0V
```

The correct codes are (Note 1.)

```
Manufacturers Code  - Byte 0  1E
Device Code         - Byte 1  FF   17C128
                              7F   17C65
                              77   17C256
```

1. The Manufacturer's Code and Device Code are read using the same byte ordering specified in the beginning of this document: i.e., LSB first, MSB last.

Programming the Device

All the bytes in the device's 64–byte page must be written, The order is not important but it is suggested that the device be written sequentially from Byte 0. Writing is accomplished by using the DATA and CLOCK pins and setting the other programming pins as follows:

RESET/$\overline{CE}$	=	0V
$\overline{CE}$	=	0V
A2 ($\overline{CEO}$)	=	(Same as applied to A2 Pin, usually 0V)
$\overline{SER\_EN}$	=	0V

Verifying the Device

All bytes in the device must be read and compared to their intended values. Reading is done using the CLOCK and DATA pins with the other programming pins set to the same value as in programming:

RESET/$\overline{CE}$	=	0V
$\overline{CE}$	=	0V
A2 ($\overline{CEO}$)	=	(Same as applied to A2 Pin, usually 0V)
$\overline{SER\_EN}$	=	0V

MPA17C256 Setting the Polarity Option

Setting the Polarity Option Active High

Write a byte of data set to FF to address 3FFF, using the previously defined 2-wire write algorithm, with the other programming pins set to the following:

RESET/$\overline{CE}$	=	VCC ± 0.25V
$\overline{CE}$	=	VCC ± 0.25V
A2 ($\overline{CEO}$)	=	(Same as applied to A2 Pin, usually 0V)
$\overline{SER\_EN}$	=	0V

This will change RESET/$\overline{OE}$ pin functionality to $\overline{RESET}$/OE, i.e., active high OE and active low $\overline{RESET}$.

Setting the Polarity Option Active Low:

Write a byte of data set to FE to address 3FFF, using the previously defined 2-wire write algorithm, with the other programming pins set to the following:

RESET/$\overline{CE}$	=	0V
$\overline{CE}$	=	VCC ± 0.25V
A2 ($\overline{CEO}$)	=	(Same as applied to A2 Pin, usually 0V)
$\overline{SER\_EN}$	=	0V

This will change $\overline{RESET}$/OE functionality to RESET/$\overline{OE}$ i.e., active low OE and active high RESET (the default condition).

After RESET polarity has been modified the MPA17C256 device must be powered down before the modified RESET polarity takes effect.

Verifying the RESET/OE Polarity

If a programmed (master) device is to be used as the source for the data to be programmed info some new devices, then the programmer can read the data from the master The polarity of the RESET/$\overline{OE}$ must be known before this can be done successfully for the MPA17C256. Depending on the capabilities of the programming device, one of the following algorithms can be used to read the programmed polarity of the RESET/$\overline{OE}$ pin.

1. It the programmer is able to sense a tn-state condition:

Switch the power on with

RESET/$\overline{CE}$	=	0V
$\overline{CE}$	=	0V
A2 ($\overline{CEO}$)	=	Input to programmer (High Z)
$\overline{SER\_EN}$	=	VCC ± 0.25V
CLOCK	=	0
INPUT	=	Input to programmer

In this condition, if the SDA pin is 3-stated then he RESET/OE fuse is active high: it the SDA pin reads a "O"or a "1", then the RESET/OE fuse is active low.

2. If the programmer is NOT able to sense a 3-state condition:

Switch the power on with

RESET/$\overline{CE}$	=	VCC ± 0.25V
$\overline{CE}$	=	0V
A2 ($\overline{CEO}$)	=	Input to programmer (High Z)
$\overline{SER\_EN}$	=	VCC ± 0.25V
CLOCK	=	0
INPUT	=	Input to programmer

Hold this configuration for t_{WR} time after V_{CC} reaches nominal level. Then, set RESET/$\overline{OE}$ to low and pulse the clock 262,144 times for the MPA17C256, reading the data provided at each clock pulse. After the last clock has been issued $\overline{CEO}$ should drop from high to low. If it does so then the polarity is RESET/$\overline{OE}$ (active low). If $\overline{CEO}$ remains high, then the polarity is $\overline{RESET}$/OE (active high). In this latter case, none of the data read is reliable and it should be discarded. The procedure should be redone with RESET/$\overline{OE}$ = 0V on power up and switched to V_{CC} ± 0.25V before starting the clock. The data read is now good data.