

DALLAS

SEMICONDUCTOR

DS1230Y/AB

256K Nonvolatile SRAM

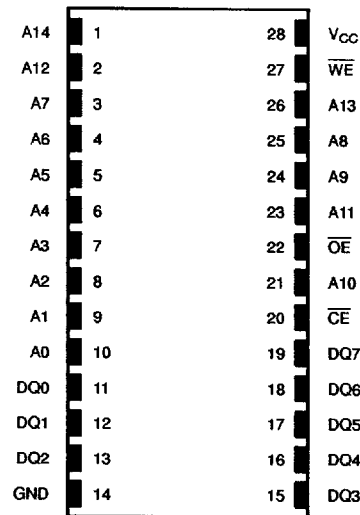
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- DIP-package devices directly replace 32K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full $\pm 10\%$ V_{CC} operating range (DS1230Y)
- Optional $\pm 5\%$ V_{CC} operating range (DS1230AB)
- Optional industrial temperature range of -40°C to $+85^{\circ}\text{C}$, designated IND
- JEDEC standard 28-pin DIP package
- Low Profile Module (LPM) package
 - Fits into standard 68-pin PLCC surface-mountable sockets
 - 250 mil package height

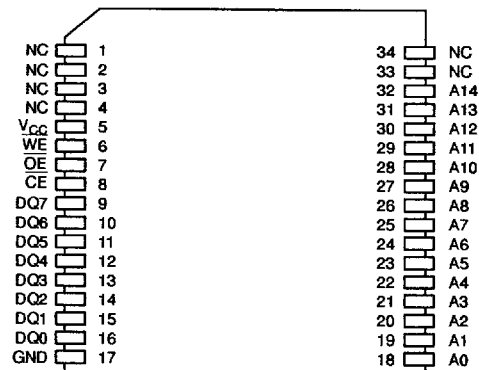
PIN DESCRIPTION

A0 - A14	- Address Inputs
DQ0 - DQ7	- Data In/Data Out
$\overline{\text{CE}}$	- Chip Enable
WE	- Write Enable
OE	- Output Enable
V_{CC}	- Power (+5V)
GND	- Ground

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34-PIN LOW PROFILE MODULE (LPM)

DESCRIPTION

The DS1230 256K Nonvolatile SRAMs are 262,144-bit, fully static, nonvolatile SRAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package DS1230 devices can be used in place of existing 32K x 8 static RAMs directly conforming to the popular byte-wide 28-pin DIP standard. The DIP devices also match the pinout of 28256 EEPROMs, allowing direct substitution while enhancing performance. DS1230 devices in the Low Profile Module package are specifically designed for surface-mount applications. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1230 devices execute a read cycle whenever \overline{WE} (Write Enable) is inactive (high) and \overline{CE} (Chip Enable) and \overline{OE} (Output Enable) are active (low). The unique address specified by the 15 address inputs ($A_0 - A_{14}$) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that \overline{CE} and \overline{OE} (Output Enable) access times are also satisfied. If \overline{OE} and \overline{CE} access times are not satisfied, then data access must be measured from the later occurring signal (\overline{CE} or \overline{OE}) and the limiting parameter is either t_{CO} for \overline{CE} or t_{OE} for \overline{OE} rather than address access.

WRITE MODE

The DS1230 devices execute a write cycle whenever the \overline{WE} and \overline{CE} signals are active (low) after address inputs are stable. The later occurring falling edge of \overline{CE} or

\overline{WE} will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of \overline{CE} or \overline{WE} . All address inputs must be kept valid throughout the write cycle. \overline{WE} must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The \overline{OE} control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled (\overline{CE} and \overline{OE} active) then \overline{WE} will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1230AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1230Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC} . Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1230AB and 4.5 volts for the DS1230Y.

FRESHNESS SEAL

Each DS1230 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To Ground

-0.3V to +7.0V

Operating Temperature

0°C to 70°C, -40°C to +85°C for IND parts

Storage Temperature

-40°C to +70°C, -40°C to +85°C for IND parts

Soldering Temperature

260°C For 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1230AB Power Supply Voltage	V _{CC}	4.75	5.0	5.25	V	
DS1230Y Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V	
Logic 1	V _{IH}	2.2		V _{CC}	V	
Logic 0	V _{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS(V_{CC}=5V ± 5% for DS1230AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1230Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I _{IL}	-1.0		+1.0	μA	
I/O Leakage Current CE ≥ V _{IH} ≤ V _{CC}	I _{IO}	-1.0		+1.0	μA	
Output Current @ 2.4V	I _{OH}	-1.0			mA	
Output Current @ 0.4V	I _{OL}	2.0			mA	
Standby Current CE = 2.2V	I _{CCS1}		5.0	10.0	mA	
Standby Current CE = V _{CC} -0.5V	I _{CCS2}		3.0	5.0	mA	
Operating Current	I _{CCO1}			85	mA	
Write Protection Voltage (DS1230AB)	V _{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1230Y)	V _{TP}	4.25	4.37	4.5	V	

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}		5	10	pF	
Input/Output Capacitance	C _{I/O}		5	10	pF	

($V_{CC}=5V \pm 5\%$ for DS1230AB)

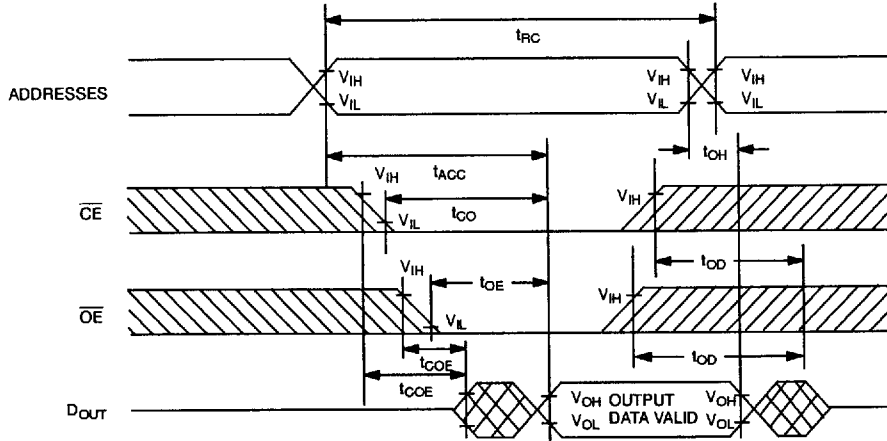
AC ELECTRICAL CHARACTERISTICS (t_A : See Note 10) ($V_{CC}=5V \pm 10\%$ for DS1230Y)

PARAMETER	SYMBOL	DS1230Y-70 DS1230AB-70		DS1230Y-85 DS1230AB-85		DS1230Y-100 DS1230AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		100		ns	
Access Time	t_{ACC}		70		85		100	ns	
OE to Output Valid	t_{OE}		35		45		50	ns	
CE to Output Valid	t_{CO}		70		85		100	ns	
OE or CE to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		ns	
Write Pulse Width	t_{WP}	55		65		75		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		5 15		ns	12 13
Output High Z from \overline{WE}	t_{ODW}		25		30		35	ns	5
Output Active from \overline{WE}	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		0 10		ns	12 13

AC ELECTRICAL CHARACTERISTICS (cont'd)

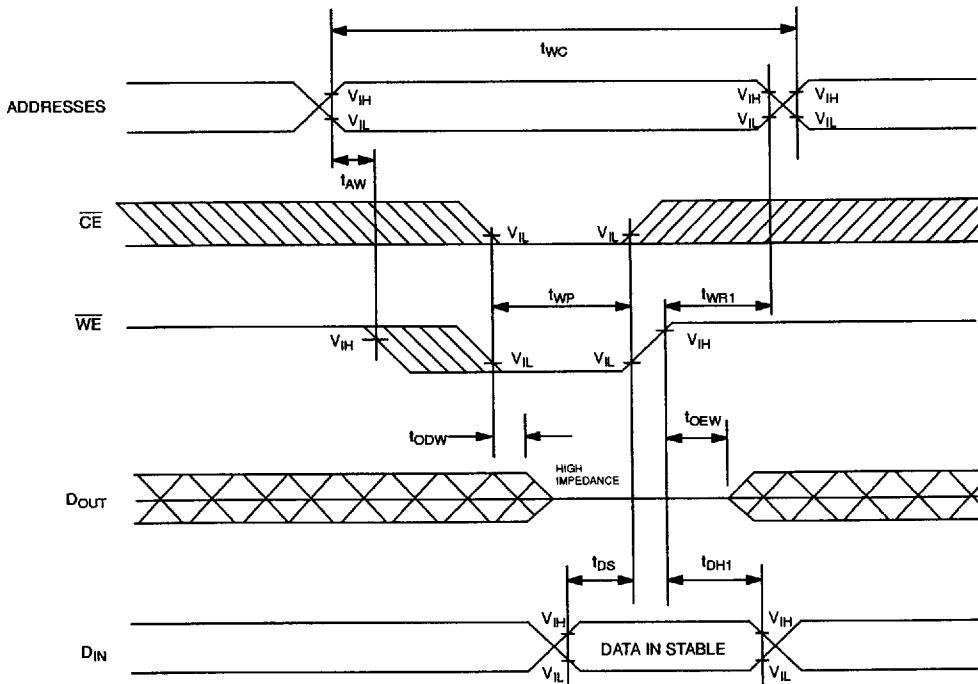
PARAMETER	SYMBOL	DS1230Y-120 DS1230AB-120		DS1230Y-150 DS1230AB-150		DS1230Y-200 DS1230AB-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
OE to Output Valid	t_{OE}		60		70		100	ns	
CE to Output Valid	t_{CO}		120		150		200	ns	
OE or CE to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		100		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		5 15		ns	12 13
Output High Z from \overline{WE}	t_{ODW}		35		35		35	ns	5
Output Active from \overline{WE}	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		0 10		ns	12 13

READ CYCLE



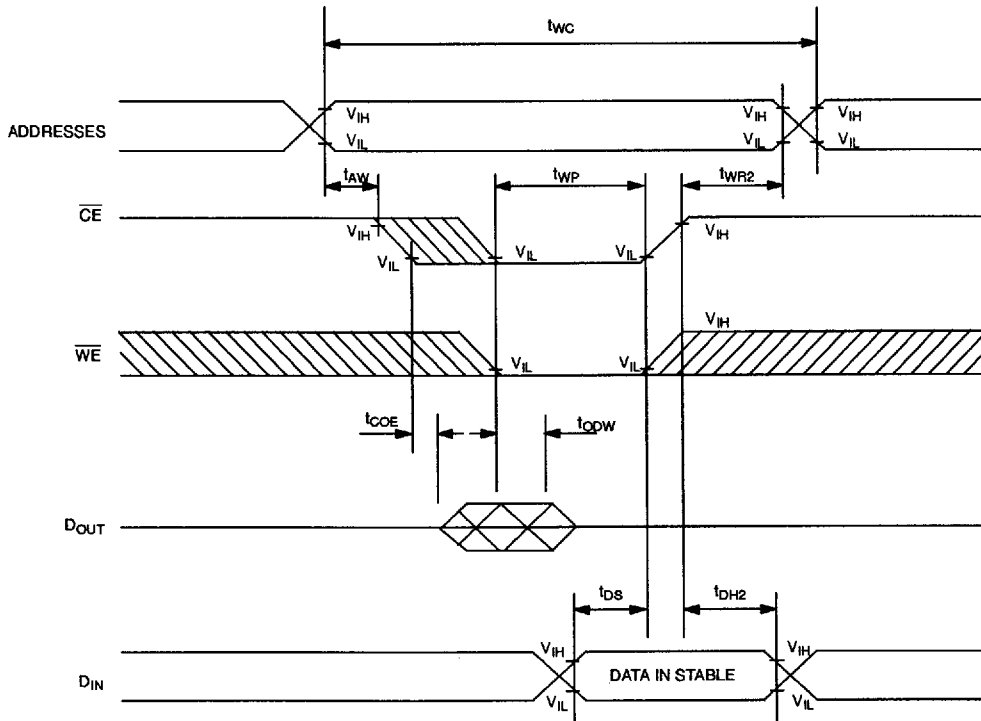
SEE NOTE 1

WRITE CYCLE 1



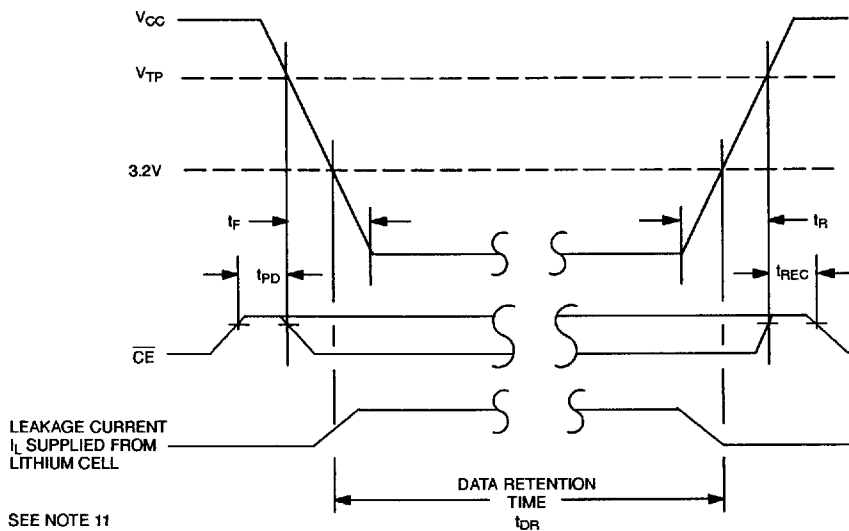
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE, at V _{IH} before Power-Down	t _{PD}	0			μs	11
V _{CC} slew from V _{TP} to 0V ($\overline{\text{CE}}$ at V _{IH})	t _F	300			μs	
V _{CC} slew from 0V to V _{TP} ($\overline{\text{CE}}$ at V _{IH})	t _R	300			μs	
CE, at V _{IH} after Power-Up	t _{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t _{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{\text{WE}}$ is high for a Read Cycle.
2. $\overline{\text{OE}} = \text{V}_{\text{IH}}$ or V_{IL} . If $\overline{\text{OE}} = \text{V}_{\text{IH}}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{\text{CE}}$ and $\overline{\text{WE}}$. t_{WP} is measured from the latter of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going low to the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{\text{CE}}$ low transition occurs simultaneously with or latter than the $\overline{\text{WE}}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{\text{CE}}$ high transition occurs prior to or simultaneously with the $\overline{\text{WE}}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{\text{WE}}$ is low or the $\overline{\text{WE}}$ low transition occurs prior to or simultaneously with the $\overline{\text{CE}}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1230Y has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{\text{WE}}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{\text{CE}}$ going high.
14. DS1230 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

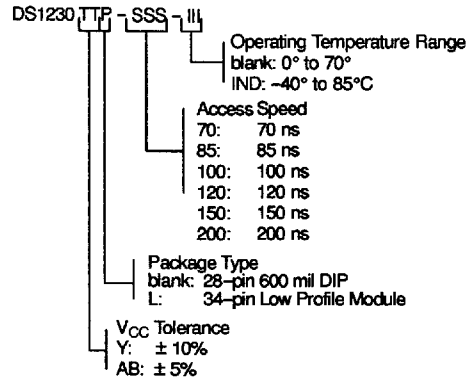
DC TEST CONDITIONS

Outputs Open
 Cycle = 200 ns for operating current
 All voltages are referenced to ground

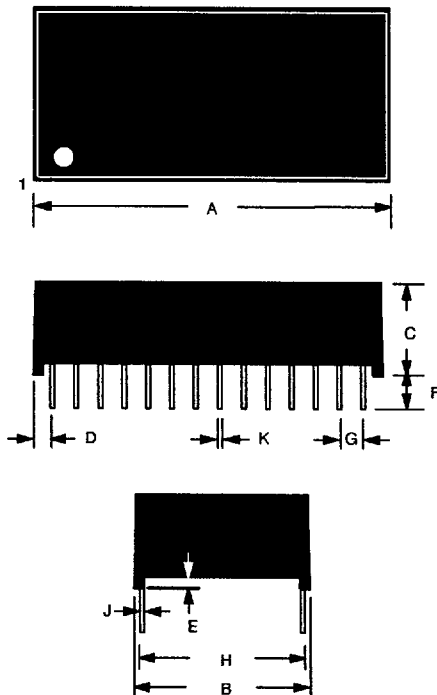
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
 Input Pulse Levels: 0 - 3.0V
 Timing Measurement Reference Levels
 Input: 1.5V
 Output: 1.5V
 Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

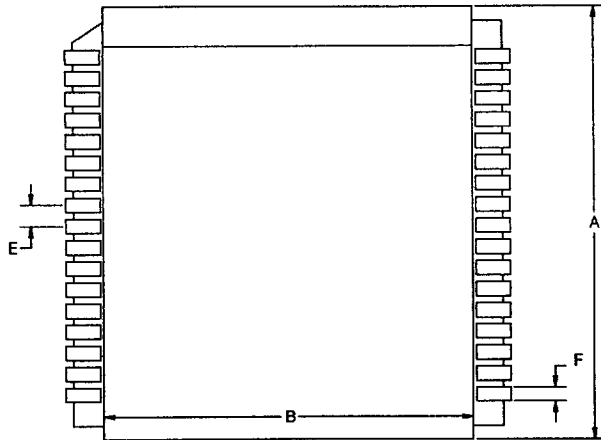


DS1230Y/AB NONVOLATILE SRAM, 28-PIN 740 MIL EXTENDED MODULE

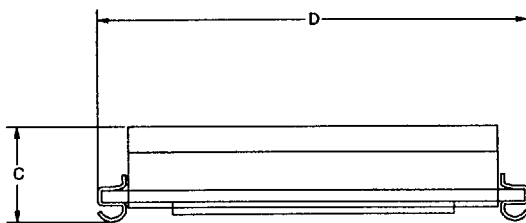


PKG	28-PIN	
	MIN	MAX
A IN.	1.480	1.500
MM	37.60	38.10
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1230YL/ABL 34-PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.050 BSC	
F	0.015	0.025



Suggested 68-pin PLCC surface mountable sockets with leads on two sides only are:

- | | |
|----------------------|--------------|
| McKenzie | 34P-SMT-3 |
| Harwin | HIS-40001-04 |
| Robinson Nugent | PLCC-34-SMT |
| Dallas Semiconductor | DS34PIN-PLC |

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.