54AC/74AC534 • 54ACT/74ACT534

Octal D-Type Flip-Flop With 3-State Outputs

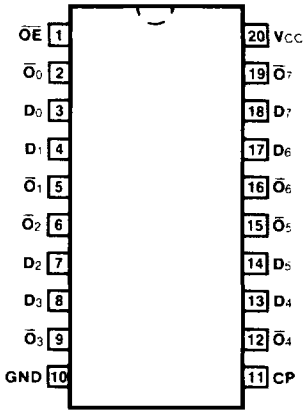
Description

The 'AC/'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'AC/'ACT534 is the same as the 'AC/'ACT374 except that the outputs are inverted.

- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT534 has TTL-Compatible Inputs**
- **Inverted Output Version of 'AC/'ACT374**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

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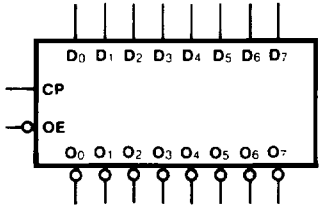
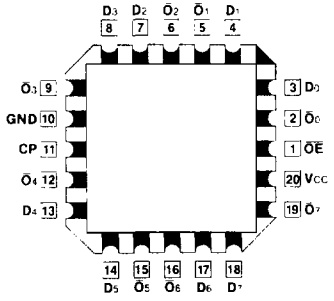
Logic Symbol





Pin Assignment for LCC

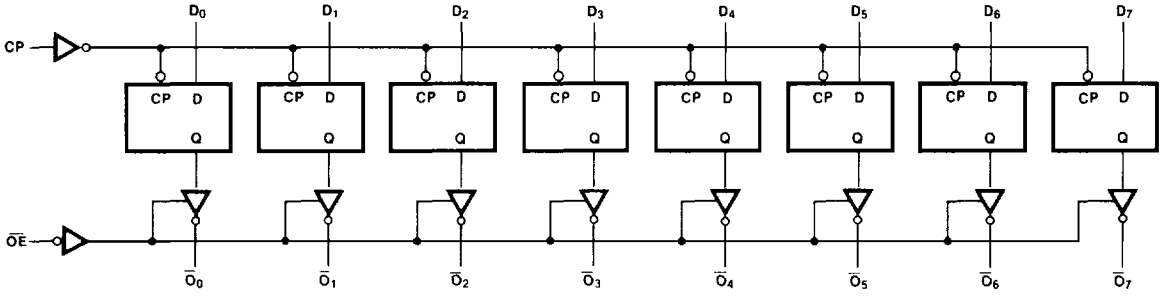
Pin Names

D_0 - D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	Complementary 3-State Outputs

Functional Description

The 'AC/'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT534)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		125 150						MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		10.0 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		9.5 6.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		8.5 6.5						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		8.5 6.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		9.0 7.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −0.5				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	3.5 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100						MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0		6.0						ns	3-6
t_{PZH}	Output Enable Time	5.0		5.5						ns	3-7
t_{PZL}	Output Enable Time	5.0		5.5						ns	3-8
t_{PHZ}	Output Disable Time	5.0		7.0						ns	3-7
t_{PLZ}	Output Disable Time	5.0		5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	5.0	2.5				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V