



## 18-Mbit (512K x 36/1M x 18) Flow-Through SRAM

### Features

- Supports 133-MHz bus operations
- 512K x 36/1M x 18 common I/O
- 2.5V core power supply ( $V_{DD}$ )
- 2.5V I/O supply ( $V_{DDQ}$ )
- Fast clock-to-output times  
— 6.5 ns (133-MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Available in JEDEC-standard lead-free 100-pin TQFP, lead-free and non-lead-free 119-ball BGA and 165-ball FBGA package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- “ZZ” Sleep Mode option

### Functional Description<sup>[1]</sup>

The CY7C1381DV25/CY7C1383DV25 are 2.5V, 512K x 36 and 1M x 18 Synchronous Flow-through SRAMs, respectively designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ( $\overline{CE}_1$ ), depth-expansion Chip Enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ <sup>[2]</sup>), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables ( $\overline{BW}_x$ , and BWE), and Global Write (GW). Asynchronous inputs include the Output Enable ( $\overline{OE}$ ) and the ZZ pin.

The CY7C1381DV25/CY7C1383DV25 allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe (ADSP) or the cache Controller Address Strobe (ADSC) inputs. Address advancement is controlled by the Address Advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

The CY7C1381DV25/CY7C1383DV25 operates from a +2.5V core power supply. All outputs also operate with a +2.5 supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

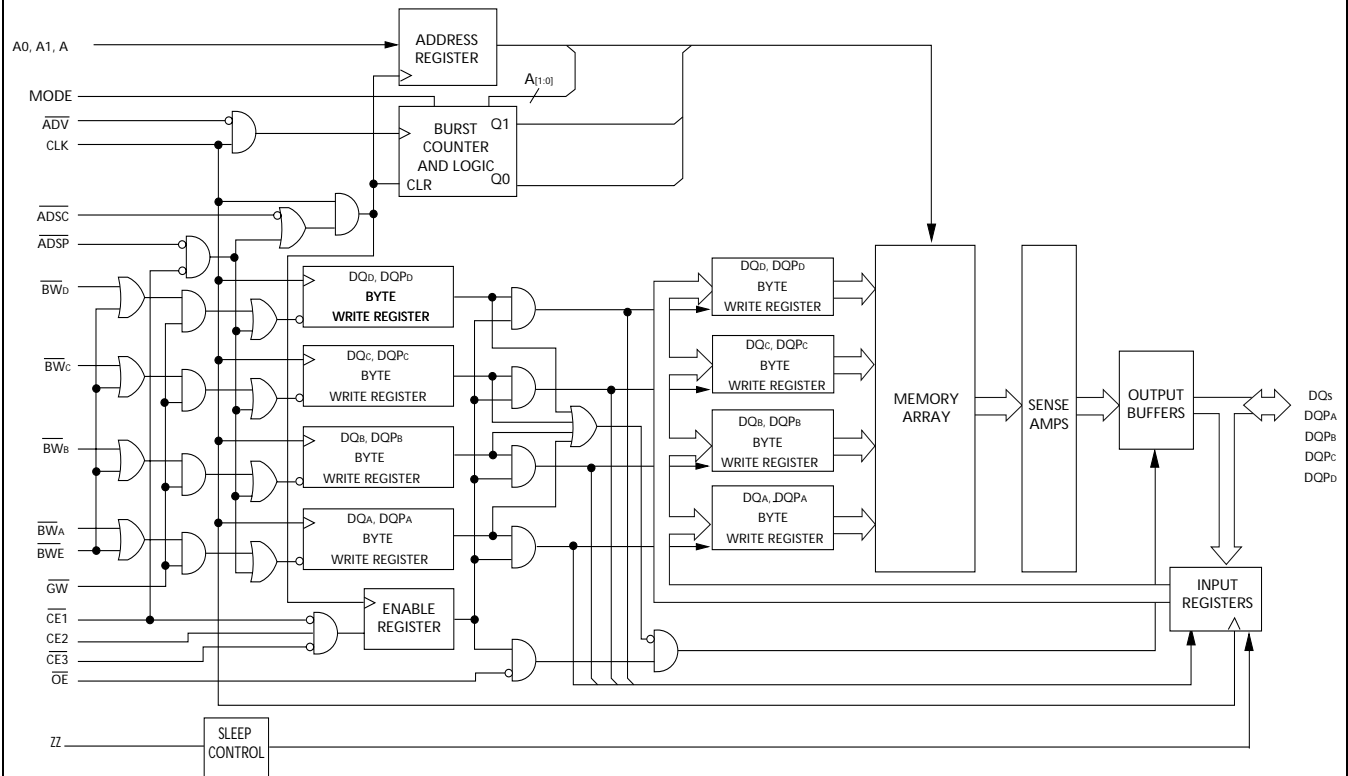
### Selection Guide

	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	210	175	mA
Maximum CMOS Standby Current	70	70	mA

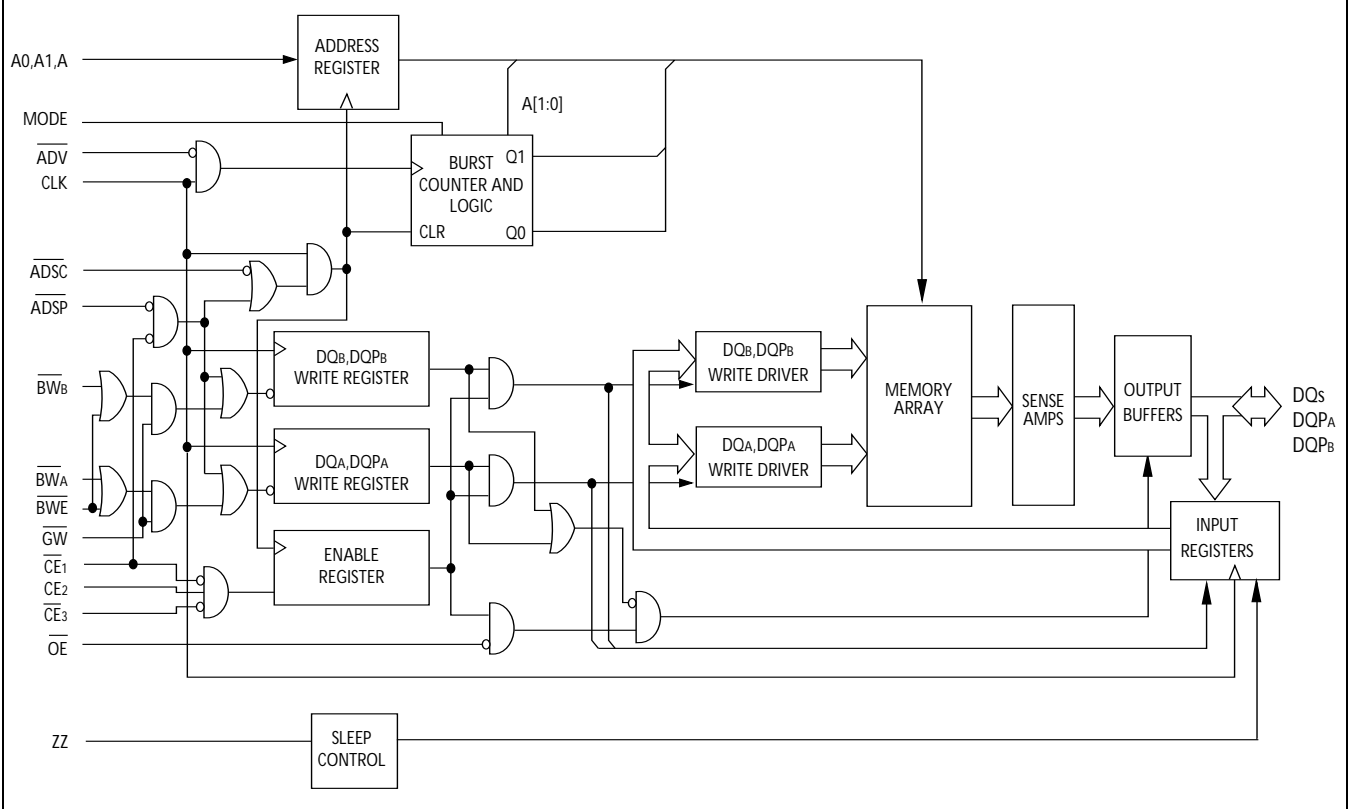
#### Notes:

1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).
2.  $\overline{CE}_3$ ,  $\overline{CE}_2$  are for TQFP and 165 FBGA package only. 119 BGA is offered only in 1 Chip Enable.

**Logic Block Diagram – CY7C1381DV25 (512K x 36)**

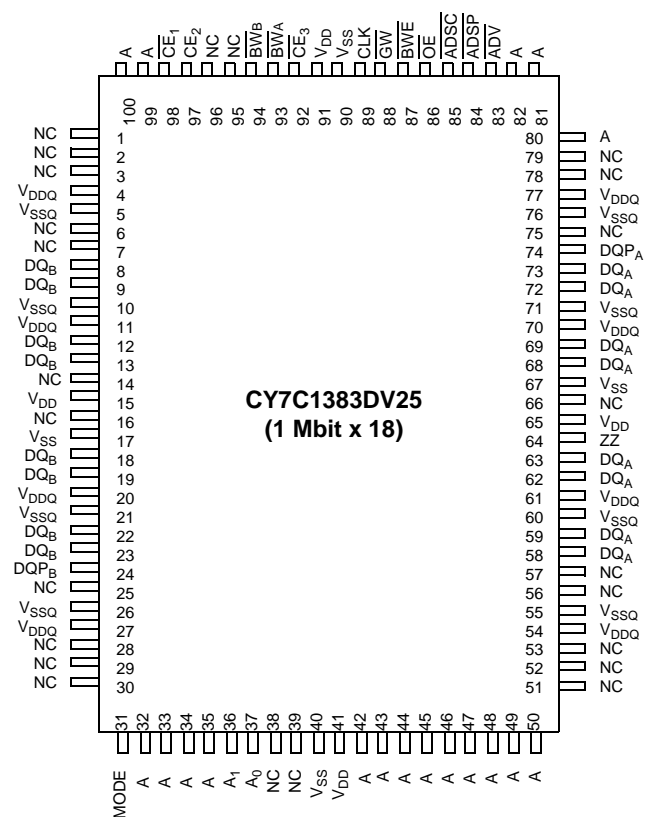
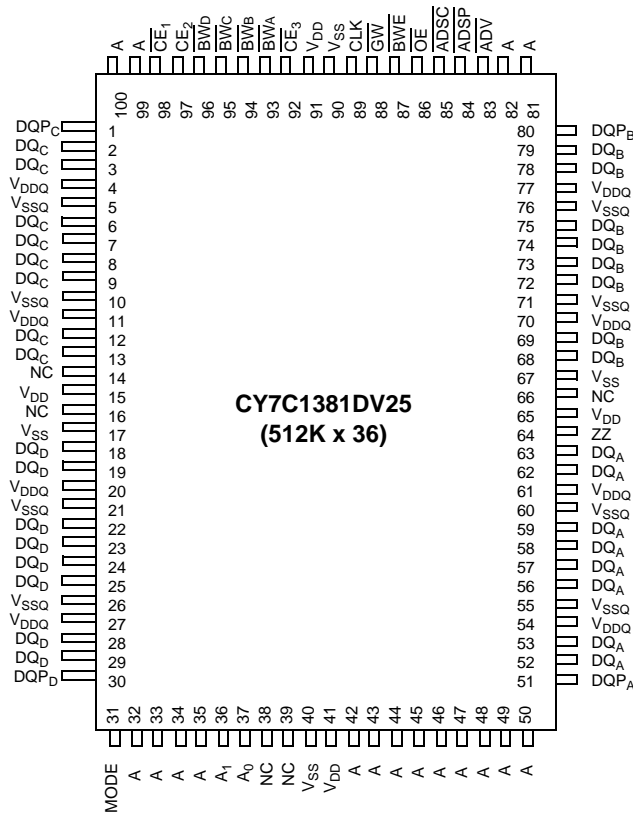


**Logic Block Diagram – CY7C1383DV25 (1M x 18)**



**Pin Configurations**

**100-pin TQFP Pinout (3 Chip Enable)**



**Pin Configurations** (continued)

**119-Ball BGA Pinout**  
**CY7C1381DV25 (512K x 36)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/288M	A	A	$\overline{\text{ADSC}}$	A	A	NC/576M
<b>C</b>	NC/144M	A	A	V <sub>DD</sub>	A	A	NC/1G
<b>D</b>	DQ <sub>C</sub>	DQP <sub>C</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	V <sub>DDQ</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>B</sub>	V <sub>DDQ</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	$\overline{\text{BW}}_C$	$\overline{\text{ADV}}$	$\overline{\text{BW}}_B$	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	$\overline{\text{BW}}_D$	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>P</b>	DQ <sub>D</sub>	DQP <sub>D</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	DQP <sub>A</sub>	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC	NC/72M	A	A	A	NC/36M	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**CY7C1383DV25 (1M x 18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/288M	A	A	$\overline{\text{ADSC}}$	A	A	NC/576M
<b>C</b>	NC/144M	A	A	V <sub>DD</sub>	A	A	NC/1G
<b>D</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>A</sub>	NC
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>B</sub>	$\overline{\text{BW}}_B$	$\overline{\text{ADV}}$	NC	NC	DQ <sub>A</sub>
<b>H</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>L</b>	DQ <sub>B</sub>	NC	NC	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>P</b>	NC	DQP <sub>B</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC/72M	A	A	NC/36M	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Pin Configurations** (continued)

**165-Ball FBGA Pinout(3 Chip Enable)**

**CY7C1381DV25 (512K x 36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
<b>B</b>	NC/144M	A	$CE_2$	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
<b>C</b>	DQP <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC/1G	DQP <sub>B</sub>
<b>D</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>N</b>	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>P</b>	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1383DV25 (1Mx 18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
<b>B</b>	NC/144M	A	$CE_2$	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
<b>C</b>	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC/1G	DQP <sub>A</sub>
<b>D</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>F</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>G</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>H</b>	V <sub>SS</sub>	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>K</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>M</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>N</b>	DQP <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
<b>P</b>	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

## Pin Definitions

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address Inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> <sup>[2]</sup> are sampled active. A <sub>[1:0]</sub> feed the 2-bit counter.
BW <sub>A</sub> , BW <sub>B</sub> , BW <sub>C</sub> , BW <sub>D</sub>	Input-Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with BWE to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input-Synchronous	<b>Global Write Enable Input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW <sub>[A:D]</sub> and BWE).
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
CE <sub>1</sub>	Input-Synchronous	<b>Chip Enable 1 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> <sup>[2]</sup> to select/deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH. CE <sub>1</sub> is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input-Synchronous	<b>Chip Enable 2 Input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>3</sub> <sup>[2]</sup> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded.
CE <sub>3</sub> <sup>[2]</sup>	Input-Synchronous	<b>Chip Enable 3 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>2</sub> to select/deselect the device. CE <sub>3</sub> is sampled only when a new external address is loaded.
OE	Input-Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when CE <sub>1</sub> is deasserted HIGH.
ADSC	Input-Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
BWE	Input-Synchronous	<b>Byte Write Enable Input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	<b>ZZ “Sleep” Input.</b> This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ <sub>s</sub>	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>x</sub> are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of OE.
DQP <sub>x</sub>	I/O-Synchronous	<b>Bidirectional Data Parity I/O Lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> . During write sequences, DQP <sub>x</sub> is controlled by BW <sub>x</sub> correspondingly.
MODE	Input-Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
V <sub>DD</sub>	Power Supply	<b>Power supply inputs to the core of the device.</b>
V <sub>DDQ</sub>	I/O Power Supply	<b>Power supply for the I/O circuitry.</b>

**Pin Definitions** (continued)

Name	I/O	Description
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b>
V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O circuitry.</b>
TDO	JTAG serial output Synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	<b>Serial data-in to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V <sub>DD</sub> through a pull-up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	<b>Serial data-in to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TCK	JTAG-Clock	<b>Clock input to the JTAG circuitry.</b> If the JTAG feature is not being utilized, this pin must be connected to V <sub>SS</sub> . This pin is not available on TQFP packages.
NC, NC/(36M, 72M, 144M, 288M, 576M, 1G)	-	<b>No Connects.</b> Not internally connected to the die. 36 Mbit, 72 Mbit, 144 Mbit, 288 Mbit, 576Mbit and 1Gbit are address expansion pins and are not internally connected to the die.
V <sub>SS</sub> /DNU	Ground/DNU	This pin can be connected to Ground or should be left floating.

**Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t<sub>CDV</sub>) is 6.5 ns (133-MHz device).

The CY7C1381DV25/CY7C1383DV25 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW<sub>X</sub>) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ , CE<sub>2</sub>,  $\overline{CE}_3$ <sup>[2]</sup>) and an asynchronous Output Enable (OE) provide for easy bank selection and output tri-state control. ADSP is ignored if CE<sub>1</sub> is HIGH.

**Single Read Accesses**

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub><sup>[2]</sup> are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the OE input is asserted LOW, the requested data will be

available at the data outputs a maximum to t<sub>CDV</sub> after clock rise. ADSP is ignored if CE<sub>1</sub> is HIGH.

**Single Write Accesses Initiated by ADSP**

This access is initiated when the following conditions are satisfied at clock rise: (1) CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub><sup>[2]</sup> are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and BWX) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device. Byte Writes are allowed. All I/Os are tri-stated during a Byte Write. Since this is a common I/O device, the asynchronous OE input signal must be deserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of OE.

**Single Write Accesses Initiated by ADSC**

This write access is initiated when the following conditions are satisfied at clock rise: (1) CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub><sup>[2]</sup> are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deserted HIGH, and (4) the write input signals (GW, BWE, and BWX) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ<sub>X</sub> will be written into the specified address location. Byte writes are allowed. All I/Os are tri-stated when a write is detected, even a Byte Write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of OE.



## Burst Sequences

The CY7C1381DV25/CY7C1383DV25 provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by  $A_{[1:0]}$ , and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a linear burst sequence.

## Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode.  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3^{[2]}$ , ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

## ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		80	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
$t_{ZZI}$	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

## Truth Table<sup>[3, 4, 5, 6, 7]</sup>

Cycle Description	Address Used	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power-down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D

## Interleaved Burst Address Table (MODE = Floating or $V_{DD}$ )

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

## Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10



**Truth Table**<sup>[3, 4, 5, 6, 7]</sup>

Cycle Description	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

**Partial Truth Table for Read/Write**<sup>[3, 8]</sup>

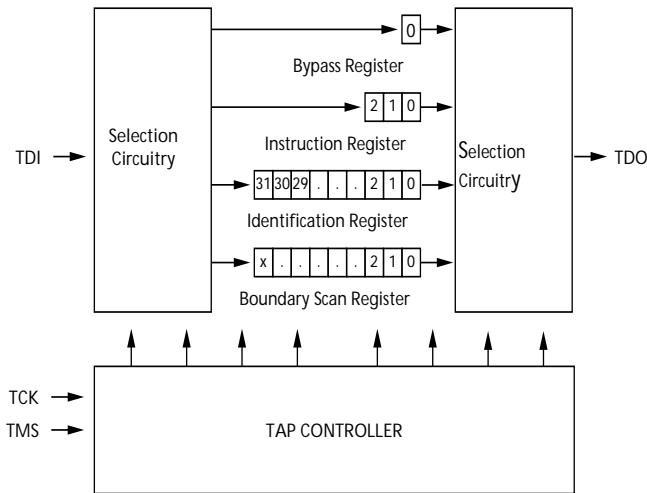
Function (CY7C1381DV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ <sub>A</sub> , DQP <sub>A</sub> )	H	L	H	H	H	L
Write Byte B (DQ <sub>B</sub> , DQP <sub>B</sub> )	H	L	H	H	L	H
Write Bytes A, B (DQ <sub>A</sub> , DQ <sub>B</sub> , DQP <sub>A</sub> , DQP <sub>B</sub> )	H	L	H	H	L	L
Write Byte C (DQ <sub>C</sub> , DQP <sub>C</sub> )	H	L	H	L	H	H
Write Bytes C, A (DQ <sub>C</sub> , DQ <sub>A</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	H	L	H	L
Write Bytes C, B (DQ <sub>C</sub> , DQ <sub>B</sub> , DQP <sub>C</sub> , DQP <sub>B</sub> )	H	L	H	L	L	H
Write Bytes C, B, A (DQ <sub>C</sub> , DQ <sub>B</sub> , DQ <sub>A</sub> , DQP <sub>C</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	H	L	L	L
Write Byte D (DQ <sub>D</sub> , DQP <sub>D</sub> )	H	L	L	H	H	H
Write Bytes D, A (DQ <sub>D</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>A</sub> )	H	L	L	H	H	L
Write Bytes D, B (DQ <sub>D</sub> , DQ <sub>B</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	H	L	H
Write Bytes D, B, A (DQ <sub>D</sub> , DQ <sub>B</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	H	L	L
Write Bytes D, B (DQ <sub>D</sub> , DQ <sub>B</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	L	H	H
Write Bytes D, B, A (DQ <sub>D</sub> , DQ <sub>C</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	L	L	H	L
Write Bytes D, C, A (DQ <sub>D</sub> , DQ <sub>B</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

**Notes:**

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$  when any one or more Byte Write Enable signals and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all Byte write enable signals,  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when ADSP is asserted, regardless of the state of GW, BWE, or BW<sub>x</sub>. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, OE must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. OE is a don't care for the remainder of the write cycle.
- OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when OE is inactive or when the device is deselected, and all data bits behave as output when OE is active (LOW).
- Table only lists a partial listing of the byte write combinations. Any Combination of BW<sub>x</sub> is valid. Appropriate write will be done based on which byte write is active.



## TAP Controller Block Diagram



### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

#### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

#### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR

state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

#### Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### TAP Instruction Set

#### Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

#### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

#### SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

#### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

**BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass

register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

**EXTEST Output Bus Tri-State**

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

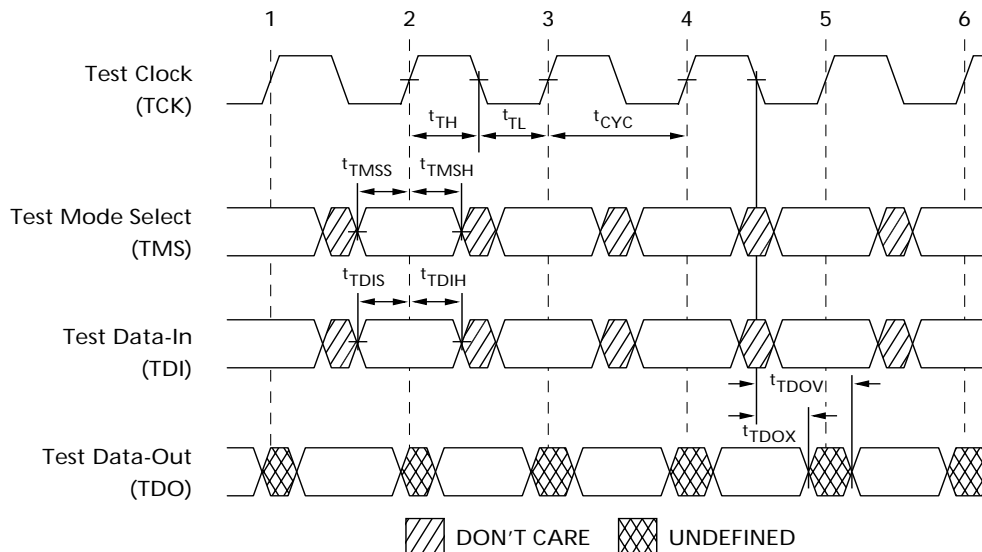
The boundary scan register has a special bit located at bit #85 (for 119-BGA package) or bit #89 (for 165-fBGA package). When this scan cell, called the “extest output bus tri-state,” is latched into the preload register during the “Update-DR” state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR,” the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

**Reserved**

These instructions are not implemented but are reserved for future use. Do not use these instructions.

**TAP Timing**



**TAP AC Switching Characteristics** Over the Operating Range<sup>[9, 10]</sup>

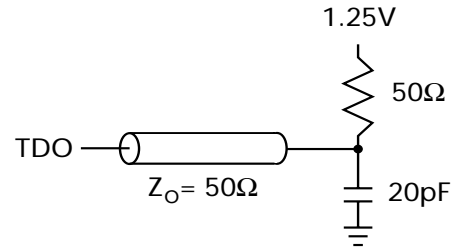
Parameter	Description	Min.	Max.	Unit
<b>Clock</b>				
t <sub>TCYC</sub>	TCK Clock Cycle Time	50		ns
t <sub>TF</sub>	TCK Clock Frequency		20	MHz
t <sub>TH</sub>	TCK Clock HIGH time	20		ns
t <sub>TL</sub>	TCK Clock LOW time	20		ns
<b>Output Times</b>				
t <sub>TDOV</sub>	TCK Clock LOW to TDO Valid		10	ns
t <sub>TDOX</sub>	TCK Clock LOW to TDO Invalid	0		ns
<b>Set-up Times</b>				
t <sub>TMSS</sub>	TMS Set-up to TCK Clock Rise	5		ns
t <sub>TDIS</sub>	TDI Set-up to TCK Clock Rise	5		ns
t <sub>CS</sub>	Capture Set-up to TCK Rise	5		ns
<b>Hold Times</b>				
t <sub>TMSH</sub>	TMS Hold after TCK Clock Rise	5		ns
t <sub>TDIH</sub>	TDI Hold after Clock Rise	5		ns
t <sub>CH</sub>	Capture Hold after Clock Rise	5		ns

**Notes:**

9. t<sub>CS</sub> and t<sub>CH</sub> refer to the set-up and hold time requirements of latching data from the boundary scan register.  
 10. Test conditions are specified using the load in TAP AC test Conditions. t<sub>R</sub>/t<sub>F</sub> = 1 ns.

**2.5V TAP AC Test Conditions**

Input pulse levels .....  $V_{SS}$  to 2.5V  
 Input rise and fall time ..... 1 ns  
 Input timing reference levels ..... 1.25V  
 Output reference levels ..... 1.25V  
 Test load termination supply voltage ..... 1.25V

**2.5V TAP AC Output Load Equivalent**

**TAP DC Electrical Characteristics And Operating Conditions**

( $0^{\circ}\text{C} < \text{TA} < +70^{\circ}\text{C}$ ;  $V_{DD} = 2.5\text{V} \pm 0.125\text{V}$  unless otherwise noted)<sup>[11]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{OH1}$	Output HIGH Voltage	$I_{OH} = -1.0\text{ mA}$ , $V_{DDQ} = 2.5\text{V}$	2.0		V
$V_{OH2}$	Output HIGH Voltage	$I_{OH} = -100\ \mu\text{A}$ , $V_{DDQ} = 2.5\text{V}$	2.1		V
$V_{OL1}$	Output LOW Voltage	$I_{OL} = 8.0\text{ mA}$ , $V_{DDQ} = 2.5\text{V}$		0.4	V
$V_{OL2}$	Output LOW Voltage	$I_{OL} = 100\ \mu\text{A}$ , $V_{DDQ} = 2.5\text{V}$		0.2	V
$V_{IH}$	Input HIGH Voltage	$V_{DDQ} = 2.5\text{V}$	1.7	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage	$V_{DDQ} = 2.5\text{V}$	-0.3	0.7	V
$I_X$	Input Load Current	$\text{GND} \leq V_{IN} \leq V_{DDQ}$	-5	5	$\mu\text{A}$

**Identification Register Definitions**

Instruction Field	CY7C1381DV25 (512K x 36)	CY7C1383DV25 (1 Mbit x 18)	Description
Revision Number (31:29)	000	000	Describes the version number
Device Depth (28:24)	01011	01011	Reserved for internal use
Device Width (23:18) 119-BGA	101001	101001	Defines memory type and architecture
Device Width (23:18) 165-FBGA	000001	000001	Defines memory type and architecture
Cypress Device ID (17:12)	100101	010101	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register

**Scan Register Sizes**

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction Bypass	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	85	85
Boundary Scan Order (165-ball FBGA package)	89	89

**Note:**

11. All voltages referenced to  $V_{SS}$  (GND).

**Identification Codes**

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

**119-Ball BGA Boundary Scan Order** <sup>[12, 13]</sup>

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	H4	23	F6	45	G4	67	L1
2	T4	24	E7	46	A4	68	M2
3	T5	25	D7	47	G3	69	N1
4	T6	26	H7	48	C3	70	P1
5	R5	27	G6	49	B2	71	K1
6	L5	28	E6	50	B3	72	L2
7	R6	29	D6	51	A3	73	N2
8	U6	30	C7	52	C2	74	P2
9	R7	31	B7	53	A2	75	R3
10	T7	32	C6	54	B1	76	T1
11	P6	33	A6	55	C1	77	R1
12	N7	34	C5	56	D2	78	T2
13	M6	35	B5	57	E1	79	L3
14	L7	36	G5	58	F2	80	R2
15	K6	37	B6	59	G1	81	T3
16	P7	38	D4	60	H2	82	L4
17	N6	39	B4	61	D1	83	N4
18	L6	40	F4	62	E2	84	P4
19	K7	41	M4	63	G2	85	Internal
20	J5	42	A5	64	H1		
21	H6	43	K4	65	J3		
22	G7	44	E4	66	2K		

**Notes:**

- 12. Balls which are NC (No Connect) are pre-set LOW.
- 13. Bit# 85 is pre-set HIGH.



**165-Ball BGA Boundary Scan Order** [12, 14]

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	N6	31	D10	61	G1
2	N7	32	C11	62	D2
3	N10	33	A11	63	E2
4	P11	34	B11	64	F2
5	P8	35	A10	65	G2
6	R8	36	B10	66	H1
7	R9	37	A9	67	H3
8	P9	38	B9	68	J1
9	P10	39	C10	69	K1
10	R10	40	A8	70	L1
11	R11	41	B8	71	M1
12	H11	42	A7	72	J2
13	N11	43	B7	73	K2
14	M11	44	B6	74	L2
15	L11	45	A6	75	M2
16	K11	46	B5	76	N1
17	J11	47	A5	77	N2
18	M10	48	A4	78	P1
19	L10	49	B4	79	R1
20	K10	50	B3	80	R2
21	J10	51	A3	81	P3
22	H9	52	A2	82	R3
23	H10	53	B2	83	P2
24	G11	54	C2	84	R4
25	F11	55	B1	85	P4
26	E11	56	A1	86	N5
27	D11	57	C1	87	P6
28	G10	58	D1	88	R6
29	F10	59	E1	89	Internal
30	E10	60	F1		

**Note:**  
 14. Bit# 89 is pre-set HIGH.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V<sub>DD</sub> Relative to GND..... -0.3V to +3.6V
- Supply Voltage on V<sub>DDQ</sub> Relative to GND ..... -0.3V to +V<sub>DD</sub>
- DC Voltage Applied to Outputs in Tri-State..... -0.5V to V<sub>DDQ</sub> + 0.5V

- DC Input Voltage ..... -0.5V to V<sub>DD</sub> + 0.5V
- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	2.5V ± 5%	2.5V – 5% to V <sub>DD</sub>
Industrial	-40°C to +85°C		

**Electrical Characteristics** Over the Operating Range <sup>[15, 16]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage		2.375	2.625	V
V <sub>DDQ</sub>	I/O Supply Voltage	for 2.5V I/O	2.375	V <sub>DD</sub>	V
V <sub>OH</sub>	Output HIGH Voltage	for 2.5V I/O, I <sub>OH</sub> = -1.0 mA	2.0		V
V <sub>OL</sub>	Output LOW Voltage	for 2.5V I/O, I <sub>OL</sub> = 1.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>[15]</sup>	for 2.5V I/O	1.7	V <sub>DD</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[15]</sup>	for 2.5V I/O	-0.3	0.7	V
I <sub>X</sub>	Input Leakage Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	µA
	Input Current of MODE	Input = V <sub>SS</sub>	-30		µA
		Input = V <sub>DD</sub>		5	µA
	Input Current of ZZ	Input = V <sub>SS</sub>	-5		µA
Input = V <sub>DD</sub>			30	µA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DD</sub> , Output Disabled	-5	5	µA
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz	210	mA
			10-ns cycle, 100 MHz	175	mA
I <sub>SB1</sub>	Automatic CE Power-down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> , inputs switching	7.5-ns cycle, 133 MHz	140	mA
			10-ns cycle, 100 MHz	120	
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0, inputs static		70	mA
I <sub>SB3</sub>	Automatic CE Power-down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub> , inputs switching	7.5-ns cycle, 133 MHz	130	mA
			10-ns cycle, 100 MHz	110	mA
I <sub>SB4</sub>	Automatic CE Power-down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0, inputs static		80	mA

**Notes:**

- 15. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL</sub>(AC) > -2V (Pulse width less than t<sub>CYC</sub>/2).
- 16. T<sub>Power-up</sub>: Assumes a linear ramp from 0V to V<sub>DD</sub>(min.) within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

**Capacitance<sup>[17]</sup>**

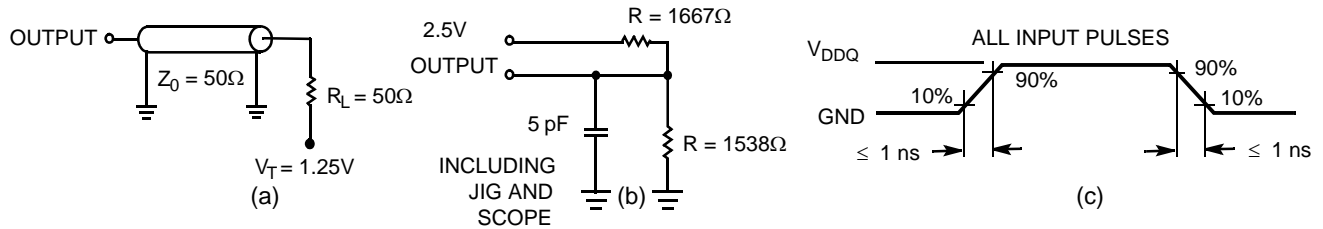
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> /V <sub>DDQ</sub> = 2.5V	5	8	9	pF
C <sub>CLK</sub>	Clock Input Capacitance		5	8	9	pF
C <sub>I/O</sub>	Input/Output Capacitance		5	8	9	pF

**Thermal Resistance<sup>[17]</sup>**

Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	28.66	23.8	20.7	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		4.08	6.2	4.0	°C/W

**AC Test Loads and Waveforms**

**2.5V I/O Test Load**



**Note:**

17. Tested initially and after any design or process change that may affect these parameters.

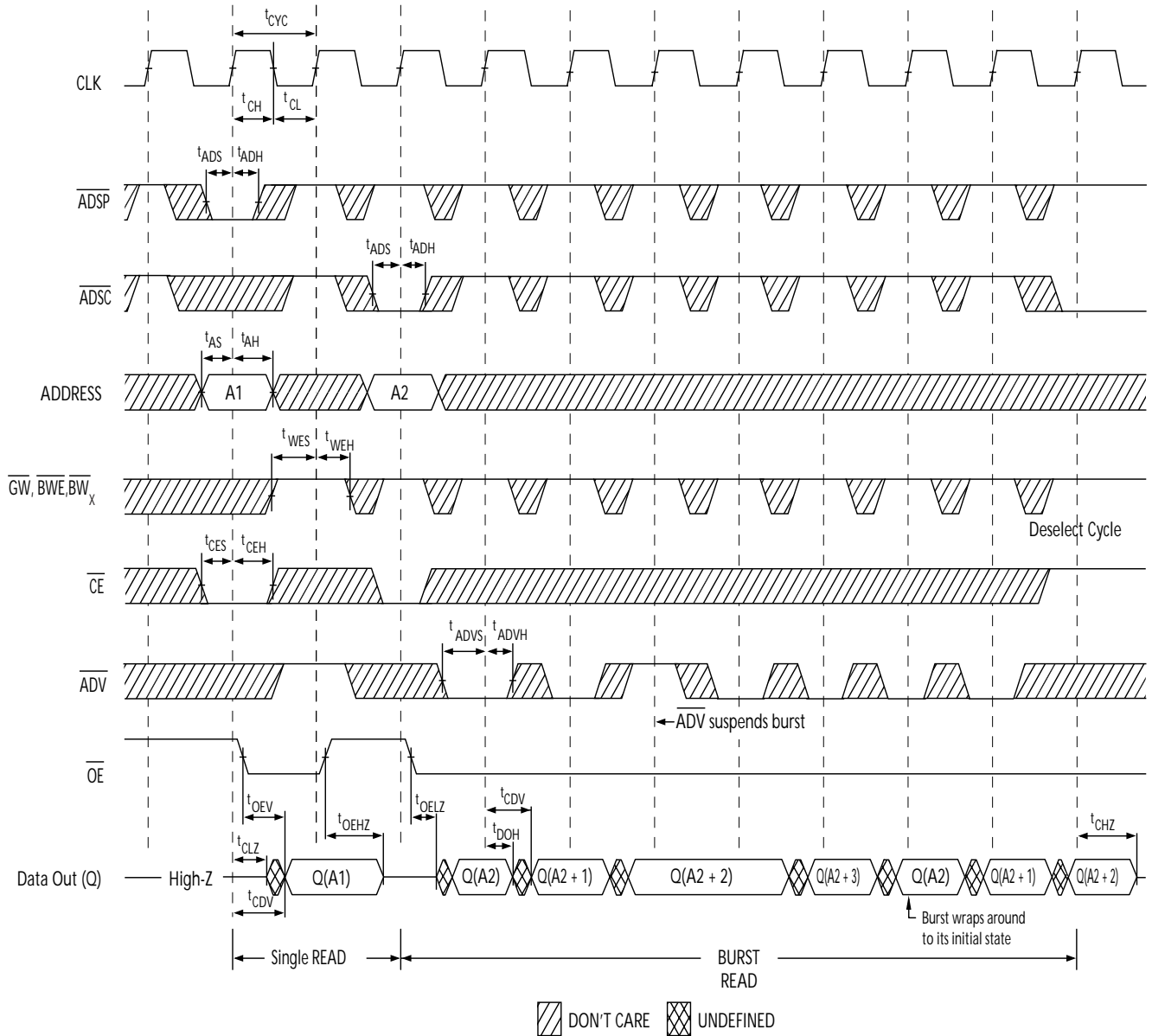
**Switching Characteristics** Over the Operating Range [22, 23]

Parameter	Description	133 MHz		100 MHz		Unit
		Min.	Max.	Min.	Max.	
t <sub>POWER</sub>	V <sub>DD</sub> (Typical) to the first Access <sup>[18]</sup>	1		1		ms
<b>Clock</b>						
t <sub>CYC</sub>	Clock Cycle Time	7.5		10		ns
t <sub>CH</sub>	Clock HIGH	2.1		2.5		ns
t <sub>CL</sub>	Clock LOW	2.1		2.5		ns
<b>Output Times</b>						
t <sub>CDV</sub>	Data Output Valid After CLK Rise		6.5		8.5	ns
t <sub>DOH</sub>	Data Output Hold After CLK Rise	2.0		2.0		ns
t <sub>CLZ</sub>	Clock to Low-Z <sup>[19, 20, 21]</sup>	2.0		2.0		ns
t <sub>CHZ</sub>	Clock to High-Z <sup>[19, 20, 21]</sup>	0	4.0	0	5.0	ns
t <sub>OEV</sub>	OE LOW to Output Valid		3.2		3.8	ns
t <sub>OELZ</sub>	OE LOW to Output Low-Z <sup>[19, 20, 21]</sup>	0		0		ns
t <sub>OEHZ</sub>	OE HIGH to Output High-Z <sup>[19, 20, 21]</sup>		4.0		5.0	ns
<b>Set-up Times</b>						
t <sub>AS</sub>	Address Set-up Before CLK Rise	1.5		1.5		ns
t <sub>ADS</sub>	ADSP, ADSC Set-up Before CLK Rise	1.5		1.5		ns
t <sub>ADVS</sub>	ADV Set-up Before CLK Rise	1.5		1.5		ns
t <sub>WES</sub>	GW, BWE, BW <sub>[A:D]</sub> Set-up Before CLK Rise	1.5		1.5		ns
t <sub>DS</sub>	Data Input Set-up Before CLK Rise	1.5		1.5		ns
t <sub>CES</sub>	Chip Enable Set-up	1.5		1.5		ns
<b>Hold Times</b>						
t <sub>AH</sub>	Address Hold After CLK Rise	0.5		0.5		ns
t <sub>ADH</sub>	ADSP, ADSC Hold After CLK Rise	0.5		0.5		ns
t <sub>WEH</sub>	GW, BWE, BW <sub>[A:D]</sub> Hold After CLK Rise	0.5		0.5		ns
t <sub>ADVH</sub>	ADV Hold After CLK Rise	0.5		0.5		ns
t <sub>DH</sub>	Data Input Hold After CLK Rise	0.5		0.5		ns
t <sub>CEH</sub>	Chip Enable Hold After CLK Rise	0.5		0.5		ns

**Notes:**

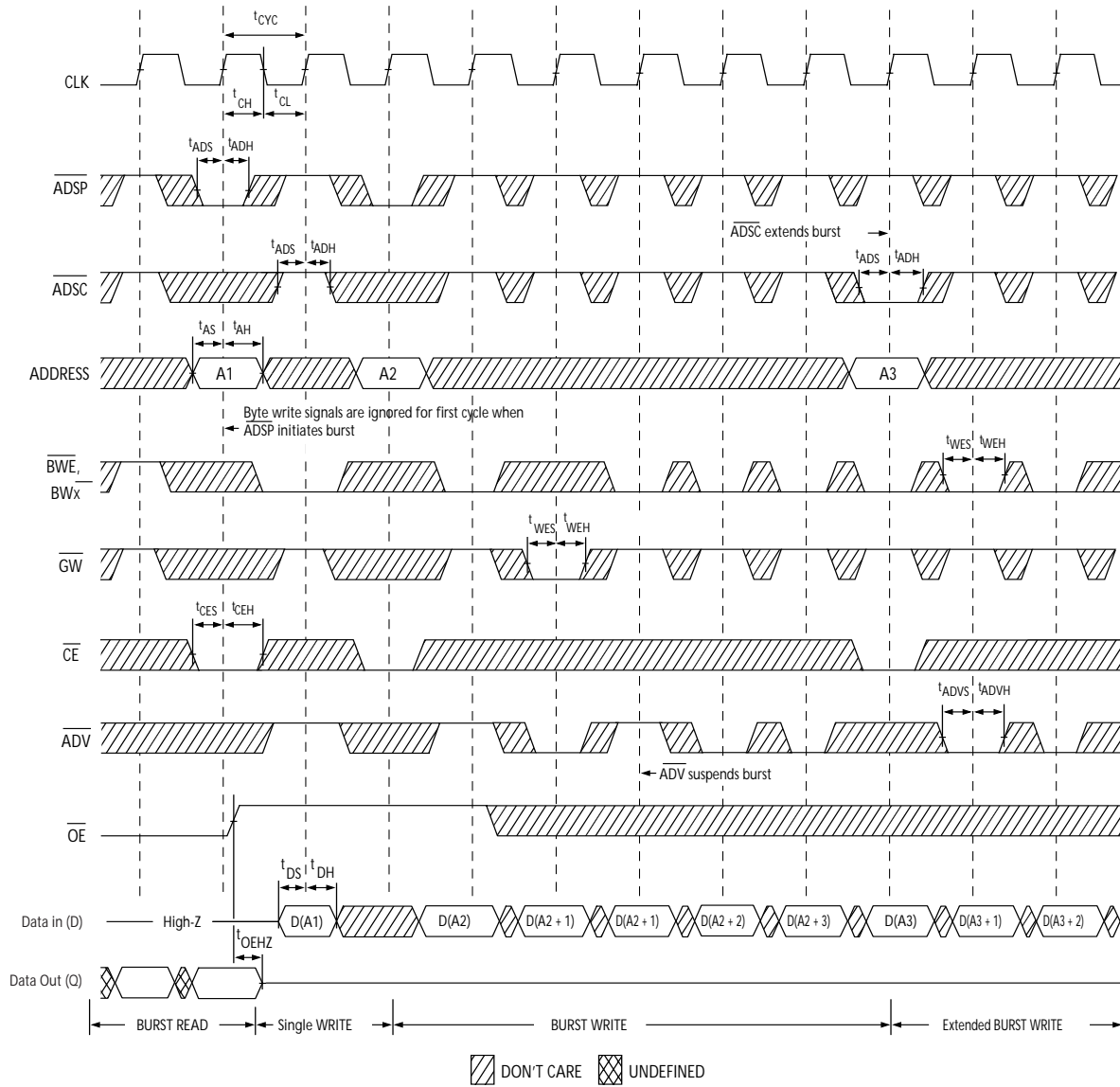
18. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD</sub>(minimum) initially, before a read or write operation can be initiated.
19. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEHZ</sub> are specified with AC Test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
20. At any given voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.
22. Timing reference level is 1.25V.
23. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

**Timing Diagrams**  
**Read Cycle Timing<sup>[24]</sup>**



**Note:**  
 24. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

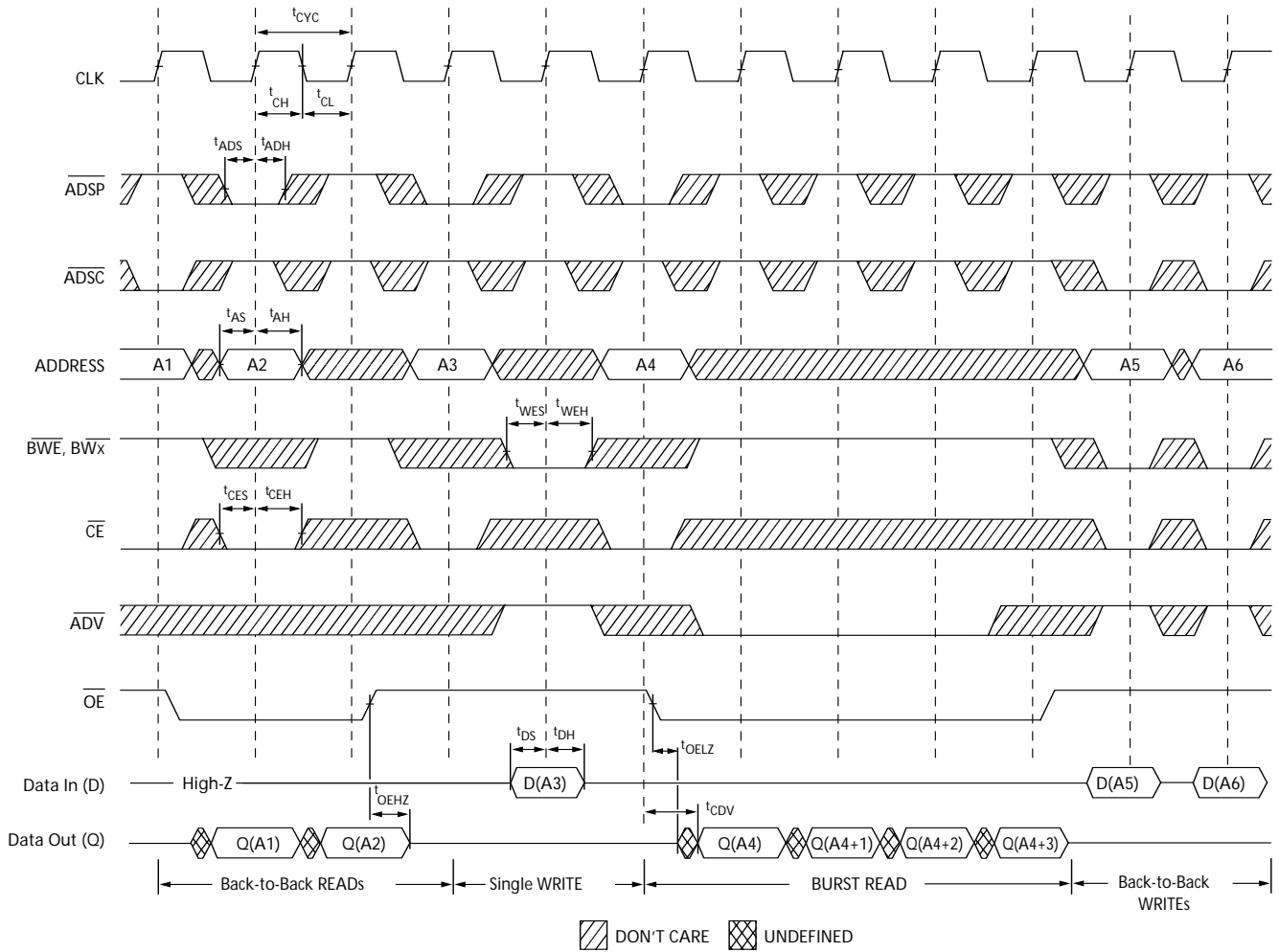
**Timing Diagrams (continued)**  
**Write Cycle Timing<sup>[24, 25]</sup>**



**Note:**  
25. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BW}_x$  LOW.

**Timing Diagrams (continued)**

**Read/Write Cycle Timing**<sup>[24, 26, 27]</sup>



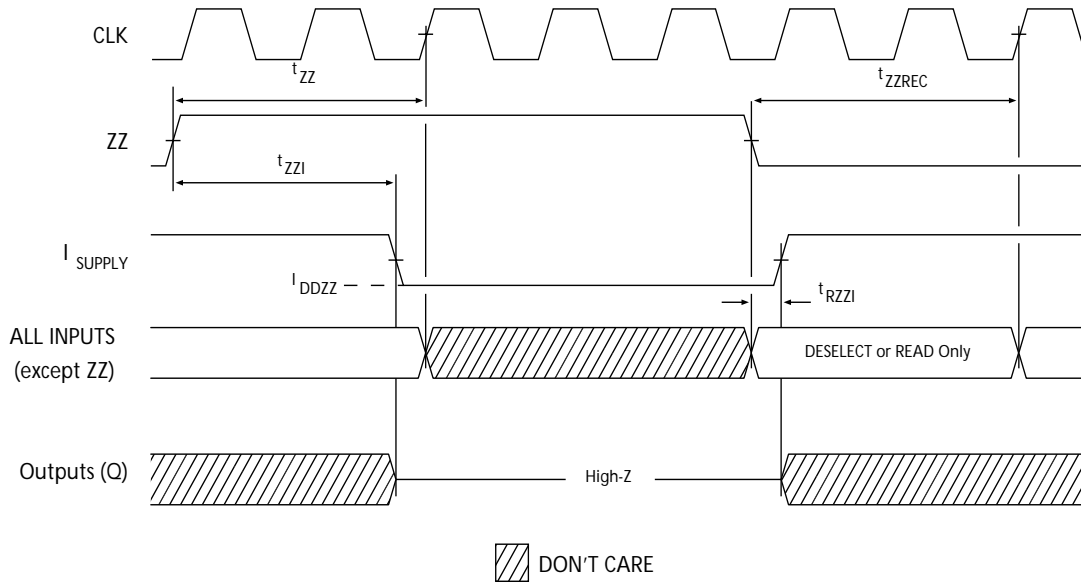
**Notes:**

- 26. The data bus (Q) remains in high-Z following a Write cycle, unless a new read access is initiated by  $\overline{ADSP}$  or  $\overline{ADSC}$ .
- 27.  $\overline{GW}$  is HIGH.



**Timing Diagrams** (continued)

**ZZ Mode Timing**<sup>[28, 29]</sup>



**Notes:**

- 28. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
- 29. DQs are in high-Z when exiting ZZ sleep mode.

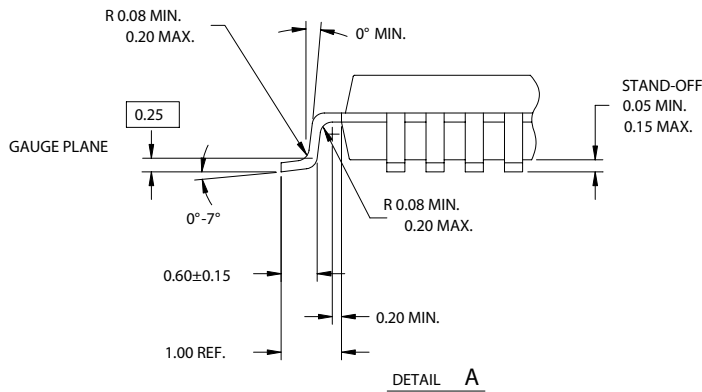
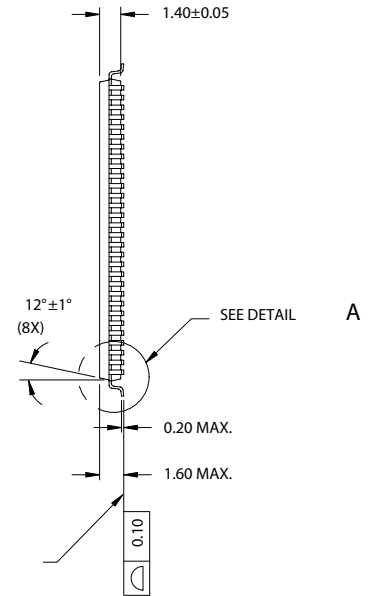
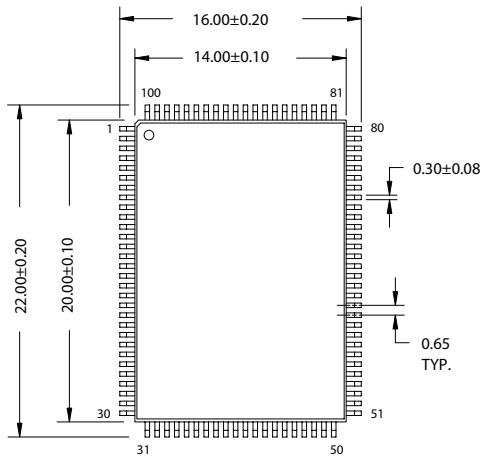
**Ordering Information**

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit [www.cypress.com](http://www.cypress.com) for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range	
133	CY7C1381CV25-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Commercial	
	CY7C1383DV25-133AXC				
	CY7C1381CV25-133BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)		
	CY7C1383DV25-133BGC				
	CY7C1381CV25-133BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free		
	CY7C1383DV25-133BGXC				
	CY7C1381CV25-133BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)		
	CY7C1383DV25-133BZC				
	CY7C1381CV25-133BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free		
	CY7C1383DV25-133BZXC				
	CY7C1381CV25-133AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free		Industrial
	CY7C1383DV25-133AXI				
	CY7C1381CV25-133BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)		
	CY7C1383DV25-133BGI				
	CY7C1381CV25-133BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free		
	CY7C1383DV25-133BGXI				
CY7C1381CV25-133BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)			
CY7C1383DV25-133BZI					
CY7C1381CV25-133BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free			
CY7C1383DV25-133BZXI					
100	CY7C1381CV25-100AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Commercial	
	CY7C1383DV25-100AXC				
	CY7C1381CV25-100BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)		
	CY7C1383DV25-100BGC				
	CY7C1381CV25-100BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free		
	CY7C1383DV25-100BGXC				
	CY7C1381CV25-100BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)		
	CY7C1383DV25-100BZC				
	CY7C1381CV25-100BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free		
	CY7C1383DV25-100BZXC				
	CY7C1381CV25-100AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free		Industrial
	CY7C1383DV25-100AXI				
	CY7C1381CV25-100BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)		
	CY7C1383DV25-100BGI				
	CY7C1381CV25-100BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free		
	CY7C1383DV25-100BGXI				
CY7C1381CV25-100BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)			
CY7C1383DV25-100BZI					
CY7C1381CV25-100BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free			
CY7C1383DV25-100BZXI					

**Package Diagrams**

**100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) (51-85050)**

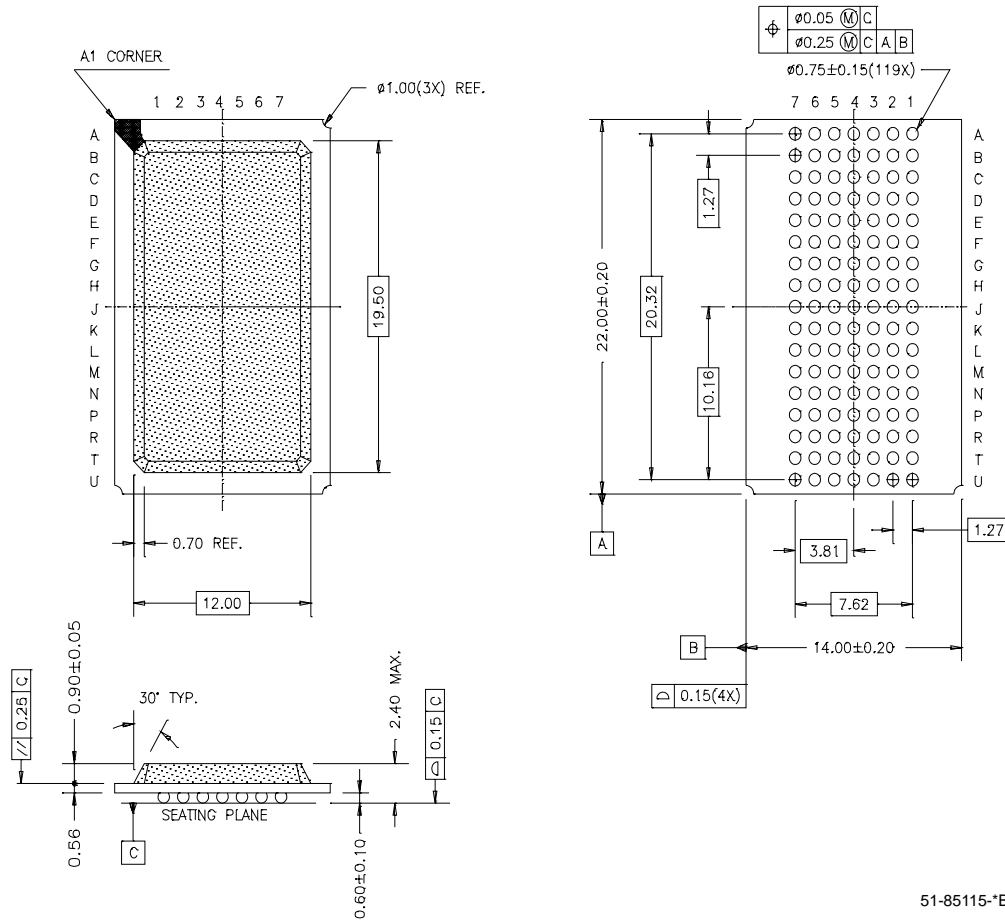


- NOTE:
1. JEDEC STD REF MS-026
  2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE  
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
  3. DIMENSIONS IN MILLIMETERS

51-85050-\*B

**Package Diagrams** (continued)

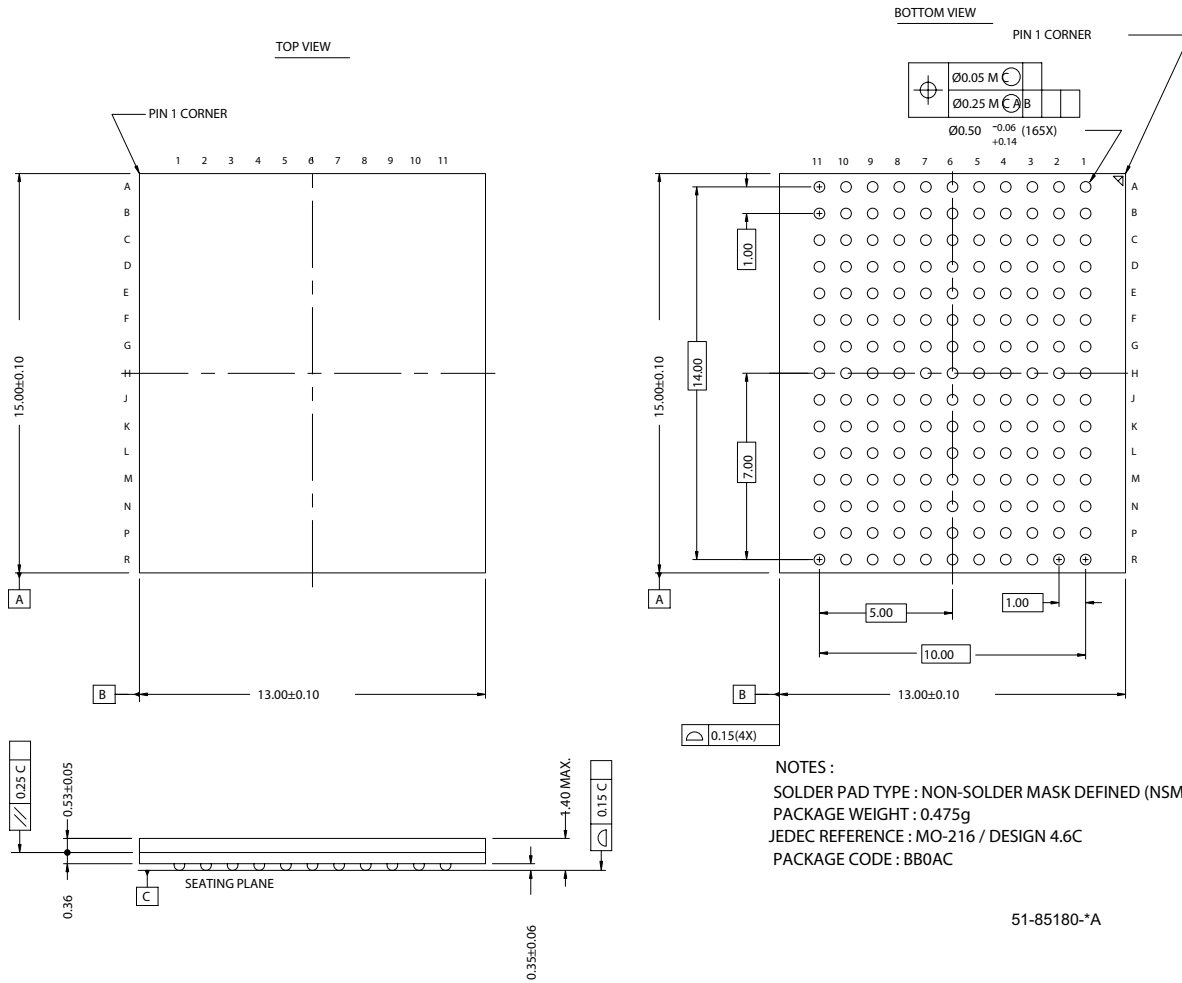
**119-Ball BGA (14 x 22 x 2.4 mm) (51-85115)**



51-85115-B

**Package Diagrams** (continued)

**165-Ball FBGA (13 x 15 x 1.4 mm) (51-85180)**



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**Document History Page**

Document Title: CY7C1381DV25/CY7C1383DV25 18-Mbit (512K x 36/1M x 18) Flow-Through SRAM				
Document Number: 38-05547				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	254518	See ECN	RKF	New data sheet
*A	288531	See ECN	SYT	Edited description under "IEEE 1149.1 Serial Boundary Scan (JTAG)" for non-compliance with 1149.1 Removed 117Mhz Speed Bin Added lead-free information for 100-Pin TQFP, 119 BGA and 165 FBGA Packages Added comment of 'Lead-free BG packages availability' below the Ordering Information
*B	326078	See ECN	PCI	Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added description on EXTEST Output Bus Tri-State Changed description on the Tap Instruction Set Overview and Extest Changed Device Width (23:18) for 119-BGA from 000001 to 101001 Added separate row for 165 -FBGA Device Width (23:18) Changed $\theta_{JA}$ and $\theta_{JC}$ for TQFP Package from 31 and 6 °C/W to 28.66 and 4.08 °C/W respectively Changed $\theta_{JA}$ and $\theta_{JC}$ or BGA Package from 45 and 7 °C/W to 23.8 and 6.2 °C/W respectively Changed $\theta_{JA}$ and $\theta_{JC}$ for FBGA Package from 46 and 3 °C/W to 20.7 and 4.0 °C/W respectively Modified $V_{OL}$ , $V_{OH}$ test conditions Removed comment of 'Lead-free BG packages availability' below the Ordering Information Updated Ordering Information Table
*C	416321	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed the description of $I_X$ from Input Load Current to Input Leakage Current on page# 17 Changed the $I_X$ current values of MODE on page # 18 from -5 $\mu$ A and 30 $\mu$ A to -30 $\mu$ A and 5 $\mu$ A Changed the $I_X$ current values of ZZ on page # 18 from -30 $\mu$ A and 5 $\mu$ A to -5 $\mu$ A and 30 $\mu$ A Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ on page # 18 Replaced Package Name column with Package Diagram in the Ordering Information table
*D	475009	See ECN	VKN	Converted from Preliminary to Final. Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND Changed $t_{TH}$ , $t_{TL}$ from 25 ns to 20 ns and $t_{DOV}$ from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.