

# FM93C56A

## 2K-Bit Serial CMOS EEPROM (MICROWIRE™ Synchronous Bus)

### General Description

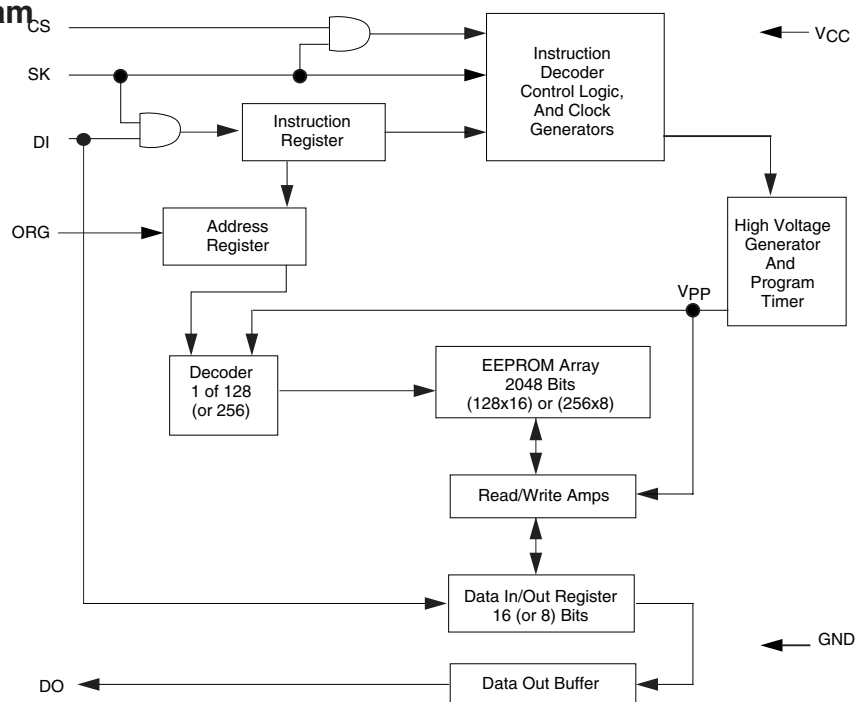
The FM93C56A is 2048 bits of CMOS nonvolatile EEPROM (Electrically Erasable Programmable Read Only Memory) with MICROWIRE serial interface. FM93C56A can be configured for either 128 x 16 bit or 256 x 8 bit array using an organization (ORG) input pin. This device is fabricated using Fairchild Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. This device is available in 8-pin DIP, SO and TSSOP packages.

The MICROWIRE serial interface offered by this EEPROM enables simple interface to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the FM93C56A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All and Erase All.

### Features

- 2.7V to 5.5V operation in all modes
- Typical active current 200µA  
10 µA standby current typical  
1 µA standby current typical (L)  
0.1 µA standby current typical (LZ)
- Self-timed programming cycle
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-Pin TSSOP, 8-pin SO, 8-pin DIP
- Schmitt Trigger inputs and V<sub>CC</sub> lockout to prevent data corruption

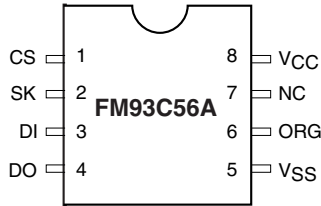
### Block Diagram



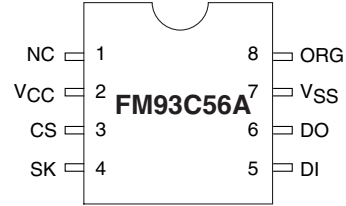
DS800029-1

## Connection Diagram

Dual-In-Line Package (N)  
8-Pin SO Package (M8)  
and 8-Pin TSSOP Package (MT8)



Rotated Die  
(93C56AT)



DS800029-2

Top View

See Package Number N08E, M08A and MTC08

## Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V <sub>SS</sub>	Ground
ORG	Memory Organization Select
NC	No Connect
V <sub>CC</sub>	Positive Power Supply

## Ordering Information

<b>FM</b>	<b>93</b>	<b>C</b>	<b>XX</b>	<b>A</b>	<b>T</b>	<b>LZ</b>	<b>E</b>	<b>XX</b>	
									<b>Package</b>
									N
									M8
									MT8
									<b>Temp. Range</b>
									None
									V
									E
									<b>Voltage Operating Range</b>
									Blank
									L
									LZ
									Blank
									T
									<b>Density</b>
									A
									56
									C
									CS
									<b>Interface</b>
									93
									FM
									<b>Letter Description</b>
									8-Pin DIP
									8-Pin SO8
									8-Pin TSSOP
									0 to 70°C
									-40 to +125°C
									-40 to +85°C
									4.5V to 5.5V
									2.7V to 5.5V
									2.7V to 5.5V and
									<1μA Standby Current
									Normal Pin Out
									Rotated Die Pin Out
									x8 or x16 Configuration
									2K
									CMOS
									Data protect and sequential
									read
									MICROWIRE
									<b>Fairchild Non-Volatile</b>
									<b>Memory</b>

### Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	$V_{CC} + 1$ to $-0.3V$
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

### Operating Conditions

Ambient Operating Temperature	0°C to +70°C
FM93C56A	-40°C to +85°C
FM93C56AE	-40°C to +125°C
FM93C56AV	
Power Supply ( $V_{CC}$ ) Range	4.5V to 5.5V

### DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
$I_{CCA}$	Operating Current		$CS = V_{IH}$ SK = 1 MHz		1	mA
$I_{CCS}$	Standby Current		$CS = 0V$ ORG = $V_{CC}$ or NC		50	$\mu A$
$I_{IL}$	Input Leakage		$V_{IN} = 0V$ to $V_{CC}$ (Note 2)	-1	1	$\mu A$
$I_{ILO}$	Input Leakage ORG Pin		ORG Tied to $V_{CC}$ ORG Tied to $V_{SS}$ (Note 3)	-1 -2.5	1 2.5	$\mu A$
$I_{OL}$	Output Leakage		$V_{IN} = 0V$ to $V_{CC}$	-1	1	$\mu A$
$V_{IL}$	Input Low Voltage			-0.1	0.8	V
$V_{IH}$	Input High Voltage			2	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage		$I_{OL} = 2.1$ mA		0.4	V
$V_{OH1}$	Output High Voltage		$I_{OH} = -400$ $\mu A$	2.4		V
$V_{OL2}$	Output Low Voltage		$I_{OL} = 10$ $\mu A$		0.2	V
$V_{OH2}$	Output High Voltage		$I_{OL} = -10$ $\mu A$	$V_{CC} - 0.2$		V
$f_{SK}$	SK Clock Frequency		(Note 4)	0	1	MHz
$t_{SKH}$	SK High Time	FM93C56A FM93C56AE		250 300		ns
$t_{SKL}$	SK Low Time			250		ns
$t_{SKS}$	SK Setup Time		SK must be at $V_{IL}$ for $t_{SKS}$ before CS goes high	50		ns
$t_{CS}$	Minimum CS Low Time		(Note 5)	250		ns
$t_{CSS}$	CS Set-Up Time			50		ns
$t_{DH}$	DO Hold Time			70		ns
$t_{DIS}$	DI Set-Up Time	FM93C56A FM93C56AE/V		100 200		ns
$t_{CSH}$	CS Hold Time			0		ns
$t_{DIH}$	DI Hold Time			20		ns
$t_{PD}$	Output Delay				500	ns
$t_{SV}$	CS to Status Valid				500	ns
$t_{DF}$	CS to DO in Hi-Z				100	ns
$t_{WP}$	Write Cycle Time				10	ms

### Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

### Operating Range

Ambient Operating Temperature	0°C to +70°C
FM93C56AL/LZ	-40°C to +85°C
FM93C56ALE/LZE	-40°C to +125°C
FM93C56A LV/LZV	-40°C to +125°C
Power Supply (V <sub>CC</sub> )	2.7V to 5.5V

### DC and AC Electrical Characteristics V<sub>CC</sub> = 2.7V to 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I <sub>CCA</sub>	Operating Current		CS = V <sub>IH</sub> , SK = 250KHz		1	mA
I <sub>CCS</sub>	Standby Current		CS = V <sub>IL</sub>		10	μA
	L				1	μA
	LZ				1	μA
I <sub>IL</sub>	Input Leakage		V <sub>IN</sub> = 0V to V <sub>CC</sub> (Note 2)		±1	μA
I <sub>ILO</sub>	Input Leakage		ORG tied to V <sub>CC</sub>	-1	1	μA
	ORG Pin		ORG tied to V <sub>SS</sub> (Note 3)	-2.5	2.5	μA
I <sub>OL</sub>	Output Leakage		V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
V <sub>IL</sub>	Input Low Voltage			-0.1	0.15 V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage			0.8 V <sub>CC</sub>	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage		I <sub>OL</sub> = 10 μA		0.1 V <sub>CC</sub>	V
V <sub>OH</sub>	Output High Voltage		I <sub>OH</sub> = -10 μA	0.9 V <sub>CC</sub>		V
f <sub>SK</sub>	SK Clock Frequency		(Note 4)	0	250	KHz
t <sub>SKH</sub>	SK High Time			1		μs
t <sub>SKL</sub>	SK Low Time			1		μs
t <sub>SKS</sub>	SK Setup Time		SK must be at V <sub>IL</sub> for t <sub>SKS</sub> before CS goes high	0.2		μs
t <sub>CS</sub>	Minimum CS Low Time		(Note 5)	1		μs
t <sub>CSS</sub>	CS Setup Time			0.2		μs
t <sub>DH</sub>	DO Hold Time			70		ns
t <sub>DIS</sub>	DI Setup Time			0.4		μs
t <sub>CSH</sub>	CS Hold Time			0		ns
t <sub>DIH</sub>	DI Hold Time			0.4		μs
t <sub>PD</sub>	Output Delay				2	μs
t <sub>SV</sub>	CS to Status Valid				1	μs
t <sub>DF</sub>	CS to DO in Hi-Z		CS = V <sub>IL</sub>		0.4	μs
t <sub>WP</sub>	Write Cycle Time				15	ms

### Capacitance T<sub>A</sub> = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C <sub>OUT</sub>	Output Capacitance		5	pF
C <sub>IN</sub>	Input Capacitance		5	pF

**Note 1:** Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** Typical leakage values are in the 20 nA range.

**Note 3:** The ORG pin may draw > 1 μA when in the x8 mode ude to an internal pull-up transistor.

**Note 4:** The shortest allowable SK clock period = 1/f<sub>SK</sub> (as shown under the f<sub>SK</sub> f<sub>SK</sub> parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t<sub>SKH</sub> and t<sub>SKL</sub> limits must be observed. Therefore, it is not allowable to set 1/f<sub>SK</sub> = t<sub>SKHminimum</sub> + t<sub>SKLminimum</sub> for shorter SK cycle time operation.

**Note 5:** CS (Chip Select) must be brought low (to V<sub>IL</sub>) for an interval of t<sub>CS</sub> in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

### AC Test Conditions

V <sub>CC</sub> Range	V <sub>IL</sub> /V <sub>IH</sub> Input Levels	V <sub>IL</sub> /V <sub>IH</sub> Timing Level	V <sub>OL</sub> /V <sub>OH</sub> Timing Level	I <sub>OL</sub> /I <sub>OH</sub>
2.7V ≤ V <sub>CC</sub> ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10μA
4.5V ≤ V <sub>CC</sub> ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	2.1mA/-0.4mA

Output Load: 1 TTL Gate (C<sub>L</sub> = 100 pF)

## MICROWIRE I/O Pin Description

### Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 3 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated (see 2 and 3). Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. After entering all required opcode and address data, bringing CS low initiates the (asynchronous) programming cycle.
3. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

### Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin. However, this pin has no effect on the asynchronous programming cycle (see the CS pin section) as the BUSY/READY status is a function of the CS pin only.

### Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

### Data-Out (DO):

All serial communication **out of** the device, Read Data ( during normal reads) as well as READY/BUSY status indication ( during programming ) are performed using this output pin. Note that, during READ operations, the EEPROM device starts to drive the DO output pin "active" after the last address bit (A0) is clocked in. Hence in applications where 3-wire configuration is required ( where DI and DO pins are tied together ) caution must be observed for correct operation. Please refer AN-758 for further information.

### Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to  $V_{CC}$ , the device is configured with a 16-bit data word and if the ORG pin is brought to  $V_{SS}$  (Ground), the device is configured with an 8-bit data word. If the ORG pin is left floating, the device will default to a 16-bit data word.

### Instruction Set for the FM93C56A

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	256 x 8	9 Bits
1	128 x 16	8 Bits

**Note:** The leading (MSB) bit is a "don't care," but must be included in the address string.

### 128 by 16-Bit Organization (FM93C56A when ORG = V<sub>CC</sub> or NC)

Instruction	SB	OP-Code 2 Bits	Address 8 Bits	Data 16 Bits	Comments
READ	1	10	A7–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXX		Disables all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
WRITE	1	01	A7–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

**Note:** The A7 bit is a "don't care" bit, but must be entered in the Address string.

**Note:** X = Don't care.

### 256 by 8-Bit Organization (FM93C56A when ORG = GND)

Instruction	SB	OP-Code 2 Bits	Address 9 Bits	Data 8 Bits	Comments
READ	1	10	A8–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXX		Disables all programming modes.
ERASE	1	11	A8–A0		Erase selected register.
WRITE	1	01	A8–A0	D7–D0	Writes data pattern D7–D0 into selected registers.
ERAL	1	00	10XXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

**Note:** The A8 bit is a "don't care" bit, but must be entered in the Address string.

**Note:** X = Don't care.

## Functional Description

### Programming:

- Programming is initiated by clocking in the Start Bit, Opcode bits, Address bits and the 8/16 data bits (refer to the ORG pin section).
- Programming is started by bringing the CS pin low. Once the programming cycle is started, it cannot be stopped. (Bringing V<sub>CC</sub> low will stop any programming, but will also result in data corruption.)
- The status of the programming cycle (BUSY or READY) is observed by bringing the CS pin high and observing the output state. If the output is LOW, the device is still programming (BUSY). If the output is HIGH, the programming cycle has been completed and the device is ready for the next operation. Note that the output will be tri-stated each time CS is brought low and the READY/BUSY status will be shown each time CS is brought high.
- After programming, the READY state (output HIGH) can be reset and the output tri-stated by clocking in a single Start Bit. This Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. In any case, clocking in a '1' bit will tri-state the output.

### Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK after the last address bit (A0) is clocked in.

### Erase/Write Enable (EWEN)

When V<sub>CC</sub> is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V<sub>CC</sub> is removed from the part.

## Functional Description (Continued)

### Erase/Write Disable (EWDS):

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

### Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. Please refer to the Programming section for details.

### Write (WRITE):

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the FM93C56A in the x8 organization) to be written into the specified address. Please refer to the Programming section for details.

### Erase All (ERAL):

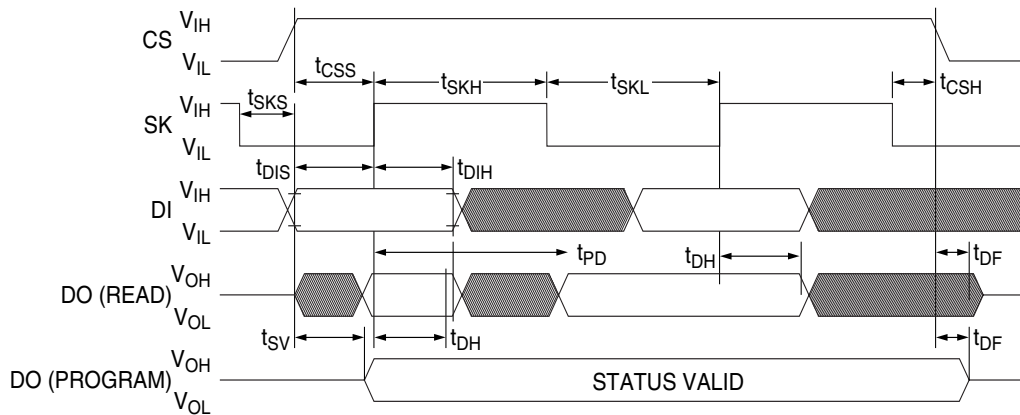
The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

### Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

## Timing Diagrams for the FM93C56A

### Synchronous Data Timing



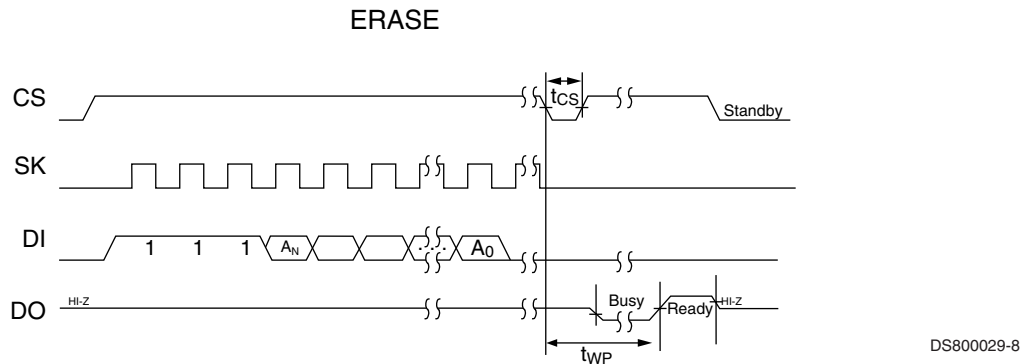
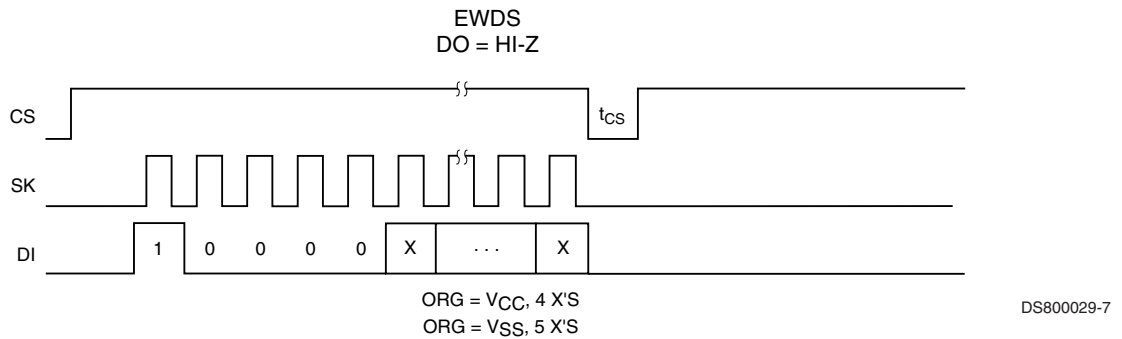
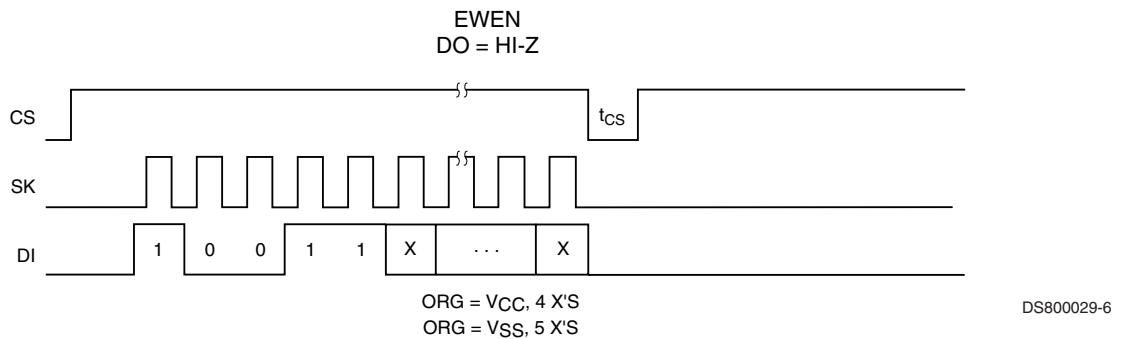
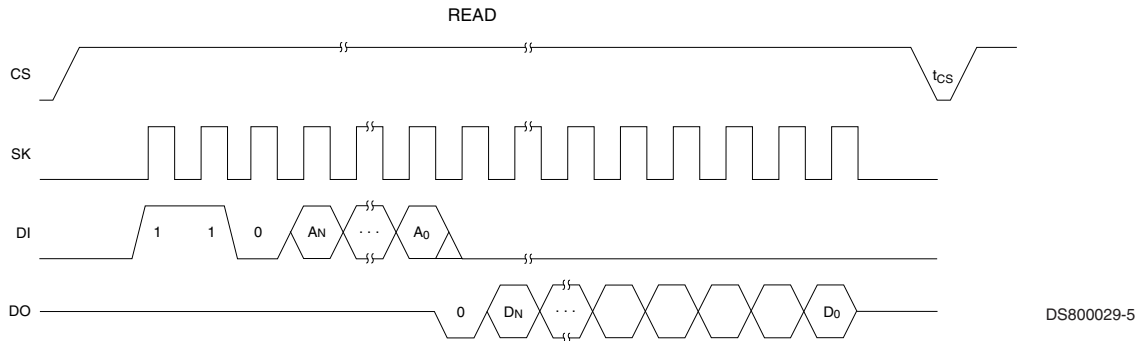
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**Timing Diagrams for the FM93C56A (Continued)**

**Key for Timing Diagrams  
Organization of Address and Data Fields for FM93C56A**

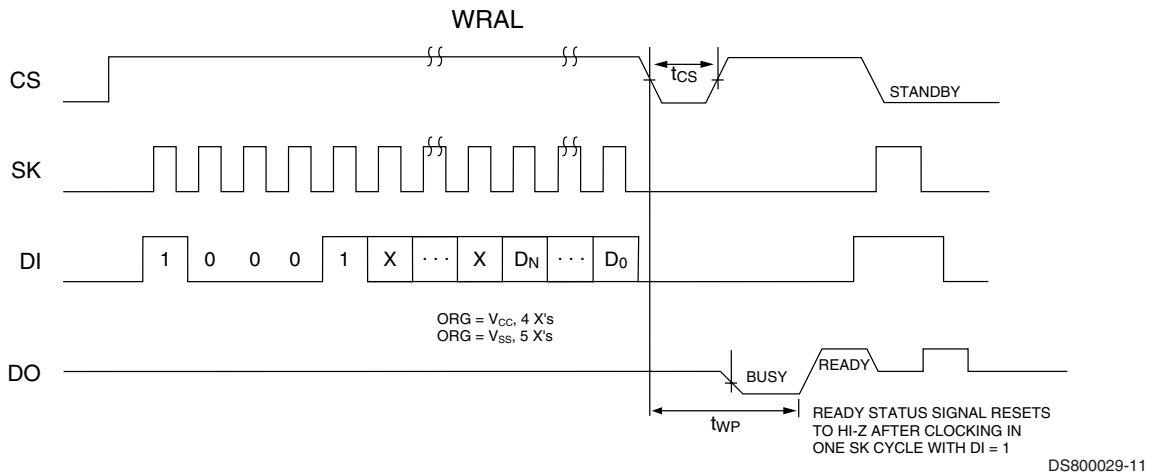
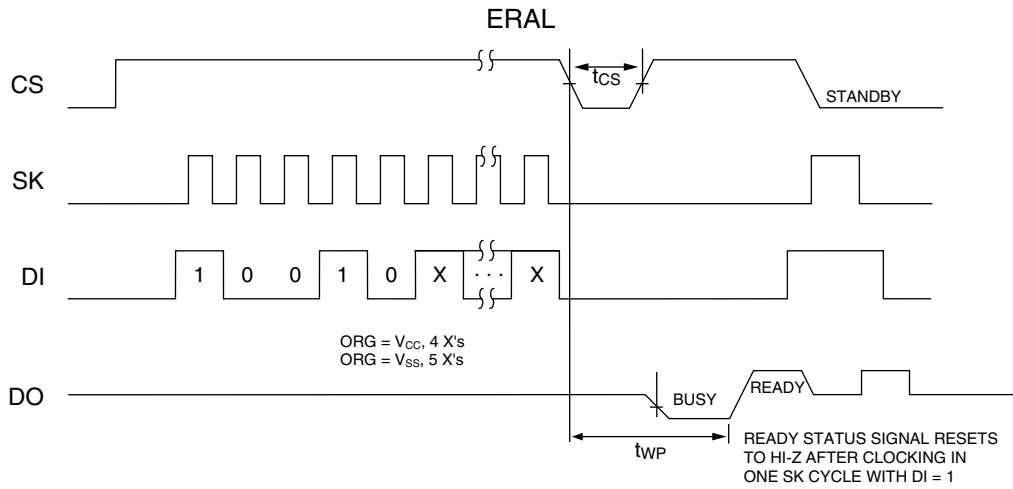
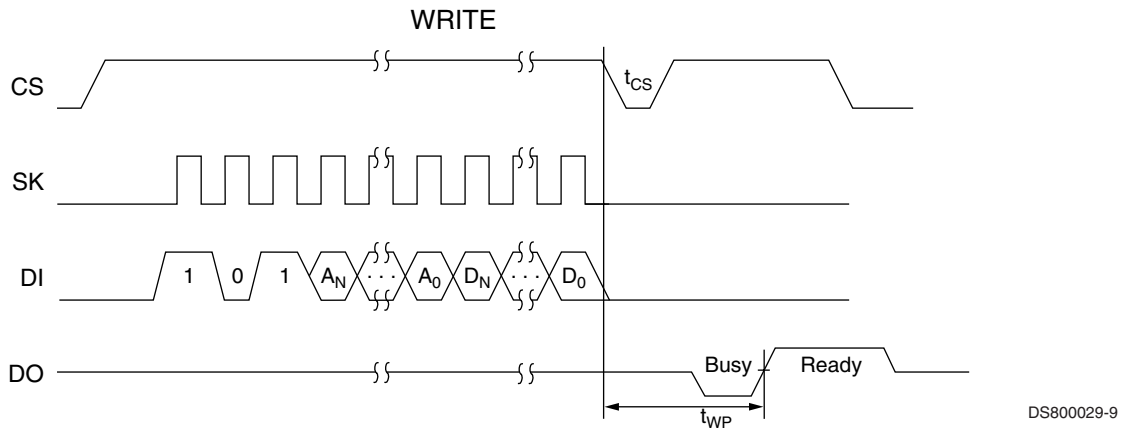
ORG Pin	Organization	A <sub>N</sub>	D <sub>N</sub>
V <sub>CC</sub> or NC	128 x 16	A7	D15
V <sub>SS</sub>	256 x 8	A8	D7

**Note:** The MSB is "don't care."

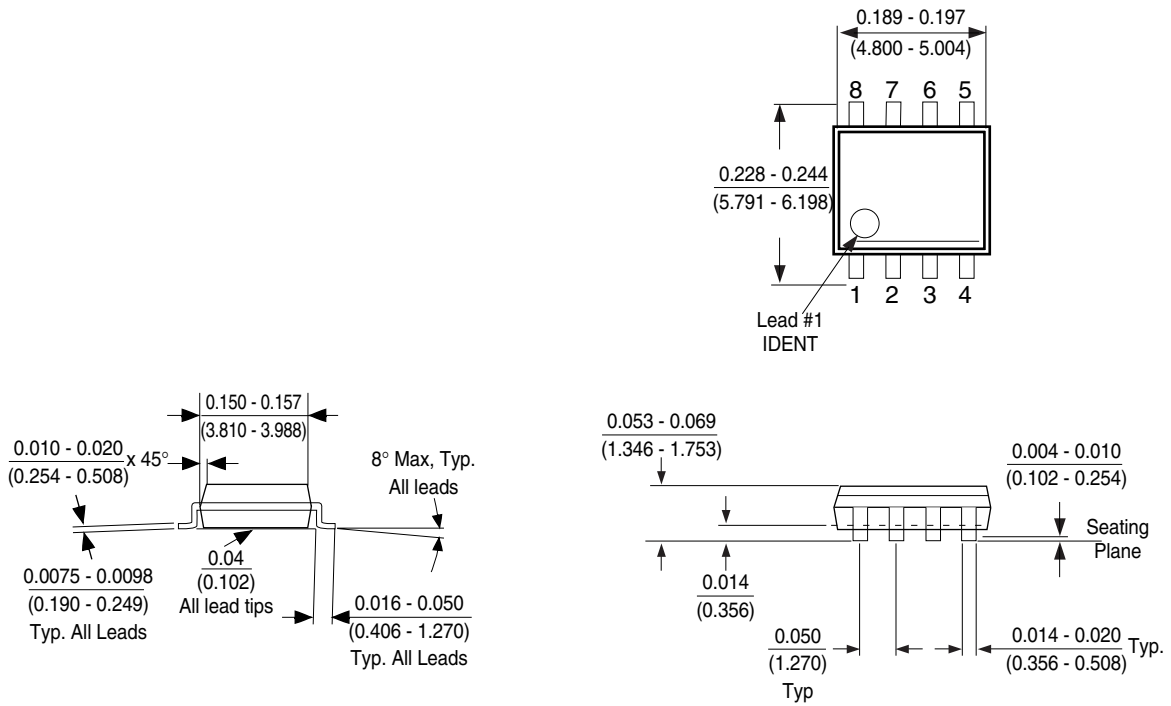




**Timing Diagrams for the FM93C56A (Continued)**

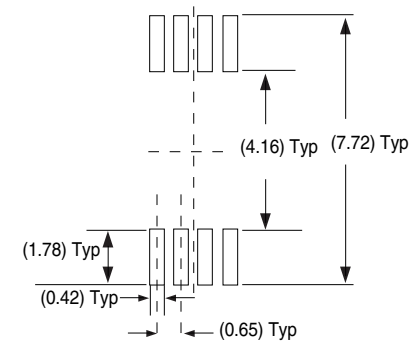
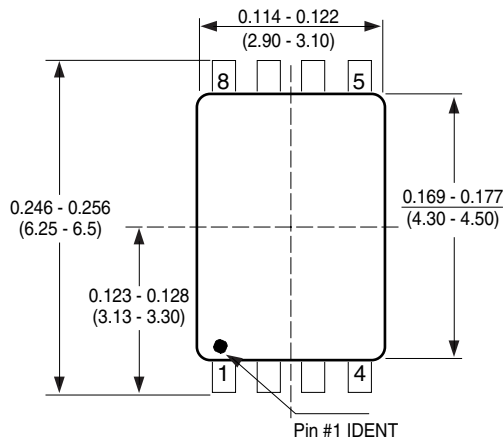


**Physical Dimensions** inches (millimeters) unless otherwise noted

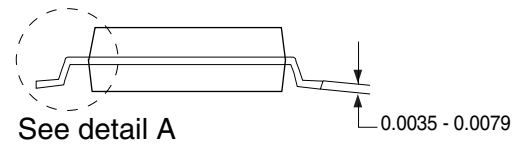
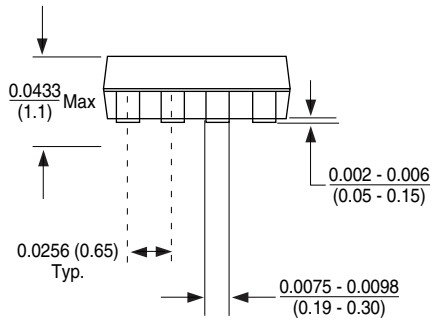


**Molded Small Outline Package (M8)**  
**Package Number M08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted

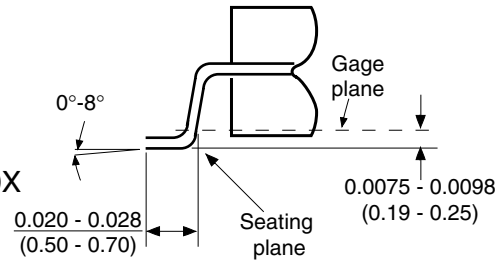


Land pattern recommendation



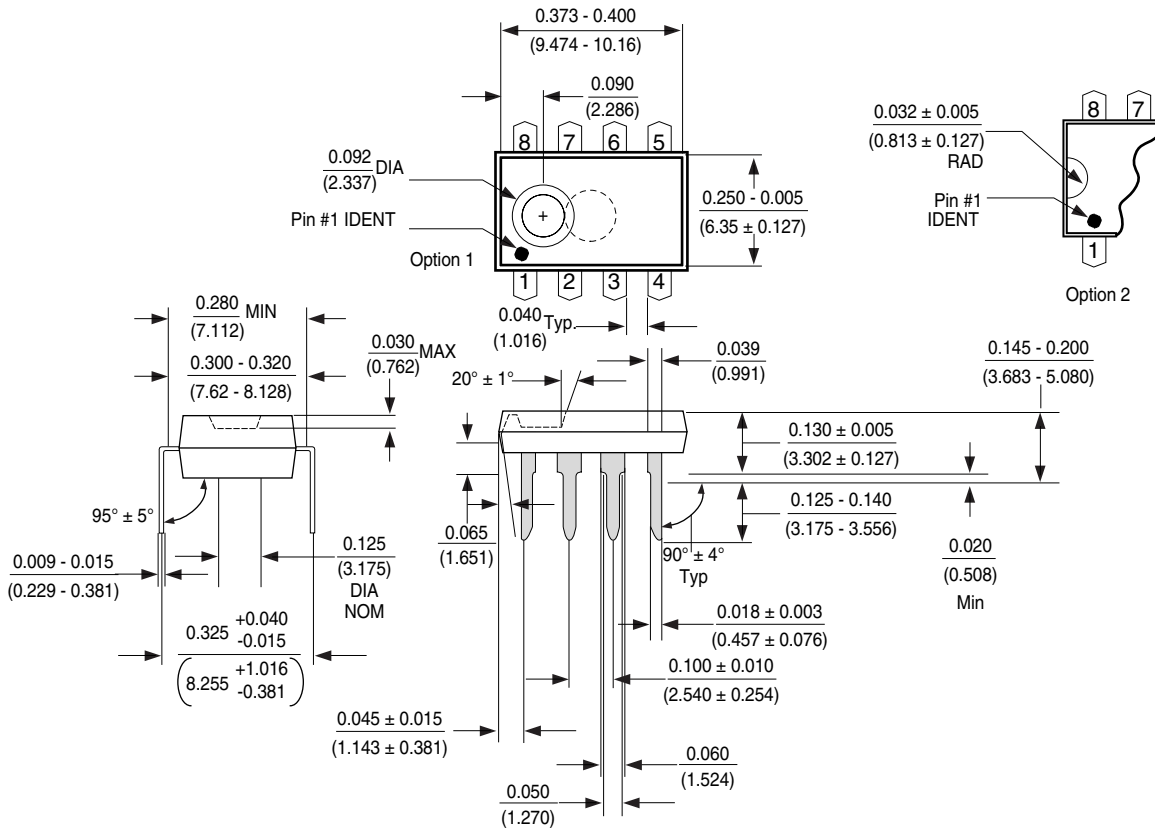
See detail A

**DETAIL A**  
Typ. Scale: 40X



**8-Pin Molded TSSOP, JEDEC (MT8)**  
**Package Number MTC08**

**Physical Dimensions** inches (millimeters) unless otherwise noted



**Molded Dual-In-Line Package (N)  
Package Number N08E**

**Life Support Policy**

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- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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