

## 74LS258A, S258 Data Selectors/Multiplexers

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)  
*Product Specification*

### Logic Products

#### FEATURES

- Multifunction capability
- Inverting data path
- 3-State outputs
- See '257 for non-inverting version

#### DESCRIPTION

The '258 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The  $I_0$  inputs are selected when the Select input is LOW and the  $I_1$  inputs are selected when the Select input is HIGH. Data appears at the outputs in inverted (complementary) form.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS258A	13ns	9mA
74S258	6ns	48mA

#### ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S258N, N74LS258AN
Plastic SOL-16	N74LS258AD

#### NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

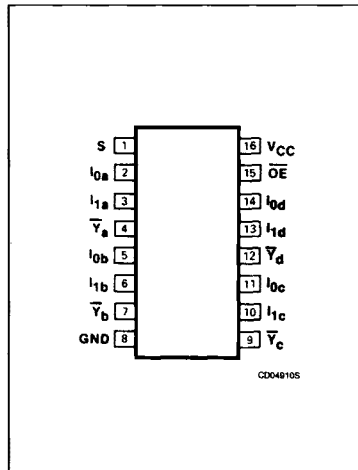
#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
S	Input	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

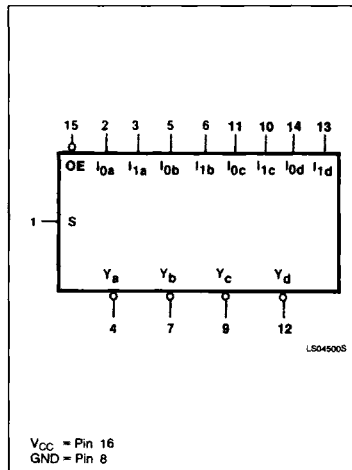
#### NOTE:

Where a 74S unit load (Sul) is to be  $50\mu A$   $I_{IH}$  and  $-2.0mA$   $I_{IL}$ , and a 74LS unit load (LSul) is  $20\mu A$   $I_{IH}$  and  $-0.4mA$   $I_{IL}$ .

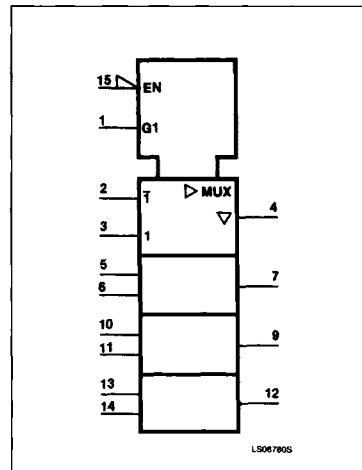
#### PIN CONFIGURATION



#### LOGIC SYMBOL



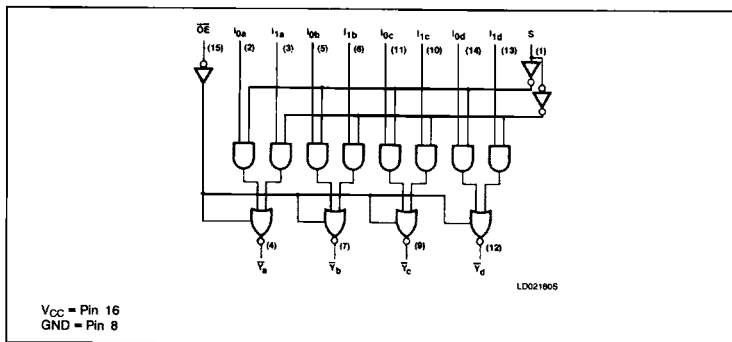
#### LOGIC SYMBOL (IEEE/IEC)



# Data Selectors/Multiplexers

# 74LS258A, S258

## LOGIC DIAGRAM



The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ( $\overline{OE}$ ) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

## FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
		$I_0$	$I_1$	
$\overline{OE}$	S			$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level  
L = LOW voltage level  
X = Don't care  
(Z) = HIGH impedance (off) state

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	74S	UNIT
$V_{CC}$	Supply voltage	7.0	7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
$I_{IN}$	Input current	-30 to +1	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in HIGH output state	-0.5 to + $V_{CC}$	-0.5 to + $V_{CC}$	V
$T_A$	Operating free-air temperature range	0 to 70		°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
$V_{CC}$	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
$V_{IH}$	HIGH-level input voltage	2.0			2.0			V
$V_{IL}$	LOW-level input voltage			+0.8			+0.8	V
$I_{IK}$	Input clamp current			-18			-18	mA
$I_{OH}$	HIGH-level output current			-2.6			-6.5	mA
$I_{OL}$	LOW-level output current			24			20	mA
$T_A$	Operating free-air temperature	0		70	0		70	°C

## Data Selectors/Multiplexers

## 74LS258A, S258

**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS <sup>1</sup>		74LS258A			74S258			UNIT	
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max		
V <sub>OH</sub> HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX	I <sub>OH</sub> = MAX	2.4	3.1		2.4	3.2		V	
		I <sub>OH</sub> = -1mA (74S)				2.7			V	
V <sub>OL</sub> LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX	I <sub>OL</sub> = MAX		0.35	0.5			0.5	V	
		I <sub>OL</sub> = 12mA (74LS)		0.25	0.4				V	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>i</sub> = I <sub>IK</sub>				-1.5			-1.2	V	
I <sub>OZH</sub> Off-state output current, HIGH-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = MIN	V <sub>O</sub> = 2.7V			20				μA	
		V <sub>O</sub> = 2.4V						50	μA	
I <sub>OZL</sub> Off-state output current, LOW-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = MIN	V <sub>O</sub> = 0.4V			-20				μA	
		V <sub>O</sub> = 0.5V						-50	μA	
I <sub>i</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5V						1.0	mA	
		V <sub>I</sub> = 7.0V	S input		0.2				mA	
			Other inputs		0.1				mA	
I <sub>IH</sub> HIGH-level input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 2.7V	S input		40			100	μA	
			Other inputs		20			50	μA	
		V <sub>I</sub> = 0.4V	S input			-0.8			mA	
I <sub>IL</sub> LOW-level input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 0.4V	Other inputs		-0.4				mA	
			V <sub>I</sub> = 0.5V	S input					-4	mA
		V <sub>I</sub> = 0.5V	Other inputs						-2	mA
			I <sub>OS</sub> Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX	-30		-130	-40	
I <sub>CC</sub> Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX	I <sub>CC</sub> H Outputs HIGH		4	7		36	56	mA	
		I <sub>CC</sub> L Outputs LOW		8.8	14		52	81	mA	
		I <sub>CC</sub> Z Outputs OFF		12	19		56	87	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- I<sub>OS</sub> is tested with V<sub>OUT</sub> = +0.5V and V<sub>CC</sub> = V<sub>CC</sub> MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I<sub>CC</sub> with all outputs open and all possible inputs grounded while achieving the stated output conditions.

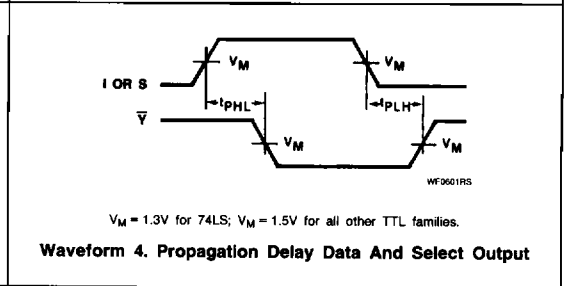
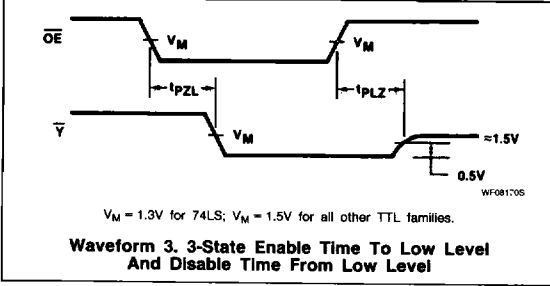
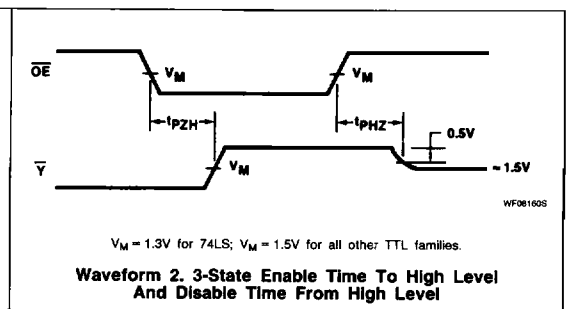
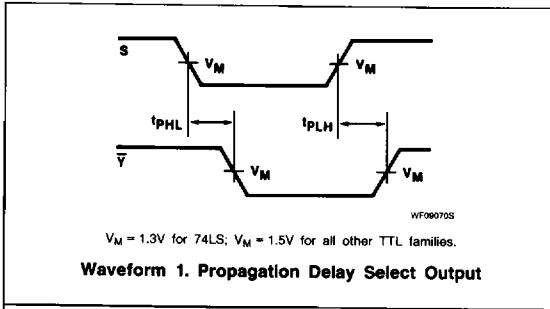
**AC ELECTRICAL CHARACTERISTICS** T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C <sub>L</sub> = 45pF, R <sub>L</sub> = 667Ω		C <sub>L</sub> = 15pF, R <sub>L</sub> = 280Ω		
		Min	Max	Min	Max	
t <sub>PLH</sub> Propagation delay t <sub>PHL</sub> Data to output	Waveform 4		18 18		6.0 6.0	ns
t <sub>PLH</sub> Propagation delay t <sub>PHL</sub> Select to output	Waveforms 1 & 4		21 21		12 12	ns
t <sub>pZH</sub> Output enable to HIGH level	Waveform 2		30		19.5	ns
t <sub>pZL</sub> Output enable to LOW level	Waveform 3		30		21	ns
t <sub>PHZ</sub> Output disable from HIGH level	Waveform 2, C <sub>L</sub> = 5pF		30		8.5	ns
t <sub>PLZ</sub> Output disable from LOW level	Waveform 3, C <sub>L</sub> = 5pF		25		14	ns

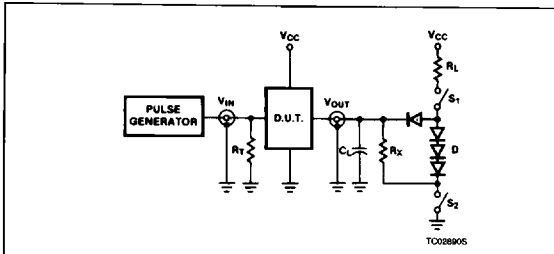
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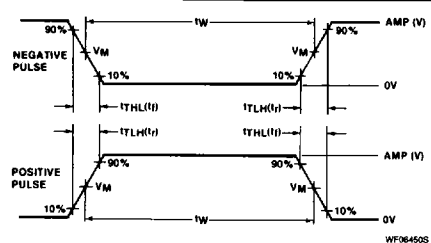
## AC WAVEFORMS



## TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3V$  for 74LS;  $V_M = 1.5V$  for all other TTL families.

Input Pulse Definition

### SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PHZ}$	Closed	Closed
$t_{PLZ}$	Closed	Closed

### DEFINITIONS

$R_L$  = Load resistor to  $V_{CC}$ ; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$  for 74, 74S,  $R_X = 5k\Omega$  for 74LS.

$t_{TLH}$ ,  $t_{THL}$  Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns