MX23L8000

8M-BIT MASK ROM (8 BIT OUTPUT)

FEATURES

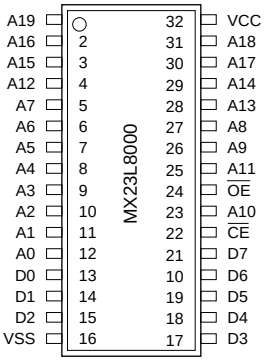
- Bit organization
  - 1M x 8 (byte mode)
- Fast access time
  - Random access: 150ns (max.) for 2.7~3.6V
    120ns (max.) for 3.0~3.6V
- Current
  - Operating: 20mA
  - Standby: 5uA
- Supply voltage
  - 2.7V~3.6V
- Package
  - 32 pin SOP (450mil)
  - 32 pin TSOP (8mm x 20mm)

ORDER INFORMATION

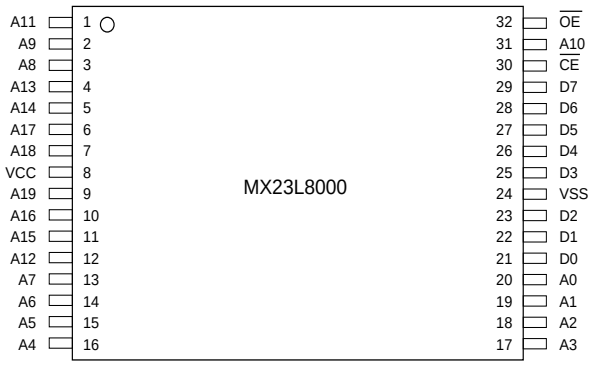
Part No.	Access Time	Package
MX23L8000MC-12	120ns	32 pin SOP
MX23L8000MC-15	150ns	32 pin SOP
MX23L8000MC-20	200ns	32 pin SOP
MX23L8000MI-15	150ns	32 pin SOP (Industrial)
MX23L8000MI-20	200ns	32 pin SOP (Industrial)
MX23L8000TC-12	120ns	32 pin TSOP
MX23L8000TC-15	150ns	32 pin TSOP
MX23L8000TC-20	200ns	32 pin TSOP
MX23L8000TI-15	150ns	32 pin TSOP (Industrial)
MX23L8000TI-20	200ns	32 pin TSOP (Industrial)

PIN CONFIGURATION

32 SOP



32 TSOP



PIN DESCRIPTION

Symbol	Pin Function
A0~A19	Address Inputs
D0~D7	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	-40° C to 85° C
Storage Temperature	Tstg	-65° C to 125° C

DC CHARACTERISTICS (Ta = -40° C ~ 85° C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	VCC-0.2V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.1V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.4V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	20mA	tRC=150ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$=VIH
Standby Current (CMOS)	ISTB2	-	5uA	$\overline{CE}$> VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25° C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25° C, f = 1MHZ

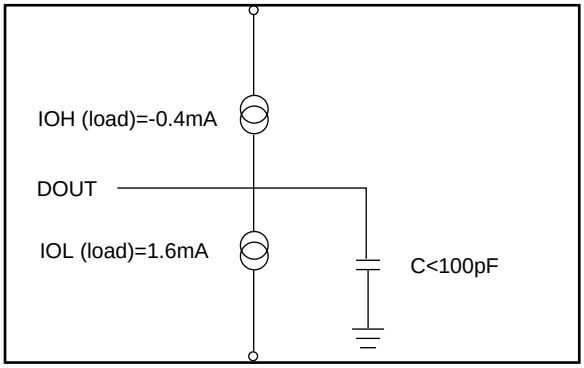
AC CHARACTERISTICS (Ta = -40° C ~ 85° C, VCC = 2.7V~3.6V)

Item	Symbol	23L8000-12		23L8000-15		23L8000-20	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	120ns	-	150ns	-	200ns	-
Address Access Time	tAA	-	120ns	-	150ns	-	200ns
Chip Enable Access Time	tACE	-	120ns	-	150ns	-	200ns
Output Enable Time	tOE	-	60ns	-	70ns	-	100ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

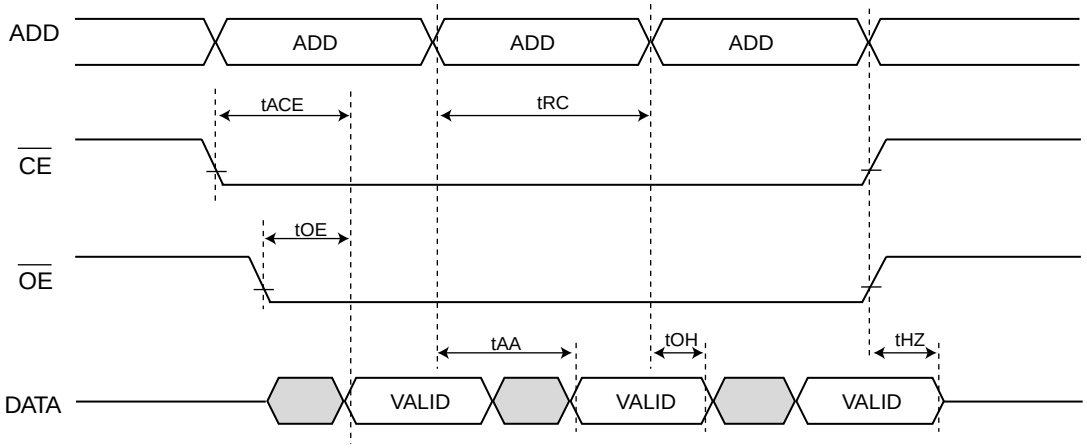
Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

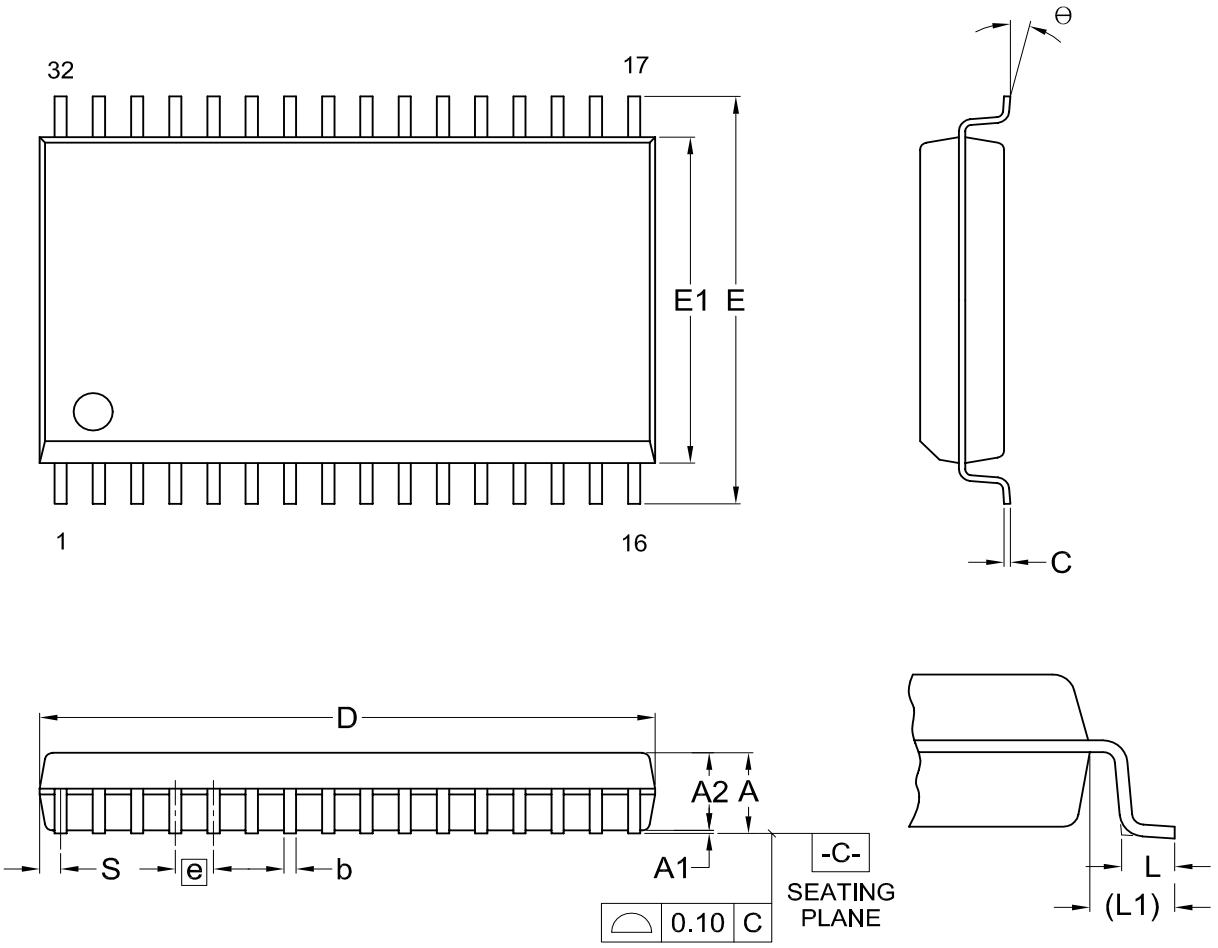
RANDOM READ



Note:$\overline{CE}$, $\overline{OE}$ are enable

PACKAGE INFORMATION

Title: **Package Outline for SOP 32L (450MIL)**

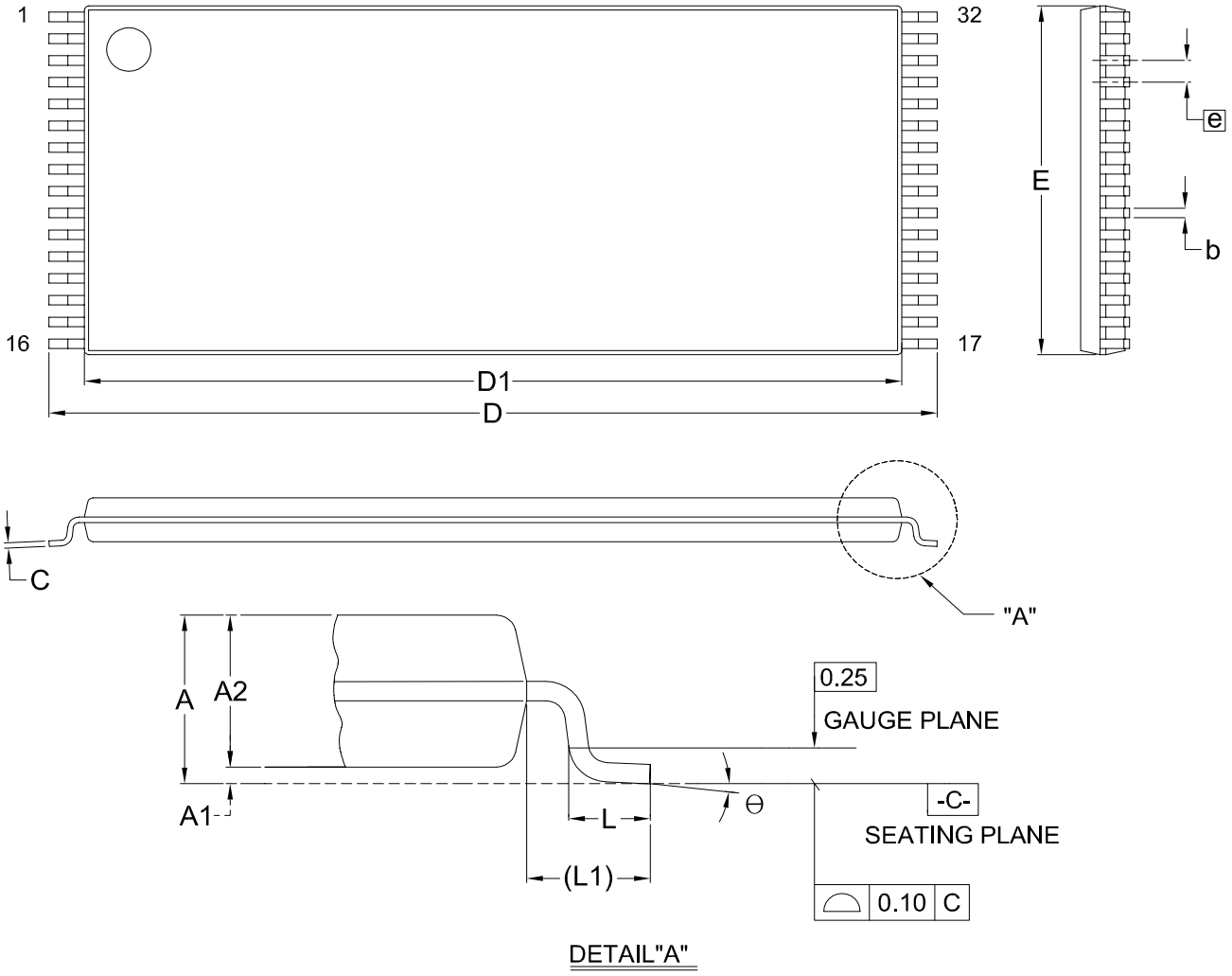


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	—	0.10	2.59	0.36	0.15	20.32	13.92	11.18		0.56	1.20	0.58	0
	Nom.	---	0.15	2.69	0.41	0.20	20.45	14.12	11.30	1.27	0.76	1.40	0.70	5
	Max.	3.00	0.20	2.80	0.51	0.25	20.57	14.32	11.43		0.96	1.60	0.83	8
Inch	Min.	---	0.004	0.102	0.014	0.006	0.800	0.548	0.440		0.022	0.047	0.023	0
	Nom.	—	0.006	0.106	0.016	0.008	0.805	0.556	0.445	0.050	0.030	0.055	0.028	5
	Max.	0.118	0.008	0.110	0.020	0.010	0.810	0.564	0.450		0.038	0.063	0.033	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404	5	MO-099			11-26-'03

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
1.5	Supply Voltage: The supply voltage is changed as 2.7V~3.6V instead of 3.0V~3.6V. AC Characteristics: The output high Z delay is changed as 20ns instead of 50ns. AC Test Conditions: The output timing level is changed as 1.4V instead of 0.8V and 2.0V.		
1.6	AC CHARACTERISTICS tOH 10ns-->0ns	P2	FEB/01/1999
1.7	Add 120ns(max.) for 3.0~3.6V	P1,2	AUG/21/2000
1.8	Modify Package Information	P4~5	JUL/16/2001
1.9	Modify Package Information	P4~5	NOV/21/2002

MACRONIX INTERNATIONAL CO., LTD.

Headquarters:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

Europe Office :
TEL:+32-2-456-8020
FAX:+32-2-456-8021

Hong Kong Office :
TEL:+86-755-834-335-79
FAX:+86-755-834-380-78

Japan Office :
Kawasaki Office :
TEL:+81-44-246-9100
FAX:+81-44-246-9105
Osaka Office :
TEL:+81-6-4807-5460
FAX:+81-6-4807-5461

Singapore Office :
TEL:+65-6346-5505
FAX:+65-6348-8096

Taipei Office :
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-262-8887
FAX:+1-408-262-8810

http : //www.macronix.com