H1852
H1852C

1800 CMOS Microprocessor Family
Input/Output Port

HUGHES
AIRCRAFT COMPANY

MICROELECTRONICS CENTER

DESCRIPTION

Hughes 1852 is an 8 bit mode programmable CMOS Input or Output Port. The device acts as a buffer between the 1802A data bus and the peripheral data bus. It can also be used as an 8 bit address latch for multiplexed address buses.

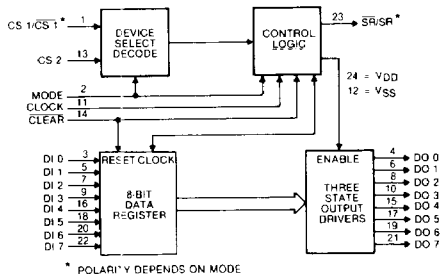
The Mode control signal programs the 1852 as an input port mode (mode = 0) or an output port (mode = 1). As an input port, data (DI 0-DI 7) is strobed from the peripheral into the 8 bit buffer register by a logic high on the Clock signal input; the negative clock transition sets the service request flip flop low ($\overline{SR}$ = 0) and latches data. When the CS 1 and CS 2 signals are enabled, the data (DO 0-DO 7) is read onto the microprocessor bus. The signal $\overline{SR}$ is then reset ($\overline{SR}$ = 1) on the negative transition $\overline{CS1} \cdot CS2$. As an output port, data (DI 0-DI 7) is strobed into the buffer register by the microprocessor when $\overline{CS1}$, CS 2, and the Clock input are activated. The Service Request is set on the negative transition of $\overline{CS1} \cdot CS2$, and will remain until the following negative transition of the clock. The Output driver is always enabled when the output mode is chosen. A $\overline{Clear}$ control allows asynchronous resetting of the port's register (DO 0-DO 7) and service request flip flop.

The 1852 operates over a 4—10.5 voltage range while the 1852C operates over a 4—6.5 voltage range. The 1852 is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request. are available upon request.

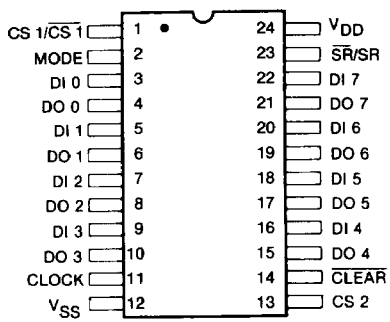
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components.
- Parallel 8 Bit Data Register and Buffer
- Stored Service Request
- Asynchronous Register Clear
- Single Voltage Supply
- Low Quiescent and Operating Power

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to +125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1852 ..... −0.5 to + 11 Volts
- 1852C ..... −0.5 to +7 Volts

Input Voltage Range ..... V_{SS} −0.3V to V_{DD} + 0.3V

Storage Temperature Range (T_{stg}) .... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range.

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
				1852			1852C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Supply-Voltage Range (At T_A = Full Package Temperature Range)	–	–	–	4	–	10.5	4	–	6.5	V
Recommended Input Voltage Range	–	–	–	V_{SS}	–	V_{DD}	V_{SS}	–	V_{DD}	V
Static Electrical Characteristics at T_A = −55 to + 125°C, V_{DD} nominal										
Quiescent Device Current, I_{DD} [4]	–	0,5	5	–	–	50	–	–	100	µA
	–	0,10	10	–	–	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.2	3.2	–	1.2	3.2	–	mA
	0.5	0,10	10	2.7	6	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1.2	−2.3	–	−1.2	−2.3	–	mA
	9.5	0,10	10	−2.7	−6	–	–	–	–	
Output Voltage Low Level, V_{OL} [1, 3]	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage High Level, V_{OH} [3]	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	2.5, 2.5	–	5	–	–	1.25	–	–	1.25	V
	5, 5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	2.5, 2.5	–	5	3.5	–	–	3.5	–	–	
	5, 5	–	10	7	–	–	–	–	–	
Input Current, I_{IN} [4]	–	0,5	5	–	–	±1	–	–	±1	µA
	–	0,10	10	–	–	±1	–	–	–	
3-State Output Leakage Current, I_{OUT} [4]	0,5	0,5	5	–	–	±1	–	–	±1	
	0,10	0,10	10	–	–	±1	–	–	–	
Operating Current, I_{DD1} [2, 3]	–	0,5	5	–	.1	2	–	.1	5	mA
	–	0,10	10	–	.4	5	–	–	–	
Input Capacitance C_{IN} [3]	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT} [3]	–	–	–	–	5	7.5	–	–	–	
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −55 to 125°C, V_{DD} = 5, 10v, V_{IH} = V_{DD}, V_{IL} = V_{SS}, C_L = 50pF, LIMITS AT V_{DD} = + 10V APPLY TO THE 1852 ONLY.										
Required Write Pulse Width, t_{WW}	–	–	5	–	130	250	–	130	250	ns
	–	–	10	–	65	130	–	–	–	
Required Data Setup Time, t_{DS}	–	–	5	–	−10	0	–	−10	0	
	–	–	10	–	−5	0	–	–	–	
Required Data Hold Time, t_{DH}	–	–	5	–	75	195	–	75	195	
	–	–	10	–	35	97	–	–	–	

*Typical values are for T_A = +25° C and nominal V_{DD}.
NOTE 1: I_{OL} = I_{OH} = 1 µA.
NOTE 2: Operating current is measured at 2MHz in an 1802 system with open outputs and a program of alternating 1 and 0 data pattern.
NOTE 3: Design assured but not tested.
NOTE 4: Parameters guaranteed by other tests at −55 C.

DYNAMIC ELECTRICAL CHARACTERISTICS, cont.

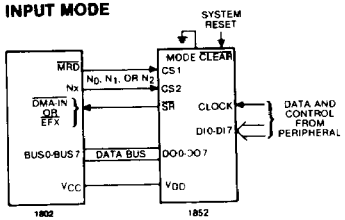
Propogation Delay Times, t_{PLH}, t_{PHL}										
Service Request: Clear to SR, t_{RSR}[3]	–	–	5	–	170	340	–	170	340	ns
	–	–	10	–	85	170	–	–	–	
Clock to SR, t_{CSR}[3]	–	–	5	–	120	240	–	120	240	
	–	–	10	–	60	120	–	–	–	
Select to SR, t_{SSR}[3]	–	–	5	–	120	240	–	120	240	
	–	–	10	–	60	120	–	–	–	
Input Mode: Data Output Hold Time, t_{DOH}[1,3]	–	–	5	30	185	370	30	185	370	ns
	–	–	10	15	100	200	–	–	–	
Select to Data Output, t_{SDO}[1,3]	–	–	5	30	185	370	30	185	370	
	–	–	10	15	100	200	–	–	–	
Output Mode: Clear to Data Output, t_{RDO}[3]	–	–	5	–	140	280	–	140	280	ns
	–	–	10	–	70	140	–	–	–	
Write to Data Output, t_{WDO}[3]	–	–	5	–	220	440	–	220	440	
	–	–	10	–	110	220	–	–	–	
Data Input to Data Output, t_{DDO}[3]	–	–	5	–	100	200	–	100	200	
	–	–	10	–	50	100	–	–	–	

* Typical Values are for T_A = + 25°C and nominal V_{DD}

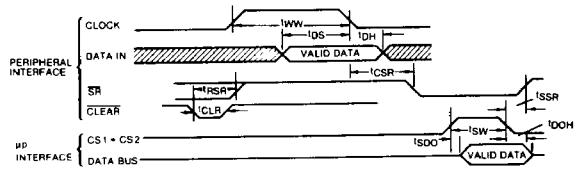
NOTE 1: Minimum value is measured from CS 2; maximum value is measured from CS 1.

SYSTEM INTERCONNECT

INPUT MODE



INPUT MODE CS1•CS2 is the overlap of CS1 = 1 and CS2 = 1



MODE = V_{SS} MODE 0 (INPUT)

CLOCK	CS1•CS2	CLEAR	DATA OUTPUT
X	0	X	HIGH IMPEDANCE
0	1	0	0
0	1	1	DATA LATCH
1	1	X	DATA INPUT

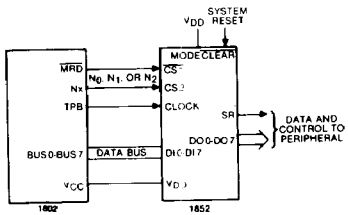
$\overline{SR}$=0 CLOCK↓ ($\overline{CLEAR}$ = 1, CS1•CS2 = 0)
$\overline{SR}$=1 (CS1•CS2)↓ OR ($\overline{CLEAR}$) ↓

MODE = V_{DD} MODE 1 (OUTPUT)

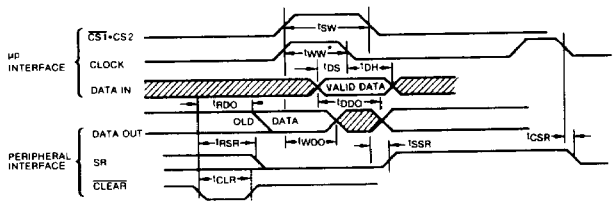
CLOCK	CS1•CS2	CLEAR	DATA OUTPUT
0	X	0	0
0	X	1	DATA LATCH
X	0	1	DATA LATCH
1	1	X	DATA INPUT

SR=1 $\overline{CS1}$•CS2↑ ($\overline{CLEAR}$ = 1)
SR=0 CLOCK↑ ($\overline{CLEAR}$ = 1, $\overline{CS1}$•CS2 = 0) OR ($\overline{CLEAR}$)↓

OUTPUT MODE



OUTPUT MODE $\overline{CS1}$•CS2 is the overlap of $\overline{CS1}$ = 0 and CS2 = 1

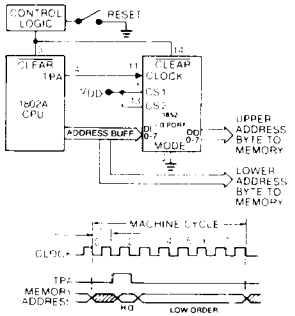


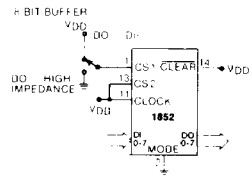
*Write is the overlap of $\overline{CS1}$•CS2 and Clock

APPLICATION EXAMPLES

Address Latch

1852 can be used as an address latch to latch the upper byte of the 1802A microprocessor memory address in each machine cycle. The figure below shows the I/O port connected for this application together with its associated timing diagram.





This figure shows 1852 connected as a non-inverting, three state, 8 bit buffer, with MODE = 0, CLOCK = 1 and CS 2 = 1, CS 1 can be used as a tri-state control. When CS 1 = 0, the output is a high impedance, but when CS 1 = 1 data output equals data input. If a high impedance state is not required, the CS 1 input can be tied high (CS 1 = 1).

SIGNAL DESCRIPTION

DI 0-DI 7: These 8 input lines are strobed into an internal buffer by a high level on the Clock input line and latched by the negative transition of the Clock input.

DO 0-DO 7: These 8 output lines reflect the information from the internal buffer when the three state drivers are enabled by CS 1 • CS 2 in the input mode or, at all times, in the output mode.

MODE: This control input sets the 1852 in the input mode with a V_{SS} applied or in the output mode with V_{DD} applied.

CLEAR: This asynchronous reset control clears the buffer register and resets the SR flip flop.

CLOCK: Input Mode: This input strobes data into the buffer when it is activated (high) and sets the SR flip flop (SR = 0) while latching data on its negative transition.

Output Mode: This input along with the chip selects ($\overline{CS1}$ • CS 2 • Clock = 1) strobes data into the buffer. The service request ($\overline{SR}$) is set high on the termination of CS 1 • CS 2 = 1 and reset low on the next negative transition of the clock.

CS 1/$\overline{CS1}$, CS 2: These chip select controls enable device selection.

SR/$\overline{SR}$: This output signal is used as a service request transfer control between the microprocessor and peripheral buses.

Hughes Microelectronics Center
500 Superior Avenue, Box H
Newport Beach, CA 92658-8903
Tele: (714) 759-2727
FAX: (714) 759-2720

12/88
Printed in U.S.A.