INTERSIL

ADVANCE INFORMATION
Specifications Subject to Change Without Notice

IM6504
4096 Bit (4096 x 1) CMOS Static RAM

FEATURES

- **Low Standby Power—275 μW maximum**
- **Low Operating Power—38.5 mW/MHz maximum**
- **High Speed—300 ns Maximum Access Time**
- **TTL Compatible Inputs and Outputs**
- **Three State Outputs**
- **Data Retention to V_{CC} = 2V**
- **On-Chip Address Register**
- **Military and Industrial Temperature Ranges**
- **Harris 6504/Mostek 4104 Compatible**

GENERAL DESCRIPTION

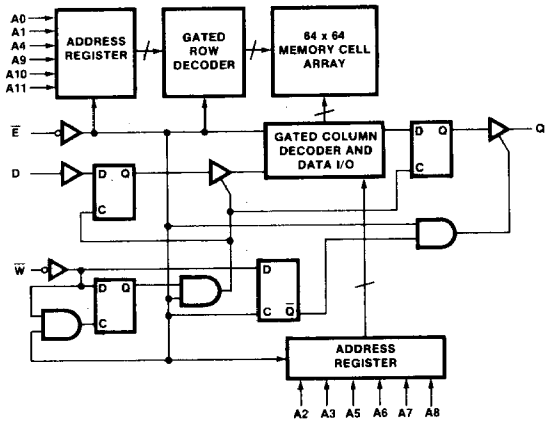
The IM6504 is a high speed, low power CMOS Static RAM organized 4096 words by 1 bit. Input and three state outputs are TTL compatible and allow for direct interface with common system bus structures. An on-chip address register simplifies system interfacing requirements.

This device is fully compatible with the Harris HM6504, but is fabricated with Intersil's selective oxidation, ion-planted, self aligned silicon gate CMOS process, called SELOX C, to achieve higher reliability and performance.

The standard part operates from 4.5 to 5.5 volts with an access time of 300ns and standby supply current of 50μA guaranteed over operating temperature range.

Minimum standby current is drawn when chip select line $\overline{E}$ is held at either V_{CC} or GND. Data rentention is guaranteed to a V_{CC} of 2.0V.

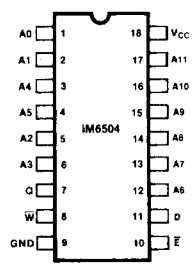
BLOCK DIAGRAM



PIN NAMES

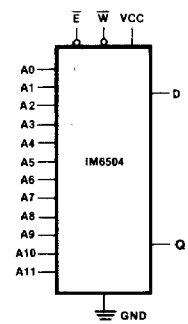
A0-A11	ADDRESS INPUTS
D	DATA INPUT
Q	DATA OUTPUT
$\overline{E}$	ADDR. STROBE/CHIP ENABLE
$\overline{W}$	WRITE ENABLE

PIN CONFIGURATIONS



(outline dwg JN)

LOGIC SYMBOL



ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6504 IJN	18 PIN CERDIP	−40°C to +85°C
IM6504 MJN	18 PIN CERDIP	−55°C to +125°C
IM6504 CJN	18 PIN CERDIP	0°C to +70°C

8

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V_{CC}) ..... +8V
Input or Output Voltage Applied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
  Temperature
    Industrial ..... −40°C to +85°C
    Military ..... −55°C to +125°C
  Voltage
    6504I,M 4.5-5.5V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS:

V_{CC} = 5.0V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logical "1"Input Voltage	V_{IH}		V_{CC}—2.0		V_{CC} +0.3	V
Logical "0" Input Voltage	V_{IL}		−0.3		0.8	
Input Leakage Current	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −1.0mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0mA			0.4	
Output Leakage Current	I_{OLK}	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		0.1	50	
		V_{CC} = 3.0V = $\overline{E}_1$		0.01	25	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0		5.0	7.0	mA
Data Retention Voltage	V_{DR}				2.0	V
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	

Note: Capacitance values guaranteed but not 100% tested.

AC CHARACTERISTICS①

TEST CONDITIONS:

V_{CC} = 5.0V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
Access Time From $\overline{E}$	TELQV		300	ns
Output Disable From $\overline{E}$	TEHQZ		100	
$\overline{E}$ Pulse Width (Pos)	TEHEL	120		
$\overline{E}$ Pulse Width (Neg)	TELEH	300		
Address Setup	TAVEL	20		
Address Hold	TELAX	50		
Write Enable Pulse Width	TWLWH	80		
Data Setup	TDVWL	0		
Data Hold	TWLDX	80		
Write Enable Read Setup	TWHEL	0		
Write Enable Pulse Setup	TWLEH	200		
Early Write Pulse Setup	TWLEL	0		
Early Write Pulse Hold	TELWH	80		
Early Write Data Setup	TDVEL	0		
Early Write Data Hold	TELDX	80		
Data Valid to Write	TQVWL	0		
Read or Write Cycle Time	TELEL	420		

1.) AC Test Conditions: Input rise and fall times are 20 ns; Output load is 1 TTL load and 50 pf. All timing measurements are taken at ½ V_{CC}.

8

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V_{CC}) ..... +8V
Input or Output Voltage Applied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65° to +150°C
Operating Range
Temperature ..... 0°C to +70°C
Voltage ..... 4.75V to 5.25V

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS:

V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logical "1"Input Voltage	V_{IH}		V_{CC}—2.0		V_{CC} +0.3	V
Logical "0" Input Voltage	V_{IL}		−0.3		0.8	
Input Leakage Current	I_{IL}	GND ≤ V_{IN} ≤ V_{CC}	−10.0		+10.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −0.4mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6mA			0.4	
Output Leakage Current	I_{OLK}	GND ≤ V_{IN} ≤ V_{CC}	−10.0		+10.0	
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		100	500	μA
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_0 = 0		5.0	7.0	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	

Note: Capacitance values guaranteed but not 100% tested.

AC CHARACTERISTICS①

TEST CONDITIONS:

V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

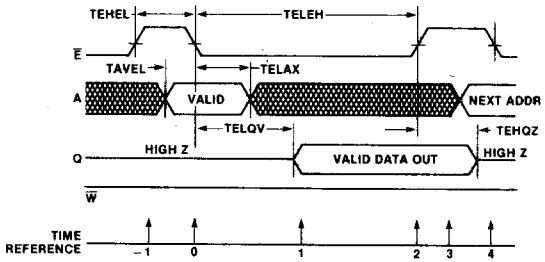
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
Access Time From $\overline{E}$	TELQV		350	ns
Output Disable From $\overline{E}$	TEHQZ		100	
$\overline{E}$ Pulse Width (Pos)	TEHEL	150		
$\overline{E}$ Pulse Width (Neg)	TELEH	350		
Address Setup	TAVEL	20		
Address Hold	TELAX	50		
Write Enable Pulse Width	TWLWH	100		
Data Setup	TDVWL	30		
Data Hold	TWLDX	100		
Write Enable Read Setup	TWHEL	0		
Write Enable Pulse Setup	TWLEH	250		
Early Write Pulse Setup	TWLEL	0		
Early Write Pulse Hold	TELWH	100		
Early Write Data Setup	TDVEL	30		
Early Write Data Hold	TELDX	100		
Data Valid to Write	TQVWL	0		
Read or Write Cycle Time	TELEL	500		

1.) AC Test Conditions: Input rise and fall times are 20 ns; Output load is 1 TTL load and 50 pF. All timing measurements are taken at ½ V_{CC}.

READ CYCLE

The falling edge of chip enable ($\overline{E}$) latches addresses in the on-chip register and initiates a read cycle (T = 0). Addresses to be latched must be present one setup time (TAVEL) prior to and one hold time (TELAX) following the falling edge of $\overline{E}$. During time T = 1 the outputs become valid from the high Z state. There is no period of active, but invalid, data on the bus. Write enable ($\overline{W}$) must remain high until after time T = 2. The read cycle is terminated when $\overline{E}$ goes high, disabling the output buffers.

TIMING



FUNCTION TABLE • READ

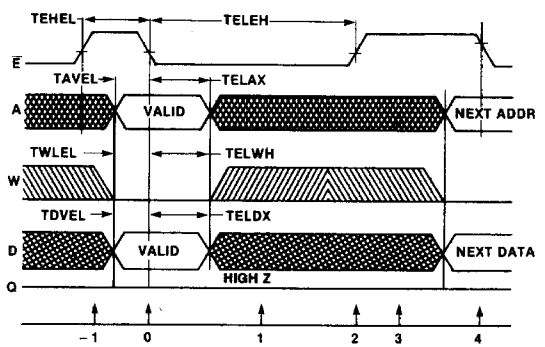
TIME REF	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	OUTPUT Q	NOTES
-1	H	X	X	Z	MEMORY INACTIVE
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	V	OUTPUT VALID
2	↗	H	X	V	READ COMPLETE
3	H	X	X	V	MEMORY INACTIVE (SAME AS -1)
4	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAMES AS 0)

EARLY WRITE CYCLE

The falling edge of $\overline{E}$ latches addresses in the on-chip register and initiates an early write cycle. Address, $\overline{W}$ and D inputs must be present for the appropriate setup and hold times prior to and following the falling edge of $\overline{E}$. The early write operation is complete at T = 2, after one minimum negative $\overline{E}$ pulse width (TELEH).

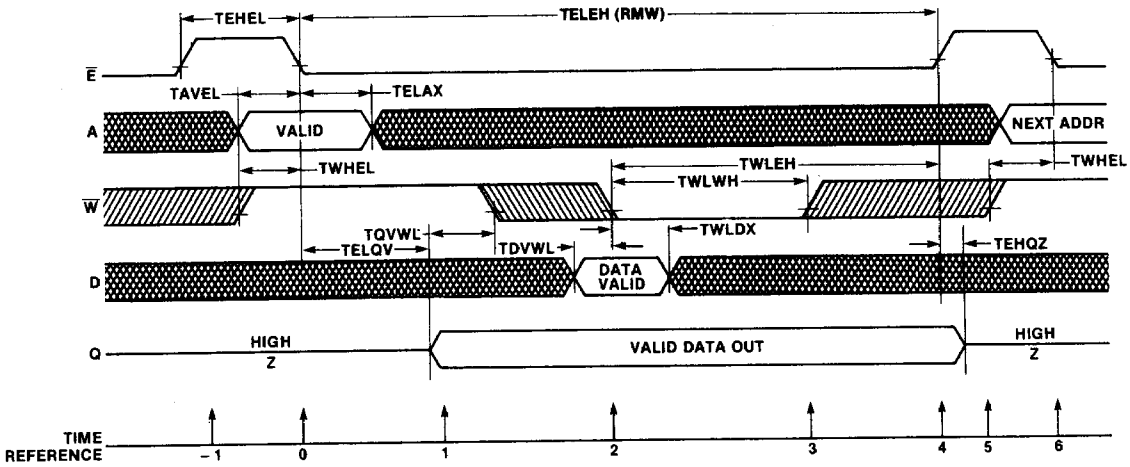
During the early write cycle, output data line Q remains in a high impedance state.

TIMING



FUNCTION TABLE • EARLY WRITE

TIME REF		INPUTS $\overline{W}$	INPUTS A	INPUTS D	Q	NOTES
-1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS
2	↗	X	X	X	Z	WRITE COMPLETE
3	H	X	X	X	Z	CYCLE ENDS, MEMORY INACTIVE (SAME AS -1)
4	↘	L	V	V	Z	NEXT CYCLE BEGINS (SAME AS 0)



READ — MODIFY — WRITE CYCLE

A read - modify - write cycle may be performed if the write portion of the cycle is controlled by $\overline{W}$, and $\overline{E}$ remains low throughout. Data is read normally, with $\overline{W}$ held high, address inputs latched at T = 0 and Q data out valid at T = 1. A data out valid to write time (TQVWL) must be observed before $\overline{W}$ is brought low to begin the write portion of the cycle.

Input Data must be valid a setup time prior to (TDVWL) and a hold time following (TWLDX) the falling edge of $\overline{W}$. At time T = 3 $\overline{W}$ is returned high, and at T = 4 $\overline{E}$ is returned high to complete the cycle. The output Q is disabled by $\overline{E}$ and goes to a high impedance state an output disable time (TEHQZ) after $\overline{E}$ is returned high (T = 5).

FUNCTION TABLE • READY—MODIFY—WRITE

TIME REF.	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	NOTES
-1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	X	V	OUTPUT VALID, READ/MODIFY TIME
2	L	↘	X	V	V	WRITE BEGINS, DATA LATCHED
3	L	↗	X	X	V	WRITE IN PROGRESS
4	↗	X	X	X	V	WRITE COMPLETE
5	H	X	X	X	Z	MEMORY INACTIVE (SAME AS -1)
6	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

8

POWER DOWN SEQUENCE

The power down sequence begins at T = 0 with $\overline{E}$ held at a logic high level and all addresses, D and $\overline{W}$ established at valid logic levels. Chip enable $\overline{E}$ must be high one minimum positive pulse width (TEHEL) before power-down. At T = 1 power supply V_{CC} may be decreased to minimum V_{CCDR}. As V_{CC} is decreased, $\overline{E}$ must remain within data retention high logic level threshold limits (V_{IHDR}), and $\overline{W}$ and A_0-A_9, must remain within V_{IHDR} or V_{IL} limits. Failure to remain within these limits may cause data loss or SCR latch-up.

The same conditions must be met, in reverse, when returning to normal power (T = 2,3).

POWER DOWN SEQUENCE