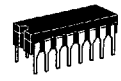
Dual Type D Master-Slave Flip-Flop

MC10131

The MC10131 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip–flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip–flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.



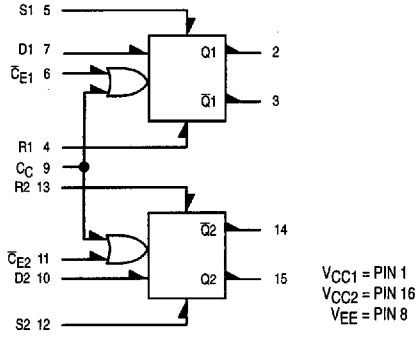
L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

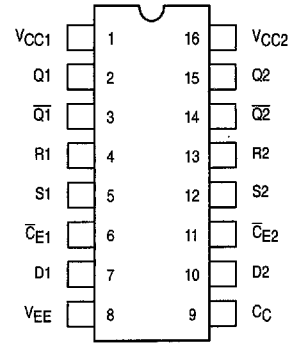
FN SUFFIX
PLCC
CASE 775–02

P_D = 235 mW typ/pkg (No Load)
F_{Tog} = 160 MHz typ
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

C = C_E + C_C. A clock H is a clock transition from a low to a high state.

R–S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		62		45	56		62	mAdc
Input Current	I_{inH}	4 5 6 7 9		525 525 350 390 425			330 330 220 245 265		330 330 220 245 265	µAdc
	I_{inL}	4, 5* 6, 7, 9*	0.5 0.5		0.5 0.5			0.3 0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 2†	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3†	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2†	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3†		−1.655 −1.655			−1.630 −1.630		−1.595 −1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t_{9+2-} t_{9+2+} t_{6+2+} t_{6+2-}	2 2 2 2	1.7 1.7 1.7 1.7	4.6 4.6 4.6 4.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	4.5 4.5 4.5 4.5	1.8 1.8 1.8 1.8	5.0 5.0 5.0 5.0	
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Set Input										ns
Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14	1.7 1.7 1.7 1.7	4.4 4.4 4.4 4.4	1.8 1.8 1.8 1.8	2.8 2.8 2.8 2.8	4.3 4.3 4.3 4.3	1.8 1.8 1.8 1.8	4.8 4.8 4.8 4.8	
Reset Input										ns
Propagation Delay	t_{4+2-} t_{13+15-} t_{4+3-} t_{13+14+}	2 15 3 14	1.7 1.7 1.7 1.7	4.4 4.4 4.4 4.4	1.8 1.8 1.8 1.8	2.8 2.8 2.8 2.8	4.3 4.3 4.3 4.3	1.8 1.8 1.8 1.8	4.8 4.8 4.8 4.8	
Setup Time	t_{setup}	7	2.5		2.5			2.5		ns
Hold Time	t_{hold}	7	1.5		1.5			1.5		ns
Toggle Frequency (Max)	f_{tog}	2	125		125	160		125		MHz

* Individually test each input applying V_{IH} or V_{IL} to input under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)

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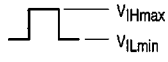
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
		5	5				8	1, 16
		6	6				8	1, 16
		7	7				8	1, 16
		9	9				8	1, 16
	I_{inL}	4, 5*		*			8	1, 16
		6, 7, 9*		*			8	1, 16
Output Voltage Logic 1	V_{OH}	2	5				8	1, 16
		2†	7				8	1, 16
Output Voltage Logic 0	V_{OL}	2	5				8	1, 16
		3†	7				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2			5		8	1, 16
		2†			7	9	8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2			5		8	1, 16
		3†			7	9	8	1, 16
Switching Times (50Ω Load) Clock Input			+1.11Vdc		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{9+2-}	2			9	2	8	1, 16
	t_{9+2+}	2	7		9	2	8	1, 16
	t_{6+2+}	2	7		6	2	8	1, 16
	t_{6+2-}	2			6	2	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2	7		9	2	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			9	2	8	1, 16
Set Input								
Propagation Delay	t_{5+2+}	2			5	2	8	1, 16
	t_{12+15+}	15	6		12	15	8	1, 16
	t_{5+3-}	3			5	3	8	1, 16
	t_{12+14-}	14	9		12	14	8	1, 16
Reset Input								
Propagation Delay	t_{4+2-}	2			4	2	8	1, 16
	t_{13+15-}	15	6		13	15	8	1, 16
	t_{4+3-}	3			4	3	8	1, 16
	t_{13+14+}	14	9		13	14	8	1, 16
Setup Time	t_{setup}	7			6, 7	2	8	1, 16
Hold Time	t_{hold}	7			6, 7	2	8	1, 16
Toggle Frequency (Max)	f_{tog}	2			6	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.