# 4-bit binary counter | 74ALS161B/74ALS163B

*74ALS161B 4-bit binary counter, asynchronous reset*
*74ALS163B 4-bit binary counter, synchronous reset*

## FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset (74ALS161B)
- Synchronous reset (74ALS163B)
- High speed synchronous expansion
- Typical count rate of 140MHz

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74ALS161B | 140MHz | 10mA |
| 74ALS163B | 140MHz | 10mA |

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | DRAWING NUMBER |
|---|---|---|
| | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = 0°C to +70°C | |
| 16-pin plastic DIP | 74ALS161BN, 74ALS163BN | SOT38-4 |
| 16-pin plastic SO | 74ALS161BD, 74ALS163BD | SOT109-1 |
| 16-pin plastic SSOP Type II | 74ALS161BDB, 74ALS163BDB | SOT338-1 |

## DESCRIPTION

Synchronous presettable 4-bit binary counters (74ALS161B, 74ALS163B) feature an internal carry look-ahead and can be used for high speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the parallel enable ($\overline{PE}$) input disables the counting action and causes the data at the D0 – D3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable (CEP, CET) inputs.

A Low level at the master reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q0 – Q3) in 74ALS161B to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 74ALS163B the clear function is synchronous. A Low level at the synchronous reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q0 – Q3) to Low levels after the next positive-going transition on the clock (CP) input ( provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1).

The carry look-ahead simplifies serial cascading of the counters. Both count enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q0. This pulse can be used to enable the next cascaded stage (see Figure 2).

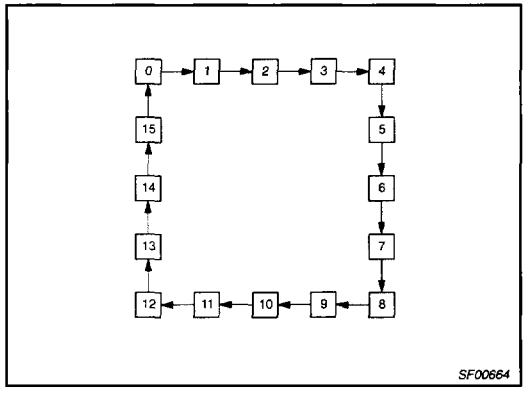
The TC output is subjected to decoding spikes due to internal race conditions, Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74ALS (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| D0 – D3 | Data inputs | 1.0/1.0 | 20µA/0.1mA |
| CEP | Count enable parallel input (active-Low) | 1.0/1.0 | 20µA/0.1mA |
| CET | Count enable trickle input (active-Low) | 1.0/1.0 | 20µA/0.1mA |
| CP | Clock input (active rising edge) | 1.0/1.0 | 20µA/0.1mA |
| $\overline{PE}$ | Parallel enable input (active-Low) | 1.0/1.0 | 20µA/0.1mA |
| $\overline{MR}$ | Asynchronous master reset input (active-Low) for 74ALS161B | 1.0/1.0 | 20µA/0.1mA |
| $\overline{SR}$ | Asynchronous reset input (active-Low) for 74ALS163B | 1.0/1.0 | 20µA/0.1mA |
| Q0 – Q3 | Flip-flop outputs | 20/80 | 0.4mA/8mA |
| TC | Terminal count output (active-Low) | 20/80 | 0.4mA/8mA |

**NOTE:** One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

## STATE DIAGRAM




## APPLICATIONS

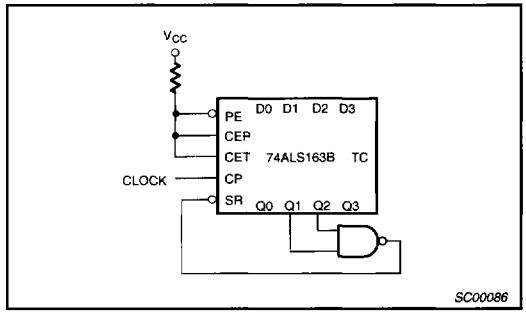



**Figure 1. Maximum Count Modifying Scheme**
**Terminal Count = 6**

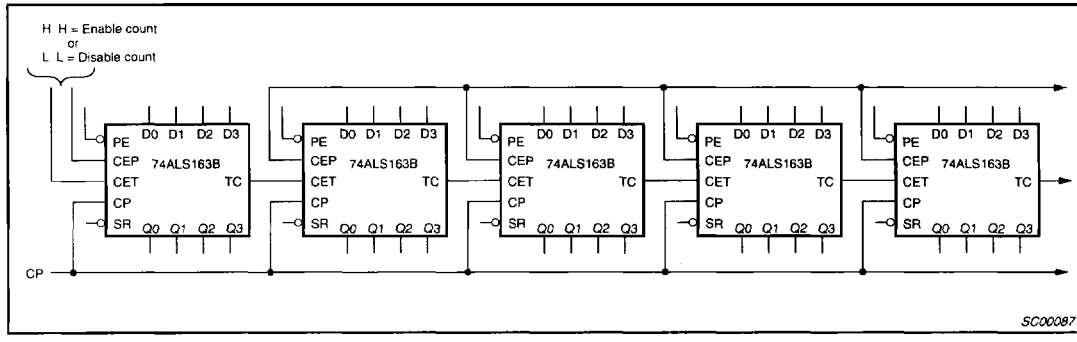
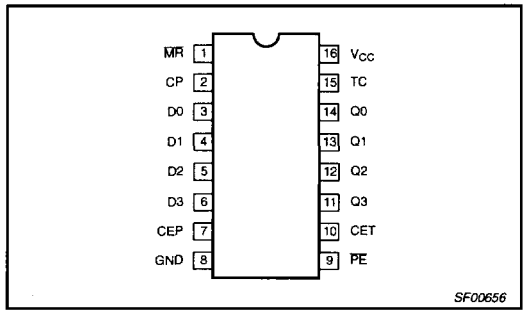
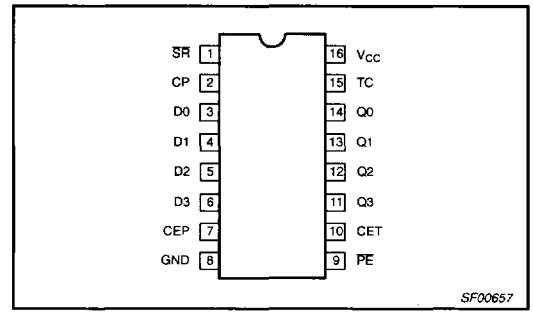



**Figure 2. Synchronous Multistage Counting Scheme**

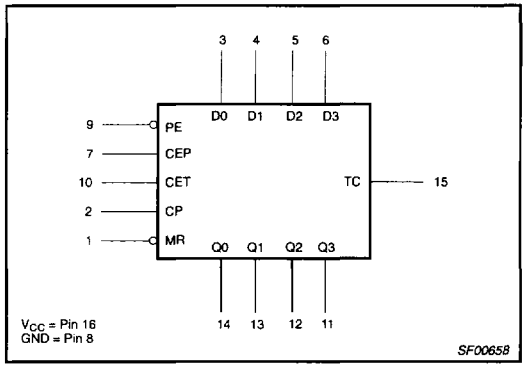
## PIN CONFIGURATION – 74ALS161B



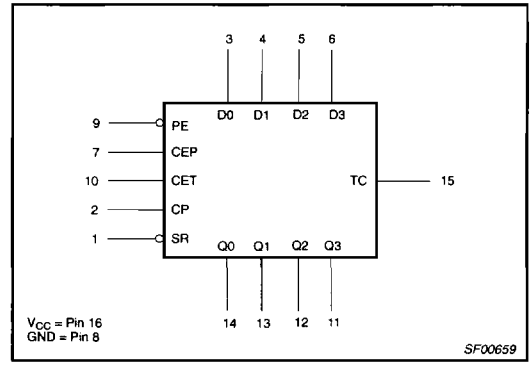

## PIN CONFIGURATION – 74ALS163B



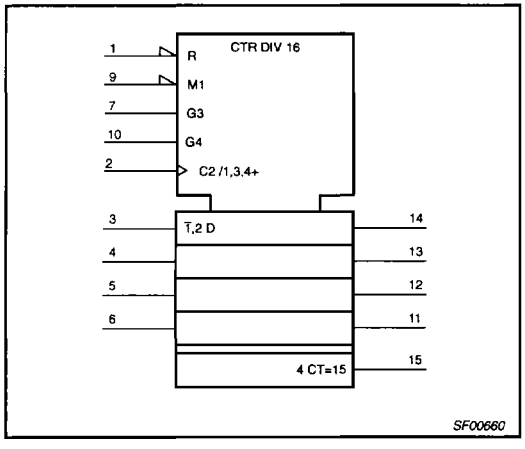

## LOGIC SYMBOL – 74ALS161B



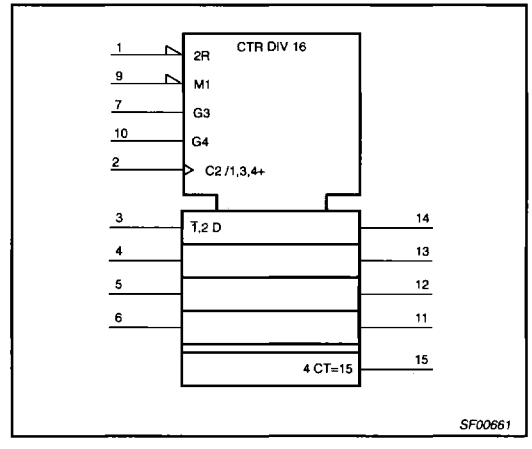

## LOGIC SYMBOL – 74ALS163B



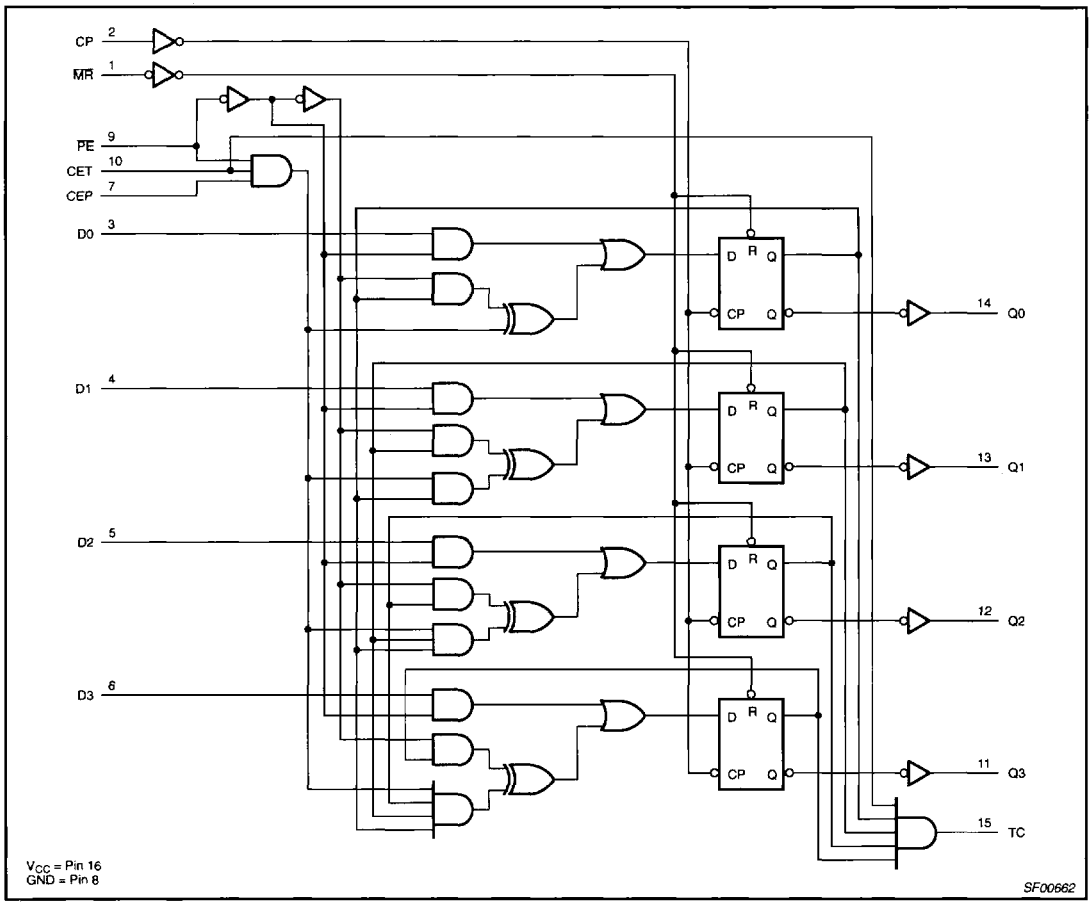

## IEC/IEEE SYMBOL – 74ALS161B




## IEC/IEEE SYMBOL – 74ALS163B



## LOGIC DIAGRAM – 74ALS161B

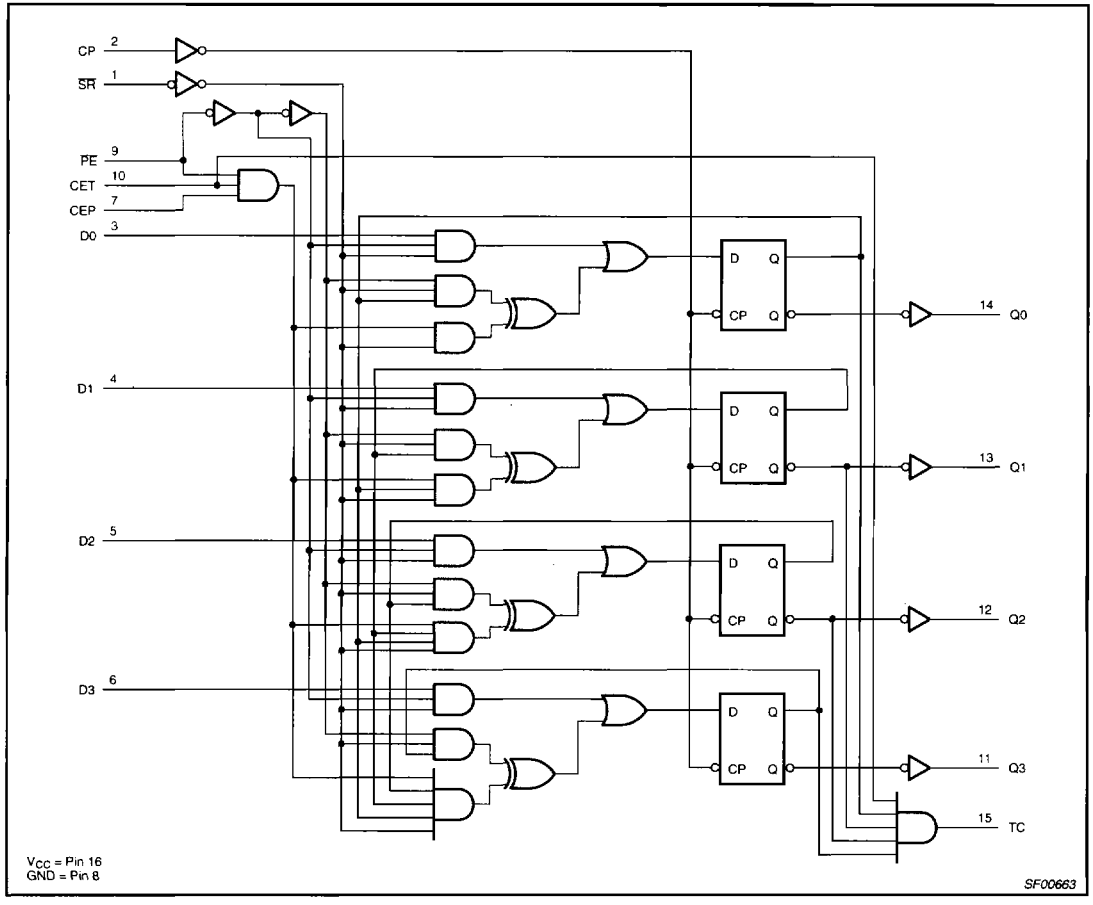



## MODE SELECTION FUNCTION TABLE – 74ALS161B

| INPUTS | | | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|
| $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | Dn | Qn | TC | |
| L | X | X | X | X | X | L | L | Reset (clear) |
| H | ↑ | X | X | l | l | L | L | Parallel load |
| H | ↑ | X | X | l | h | H | (a) | |
| H | ↑ | h | h | h | X | count | (a) | Count |
| h | X | l | X | h | X | qn | (a) | Hold (do nothing) |
| h | X | X | l | h | X | qn | L | |

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
qn = *Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition*
X = Don't care
(a) = The output is High when CET is High and the counter is at terminal count (HHHH)
↑ = Low-to-High clock transition

## LOGIC DIAGRAM – 74ALS163B




## MODE SELECTION FUNCTION TABLE – 74ALS163B

| INPUTS | | | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|
| $\overline{SR}$ | CP | CEP | CET | $\overline{PE}$ | Dn | Qn | TC | |
| l | ↑ | X | X | X | X | L | L | Reset (clear) |
| h | ↑ | X | X | l | l | L | L | Parallel load |
| h | ↑ | X | X | l | h | H | (a) | |
| h | ↑ | h | h | h | X | count | (a) | Count |
| h | X | l | X | h | X | qn | (a) | Hold (do nothing) |
| h | X | X | l | h | X | qn | L | |

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
qn = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
(a) = The output is High when CET is High and the counter is at terminal count (HHHH)
↑ = Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | −0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | −0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | 16 | mA |
| $T_{amb}$ | Operating free-air temperature range | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature range | −65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 8 | mA |
| $T_{amb}$ | Operating free-air temperature range | 0 | | +70 | °C |

## DC ELECTRICAL CHARACTERISTICS

*(Over recommended operating free-air temperature range unless otherwise noted.)*

| SYMBOL | PARAMETER | TEST CONDITIONS[1] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP[2] | MAX | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = ±10%, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OH}$ = −0.4mA | $V_{CC}$ − 2 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = 4mA | | 0.25 | 0.40 | V |
| | | | $I_{OL}$ = 8mA | | 0.35 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | −0.73 | −1.5 | V |
| $I_I$ | Input current at minimum input voltage | $V_{CC}$ = MAX, $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | | −0.1 | mA |
| $I_O$ | Output current[3] | $V_{CC}$ = MAX, $V_O$ = 2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current (total) | $V_{CC}$ = MAX | | | 10 | 21 | mA |

**NOTES:**

1. *For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.*
2. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## AC ELECTRICAL CHARACTERISTICS

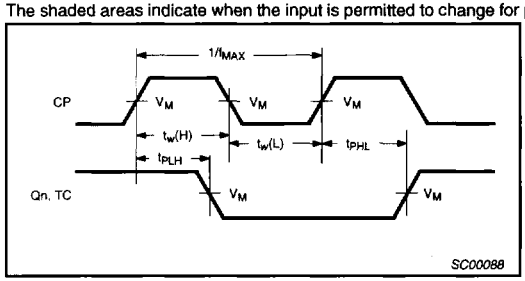
| SYMBOL | PARAMETER | | TEST CONDITION | LIMITS $T_{amb}$ = 0°C to +70°C $V_{CC}$ = +5.0V ± 10% $C_L$ = 50pF, $R_L$ = 500Ω | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| $f_{MAX}$ | Maximum clock frequency | | Waveform 1 | 100 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to Qn | | Waveform 1 | 4.0<br>6.0 | 13.0<br>16.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to TC | | Waveform 1 | 6.0<br>8.0 | 16.0<br>16.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CET to TC | | Waveform 2 | 3.0<br>3.0 | 10.0<br>10.0 | ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to Qn | 74ALS161B | Waveform 3 | 8.0 | 15.0 | ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to TC | 74ALS163B | Waveform 3 | 11.0 | 19.0 | ns |

## AC ELECTRICAL CHARACTERISTICS

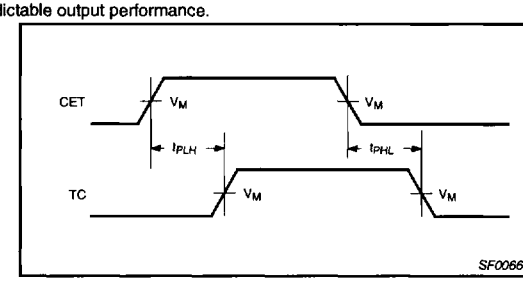
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS $T_{amb}$ = 0°C to +70°C $V_{CC}$ = +5.0V ± 10% $C_L$ = 50pF, $R_L$ = 500Ω | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{su}(H)$<br>$t_{su}(L)$ | Setup time, High or Low<br>Dn to CP | Waveform 6 | 8.0<br>8.0 | | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold time, High or Low<br>Dn to CP | Waveform 6 | 0.0<br>0.0 | | ns |
| $t_{su}(H)$<br>$t_{su}(L)$ | Setup time, High or Low<br>$\overline{PE}$ or $\overline{SR}$ to CP | Waveform 5 or 6 | 10.0<br>10.0 | | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold time, High or Low<br>$\overline{PE}$ or $\overline{SR}$ to CP | Waveform 6 | 0.0<br>0.0 | | ns |
| $t_{su}(H)$<br>$t_{su}(L)$ | Setup time, High or Low<br>CET or CEP to CP | Waveform 4 | 10.0<br>10.0 | | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold time, High or Low<br>CET or CEP to CP | Waveform 4 | 0.0<br>0.0 | | ns |
| $t_w(H)$<br>$t_w(L)$ | CP Pulse width (load),<br>High or Low | Waveform 1 | 5.0<br>5.0 | | ns |
| $t_w(H)$<br>$t_w(L)$ | CP Pulse width (count),<br>High or Low | Waveform 1 | 5.0<br>5.0 | | ns |
| $t_w(L)$ | $\overline{MR}$ or $\overline{SR}$ Pulse width, Low | Waveform 3 | 5.0 | | ns |
| $t_{REC}$ | Recovery time, $\overline{CR}$ or $\overline{SR}$ to CP | Waveform 3 | 10.0 | | ns |

## AC WAVEFORMS

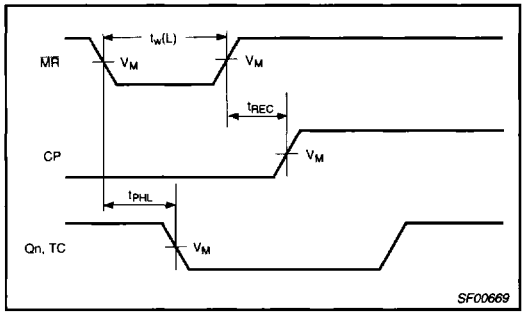
For all waveforms, $V_M$ = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



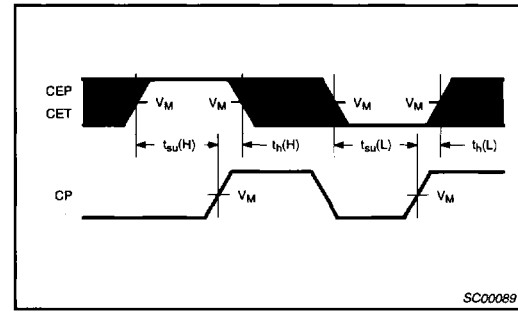

**Waveform 1. Propagation Delay for Clock Input to Output, Clock PUlse Width, and Maximum Clock Frequency**



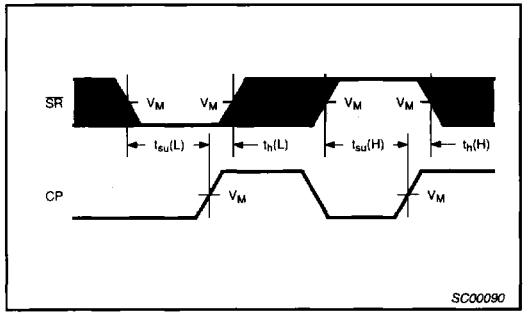

**Waveform 2. Propagation Delay for CET to TC Output**



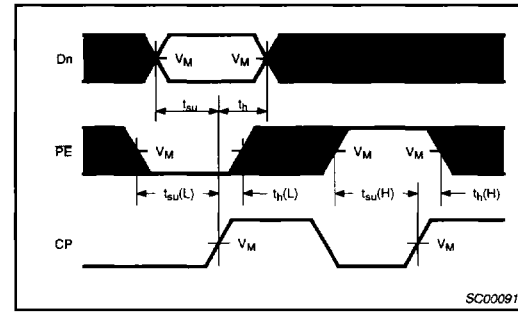

**Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time**




**Waveform 4. CEP and CET Setup and Hold Times**

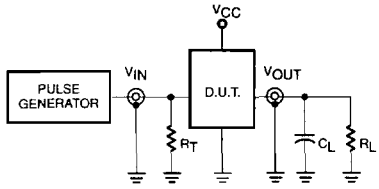



**Waveform 5. Synchronous Reset Setup and Hold Times**

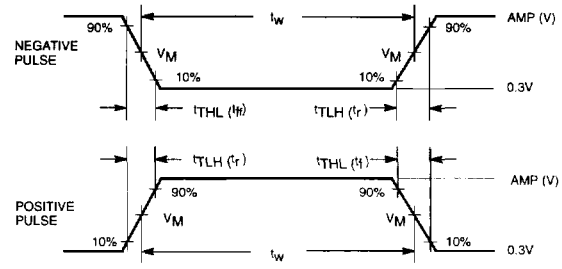



**Waveform 6. Data and Parallel Enable Setup and Hold Times**

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for Totem-pole Outputs**




**Input Pulse Definition**

| Family | INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|---|
| | Amplitude | $V_M$ | Rep.Rate | $t_w$ | $t_{TLH}$ | $t_{THL}$ |
| 74ALS | 3.5V | 1.3V | 1MHz | 500ns | 2.0ns | 2.0ns |

**DEFINITIONS:**

$R_L$ = Load resistor; see AC electrical characteristics for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

SC00005