Comlinear
A National Semiconductor Company

Dual Wideband, Low-Noise, Voltage-Feedback Op Amp

CLC428

APPLICATIONS:

- General purpose dual op amp
- Low noise integrators
- Low noise active filters
- Diff-in/diff-out instrumentation amp
- Driver/receiver for transmission systems
- High-speed detectors
- I/Q channel amplifiers

FEATURES:

- Wide unity-gain bandwidth: 160MHz
- Ultra-low noise: 2.0nV/√Hz
- Low distortion: -78dBc 2nd (2MHz)
  -62/-72dBc (10MHz)
- Settling time: 16ns to 0.1%
- Supply voltage range: ±2.5 to ±5 or single supply
- High output current: ±80mA

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DESCRIPTION

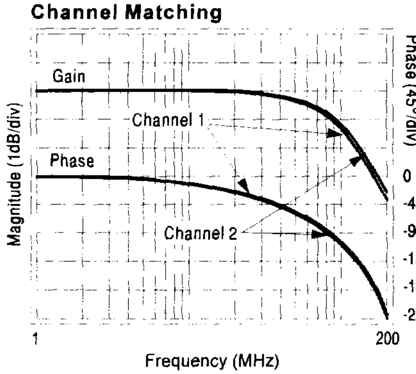
The CLC428 is a very high-speed dual op amp that offers a traditional voltage-feedback topology featuring unity-gain stability and slew-enhanced circuitry. The CLC428's ultra low noise and very low harmonic distortion combine to form a very wide dynamic-range op amp that operates from a single (5 to 12V) or dual (±5V) power supply.

Each of the CLC428's closely matched channels provides a 160MHz unity-gain bandwidth with an ultra low input voltage noise density (2nV/√Hz). Very low 2nd/3rd harmonic distortion (-62/-72dBc) as well as high channel-to-channel isolation (-62dB) make the CLC428 a perfect wide dynamic-range amplifier for matched I/Q channels.

With its fast and accurate settling (16ns to 0.1%), the CLC428 is also a excellent choice for wide-dynamic range, anti-aliasing filters to buffer the inputs of hi-resolution analog-to-digital converters. Combining the CLC428's two tightly-matched amplifiers in a single eight-pin SOIC reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

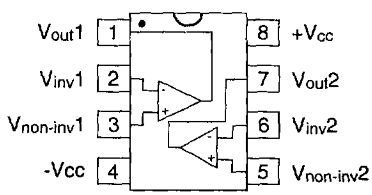
To reduce design times and assist in board layout, the CLC428 is supported by an evaluation board and a SPICE simulation model available from Comlinear.

Channel Matching



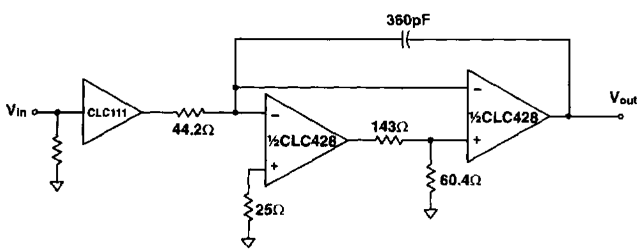
PINOUT

DIP & SOIC

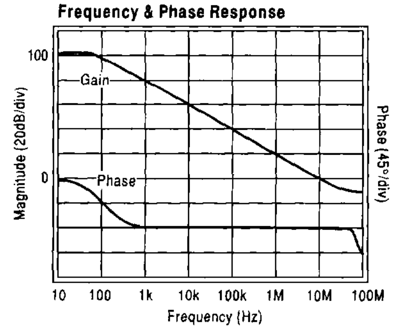


TYPICAL APPLICATION

5-Decade Integrator



Frequency & Phase Response



CLC428 Electrical Characteristics (V_{CC} = ±5V; A_v = +2V/V; R_f =100Ω; R_g =100Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC428	+25°C	+25°C	0 to +70°C	-40 to +85°C		
FREQUENCY DOMAIN RESPONSE							
gain bandwidth product	V_{out} < 0.5V_{pp}	135	100	80	70	MHz	
-3dB bandwidth, Av=+1	V_{out} < 0.5V_{pp}	160	120	90	80	MHz	
Av=+2	V_{out} < 0.5V_{pp}	80	50	40	35	MHz	B,1
	V_{out} < 5.0V_{pp}	40	25	22	20	MHz	
gain flatness	V_{out} < 0.5V_{pp}						
peaking	DC to 200MHz	0.0	0.6	0.8	1.0	dB	B,1
rolloff	DC to 20MHz	0.05	0.5	0.7	0.7	dB	B,1
linear phase deviation	DC to 20MHz	0.2	1.0	1.5	1.5	°	
TIME DOMAIN RESPONSE							
rise and fall time	1V step	5.5	7.5	9.0	10.0	ns	
settling time	2V step to 0.1%	16	20	24	24	ns	
overshoot	1V step	1	5	10	10	%	
slew rate	5V step	500	300	275	250	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	1V_{pp},10MHz	- 62	- 50	- 45	- 43	dBc	B
3rd harmonic distortion	1V_{pp},10MHz	- 72	- 60	- 56	- 56	dBc	B
equivalent input noise							
voltage	1MHz to 100MHz	2.0	2.5	2.8	2.8	nV/√Hz	
current	1MHz to 100MHz	2.0	3.0	3.6	4.6	pA/√Hz	
crosstalk	input referred, 10MHz	- 62	- 58	- 58	- 58	dB	
STATIC DC PERFORMANCE							
open-loop gain		60	56	50	50	dB	
input offset voltage		1.0	2.0	3.0	3.5	mV	A
average drift		5	---	15	20	µV/°C	
input bias current		1.5	25	40	65	µA	A
average drift		150	---	600	700	nA/°C	
input offset current		0.3	3	5	5	µA	
average drift		5	---	25	50	nA/°C	
power supply rejection ratio		66	60	55	55	dB	B
common-mode rejection ratio		63	57	52	52	dB	
supply current	per channel, R_L= ∞	11	12	13	15	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	500	250	125	125	kΩ	
	differential-mode	200	50	25	25	kΩ	
input capacitance	common-mode	2.0	3.0	3.0	3.0	pF	
	differential-mode	2.0	3.0	3.0	3.0	pF	
output resistance	closed loop	0.05	0.1	0.2	0.2	Ω	
output voltage range	R_L= ∞	± 3.8	± 3.5	± 3.3	± 3.3	V	
	R_L=100Ω	± 3.5	± 3.2	± 2.6	± 1.3	V	
input voltage range	common mode	± 3.7	± 3.5	± 3.3	± 3.3	V	
output current		± 80	± 50	± 40	± 20	mA	

Absolute Maximum Ratings

supply voltage	±7V
short circuit current	(note 2)
common-mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+200°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
L-level: spec is 100% wafer probed at 25°C.
B) J-level: spec is sample tested at 25°C.
1) Spec is guaranteed at 0.5Vpp but tested at 0.1Vpp.
2) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 200mA.

Ordering Information

Model	Temperature Range	Description
CLC428AJP	-40°C to +85°C	8-pin PDIP
CLC428AJE	-40°C to +85°C	8-pin SOIC
CLC428ALC	-40°C to +85°C	dice
CLC428A8B*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC428AMC*	-55°C to +125°C	dice, MIL-STD-883
CLC428AIB*	-40°C to +85°C	8-pin CerDIP
5962-9470801MPA*	-55°C to +125°C	DESC SMD

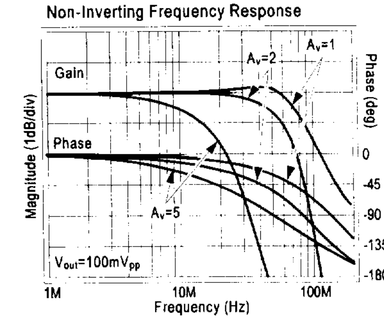
*See CLC428 MIL-883 Data Sheet for Specifications

Package Thermal Resistance

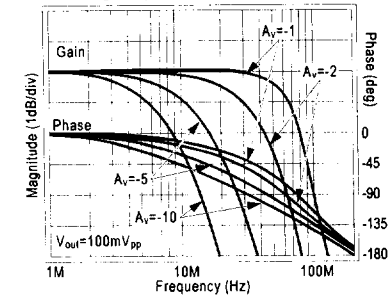
Package	θ_{jc}	θ_{jA}
Plastic (AJP)	75°/W	90°/W
Surface Mount (AJE)	90°/W	105°/W

CLC428 Typical Performance (TA=+25°C, AV=+2, VCC=±5V, Rf=100Ω, RL=100Ω, unless noted)

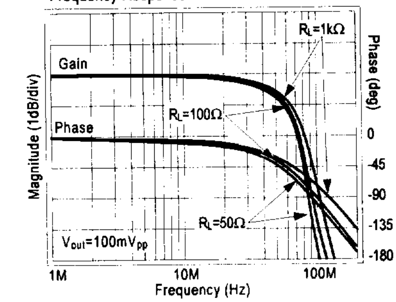
Non-Inverting Frequency Response



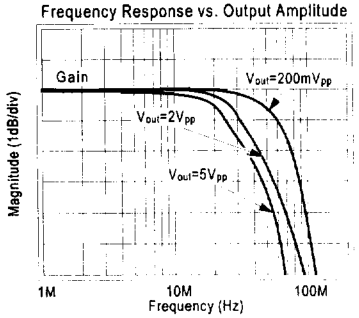
Inverting Frequency Response



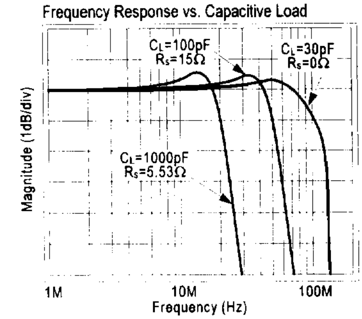
Frequency Response vs. Load Resistance



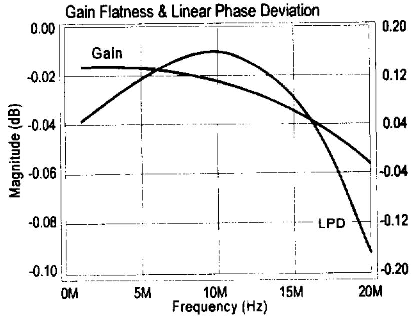
Frequency Response vs. Output Amplitude



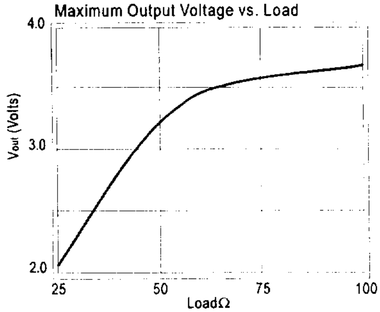
Frequency Response vs. Capacitive Load



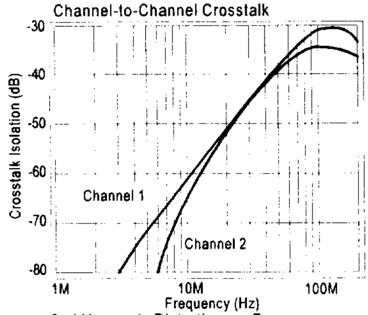
Gain Flatness & Linear Phase Deviation



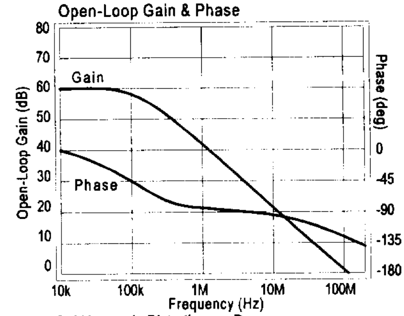
Maximum Output Voltage vs. Load



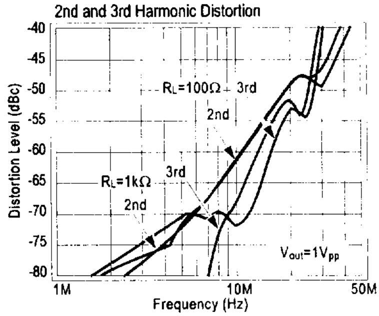
Channel-to-Channel Crosstalk



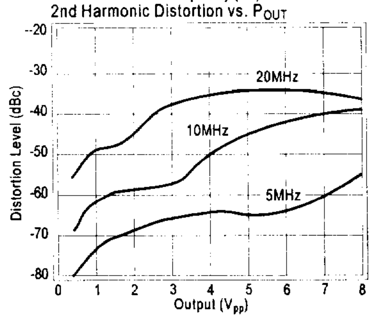
Open-Loop Gain & Phase



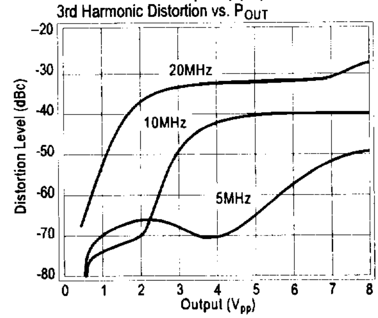
2nd and 3rd Harmonic Distortion



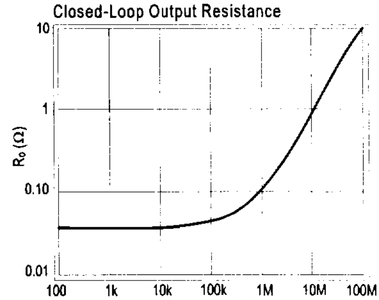
2nd Harmonic Distortion vs. POUT



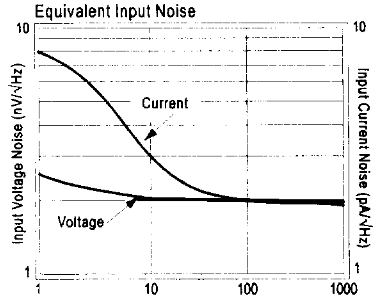
3rd Harmonic Distortion vs. POUT



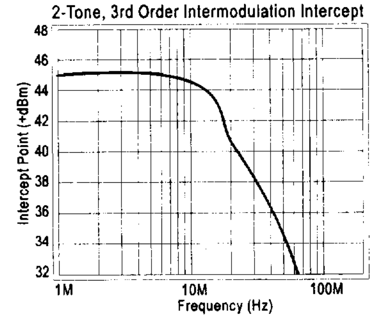
Closed-Loop Output Resistance



Equivalent Input Noise

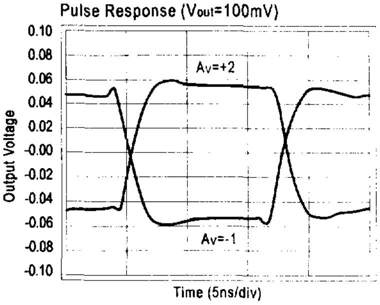


2-Tone, 3rd Order Intermodulation Intercept

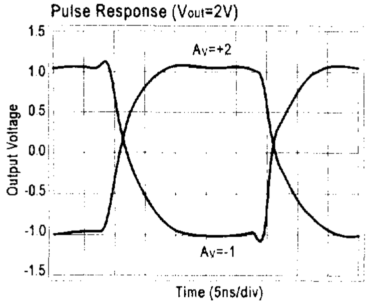


CLC428 Typical Performance (T_A=+25 C, A_V=+2, V_{CC}=±5V, R_f=100Ω, R_L=100Ω, unless noted)

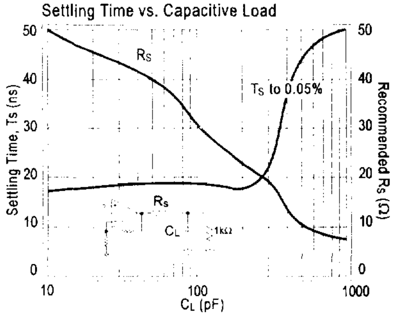
Pulse Response (V_{out}=100mV)



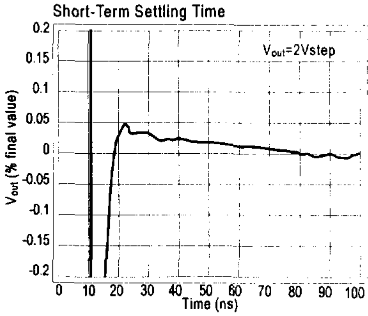
Pulse Response (V_{out}=2V)



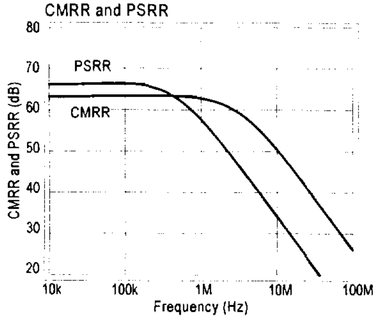
Settling Time vs. Capacitive Load



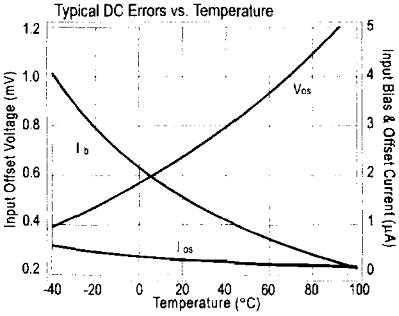
Short-Term Settling Time



CMRR and PSRR



Typical DC Errors vs. Temperature



Application Discussion

Low Noise Design

Ultimate low noise performance from circuit designs using the CLC428 requires the proper selection of external resistors. By selecting appropriate low-valued resistors for R_f and R_g, amplifier circuits using the CLC428 can achieve output noise that is approximately the equivalent voltage input noise of 2.0 nV/√Hz multiplied by the desired gain (Av).

Each amplifier in the CLC428 has an equivalent input noise resistance which is optimum for matching source impedances of approximately 1k. Using a transformer, any source can be matched to achieve the lowest noise design.

For even lower noise performance than the CLC428, consider the CLC425 or CLC426 at 1.05 and 1.6 nV/√Hz, respectively.

DC Bias Currents and Offset Voltages

Cancellation of the output offset voltage due to input bias currents is possible with the CLC428. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (Vos) multiplied by the desired gain (Av). Comlinear Application Note OA-7 offers several solutions to further reduce the output offset.

Output and Supply Considerations

With ±5V supplies, the CLC428 is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the CLC428's output current capability, typically 80mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled "Settling Time vs. Capacitive Load" in the Typical Performance section.

Layout

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be place as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. Comlinear suggests the 730036 (through-hole) or the 730027 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

Analog Delay Circuit (All-Pass Network)

The circuit in Figure 1 implements an all-pass network using the CLC428. A wide bandwidth buffer (CLC111) drives the circuit and provides a high input impedence for the source. As shown in Figure 2, the circuit provides a

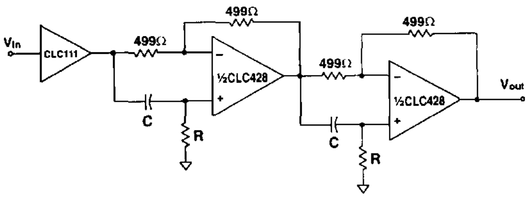


Figure 1

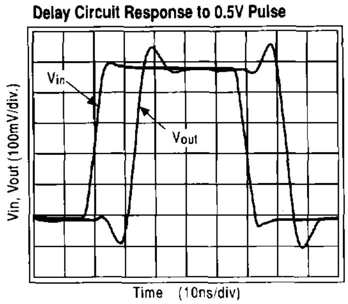


Figure 2

13.1ns delay (with R =40.2Ω, C=47pF). R_f and R_g should be of equal and low value for parasitic insensitive operation. The circuit gain is +1 and the delay is determined by the following equations.

$$\tau_{delay} = 2(2RC + T_d) \qquad \text{Eq. 1}$$

$$T_d = \frac{1}{360}\frac{d\phi}{df}; \qquad \text{Eq. 2}$$

where T_d is the delay of the op amp at A_V=+1. The CLC428 provides a typical delay of 2.8ns at its -3dB point.

Full Duplex Digital or Analog Transmission

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The CLC428's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 3, one of the CLC428's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms differential amplifier for the signals transmitted by driver A_1 (B_1). If the coax cable is lossless and R_f equals R_g, receiver A_2 (B_2) will then reject the signals from driver

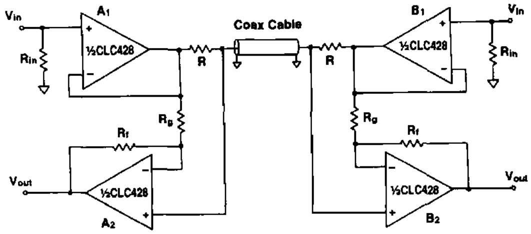


Figure 3

A_1 (B_1) and pass the signals from driver B_1 (A_1). The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2}V_{in_{A(B)}}\left(1-\frac{R_f}{R_g}\right)+\frac{1}{2}V_{in_{B(A)}}\left(1+\frac{R_f}{R_g}\right) \qquad \text{Eq. 3}$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 4 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

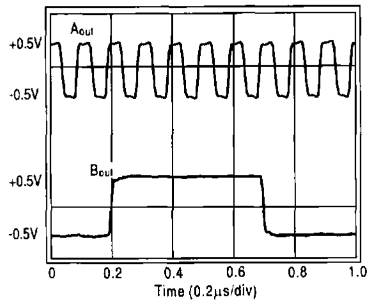


Figure 4

Five Decade Integrator

A composite integrator, as shown in Figure 5, uses the CLC428 dual op amp to increase the circuits' usable frequency range of operation. The transfer function of this circuit is:

$$V_o = \frac{1}{RC}\int V_{in}dt \qquad \text{Eq. 4}$$

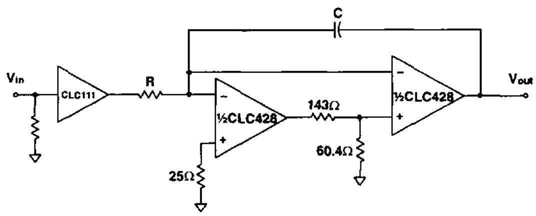


Figure 5

A resistive divider made from the 143Ω and 60.4Ω resistors was chosen to reduce the loop-gain and stabilize the network. The CLC428 composite integrator provides integration over five decades of operation. R and C set the integrator's gain. Figure 6 shows the frequency and phase response of the circuit in Figure 5 with R=44.2Ω and C=360pF.

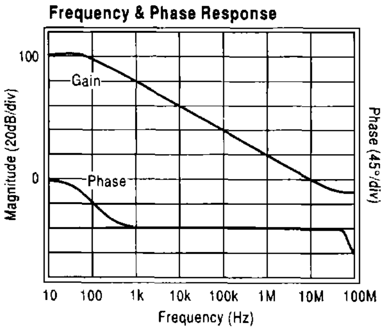


Figure 6

Positive Peak Detector

The CLC428's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 7.

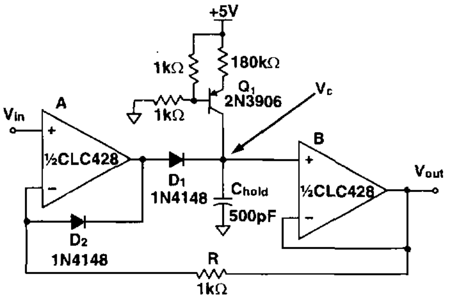


Figure 7

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the of the circuit's performance is shown in Figure 8 with a 1MHz sinusoidal input.

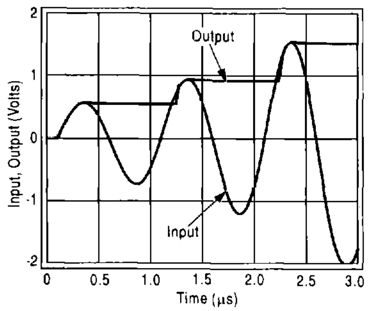


Figure 8

A current source, built around Q_1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D_2 prevents negative saturation when V_{in} is less than V_c. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

Adjustable or Bandpass Equalizer

A "boost" equalizer can be made with the CLC428 by summing a bandpass response with the input signal, as shown in Figure 9.

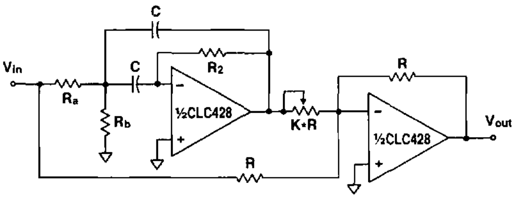


Figure 9

The overall transfer function is shown in Eq. 5.

$$\frac{V_{out}}{V_{in}} = \left(\frac{R_b}{K(R_a+R_b)}\right)\frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} - 1 \qquad \text{Eq. 5}$$

To build a boost circuit, use the design equations Eq. 6 and Eq. 7.

$$\frac{R_2C}{2} = \frac{Q}{\omega_o}, \quad 2C(R_a \| R_b) = \frac{1}{Q\omega_o} \qquad \text{Eq. 6,7}$$

Select R_2 and C using Eq. 6. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use Eq. 7 to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Eq. 8.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \qquad \text{Eq. 8}$$

Figure 10 shows an example of the response of the circuit of Figure 9, where f_o is 2.3MHz. The component values are as follows: R_a =2.1kΩ, R_b =68.5Ω, R_2 =4.22kΩ, R =500Ω, KR =50Ω, C =120pF.

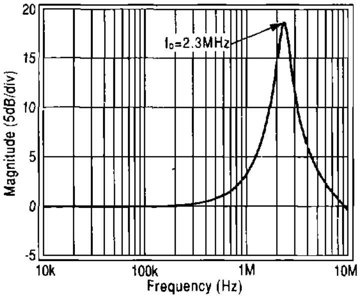


Figure 10