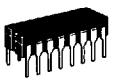
Dual D Type Master-Slave Flip-Flop

MC10H131

The MC10H131 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	–8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note)

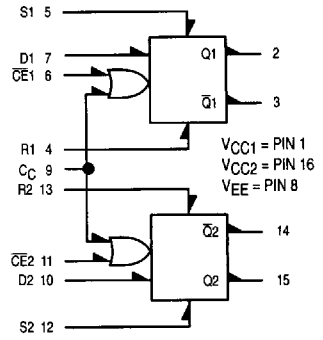
Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	62	—	56	—	62	mA
Input Current High Pins 6, 11 Pin 9 Pins 7, 10 Pins 4, 5, 12, 13	I_{inH}	 — — — —	 530 660 485 790	 — — — —	 310 390 285 465	 — — — —	 310 390 285 465	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
Low Output Voltage	V_{OL}	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
High Input Voltage	V_{IH}	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
Low Input Voltage	V_{IL}	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

Propagation Delay Clock, $\overline{CE}$ Set, Reset	t_{pd}	 0.8 0.6	 1.6 1.6	 0.8 0.7	 1.7 1.7	 0.8 0.7	 1.8 1.8	ns
Rise Time	t_r	0.6	2.0	0.6	2.0	0.6	2.2	ns
Fall Time	t_f	0.6	2.0	0.6	2.0	0.6	2.2	ns
Set–up Time	t_{set}	0.7	—	0.7	—	0.7	—	ns
Hold Time	t_{hold}	0.8	—	0.8	—	0.8	—	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

LOGIC DIAGRAM



RS TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

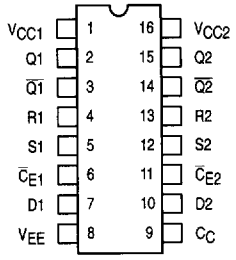
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

$C = \overline{CE} + C_C$

A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

APPLICATION INFORMATION

The MC10H131 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip–flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip–flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

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