SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1846/SG2846/SG3846
SG1847/SG2847/SG3847

CURRENT MODE PWM CONTROLLER

DESCRIPTION

The SG1846/1847 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadtime adjust capability, and a ±1% trimmed bandgap reference.

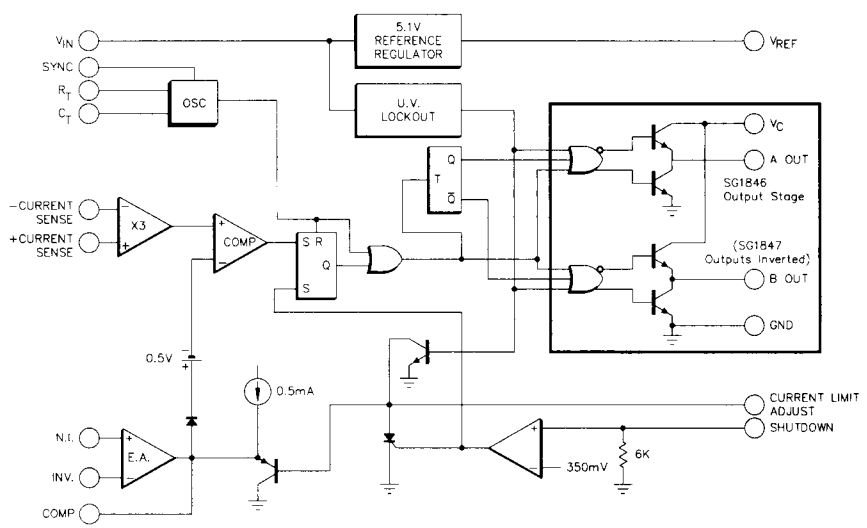
FEATURES

- **Automatic feed forward compensation**
- **Programmable pulse by pulse current limiting**
- **Automatic symmetry correction in push-pull configuration**
- **Enhanced load response characteristics**
- **Parallel operation capability for modular power systems**
- **Differential current sense amplifier with wide common mode range**
- **Double pulse suppression**
- **200mA totem-pole outputs**
- **± 1% bandgap reference**
- **Under-voltage lockout**
- **Soft-start capability**
- **Shutdown capability**
- **500KHz operation**

HIGH RELIABILITY FEATURES - SG1846/47

- **Available to MIL-STD - 883**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



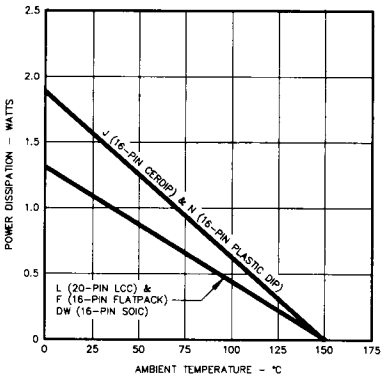
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1 and 2)

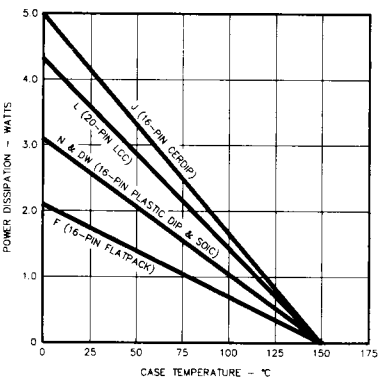
Supply Voltage ($+V_{IN}$) 40V
Collector Supply Voltage(V_C) 40V
Analog Inputs (Pins 3, 4, 5, 6, & 16) ..... -0.3V to $+V_{IN}$
Logic Input ..... -0.3V to 5.5V
Soure/Sink Load current (continuous) 200mA
Source/Sink Load Current (peak, 200ns) 500mA
Reference Load Current 30mA
Soft Start Sink Current 50mA
Sync Output Current 5mA
Error Amplifier Output Current 5mA
Oscillator Charging current (Pin 9) 5mA
Operating Junction Temperature
Hermetic (J, L, F Packages) ..... 150°C
Plastic (N, DW Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. Pin numbers refer to ceramic J package.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage Range ..... 8V to 40V
Collector Supply Voltage Range ..... 4.5V to 40V
Source/Sink Output Current (continuous) 100mA
Source/Sink Output Current (peak 200ns) 200mA
Reference Load Current ..... 0 to 10mA
Oscillator Frequency Range ..... 1KHz to 500KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 100KΩ
Oscillator Timing Capacitor (C_T) ..... 1000 pF to 0.1μF
Operating Ambient Temperature Range
SG1846/1847 ..... -55°C to 125°C
SG2846/2847 ..... -25°C to 85°C
SG3846/3847 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1846/SG1847 with $-55°C \le T_A \le 125°C$, SG2846/SG2847 with $-25°C \le T_A \le 85°C$, SG3846/SG3847 with $0°C \le T_A \le 70°C$, $+V_{IN} = 15V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1846/47 SG2846/47			SG3846/47			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	$T_J = 25°C$, $I_O = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8V to 40V		5	20		5	20	mV
Load Regulation	I_L = 1mA to 10mA		3	15		3	15	mV
Temperature Stability (Note 4)			0.4			0.4		mV/°C
Total Output Variation (Note 4)	Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage (Note 4)	10Hz ≤ f ≤ 10KHz. T_J = 25°C		100			100		μV
Long Term Stability (Note 4)	$T_J = 125°C$, 1000Hrs.		5			5		mV
Short Circuit Output Current	V_{REF} = 0V	-10	-45		-10	-45		mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1846/47 SG2846/47			SG3846/47			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 9)								
Initial Accuracy	T_J = 25°C	39	43	47	39	43	47	KHz
Voltage Stability	V_{IN} = 8V to 40V		1	2		1	2	%
Temperature Stability (Note 4)	**Over Operating Range**		1			1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8 = 0V	3.9			3.9			V
Sync Input Low Level	**Pin 8 = 0V**			2.5			2.5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V		1.2	1.5		1.2	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN} = 8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	**V_O = 1.2V to 3V, V_{CM} = 2V**	80	105		80	105		dB
Unity Gain Bandwidth (Note 4)	T_J = 25°C	0.7	1.0		0.7	1.0		MHz
CMRR	**V_{CM} = 0V to 38V, V_{IN} = 40V**	75	100		75	100		dB
PSRR	V_{IN} = 8V to 40V	80	105		80	105		dB
Output Sink Current	**V_{ID} = - 15mV to -5V, $V_{PIN\,7}$ = 1.2V**	2	6		2	6		mA
Output Source Current	V_{ID} = 15mV to 5V, $V_{PIN\,7}$ = 2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	**R_L = 15KΩ (Pin 7)**	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L = 15KΩ (Pin 7)		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain (Notes 5 & 6)	**$V_{PIN\,3}$ = 0V, Pin 1 Open**	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential (Note 6)	Pin 1 Open R_L = 15KΩ (Pin 7)							
Input Signal ($V_{PIN\,4}$ - $V_{PIN\,3}$)(Note 5)		1.1	1.2		1.1	1.2		V
Input Offset Voltage (Note 5)	$V_{PIN\,1}$ = 0.5V, Pin 7 Open		5	25		5	25	mV
CMRR	**V_{CM} = 1V to 12V**	60	83		60	83		dB
PSRR	V_{IN} = 8V to 40V	60	84		60	84		dB
Input Bias Current (Note 5)	**$V_{PIN\,1}$ = 0.5V, Pin 7 Open**		-2.5	-10		-2.5	-10	µA
Input Offset Current (Note 5)	$V_{PIN\,1}$ = 0.5V, Pin 7 Open		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs (Note 4)	T_J = 25°C		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset Voltage (Note 5)	**$V_{PIN\,3}$ = 0, $V_{PIN\,4}$ = 0V, Pin 7 Open**	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\,5}$ = V_{REF}, $V_{PIN\,6}$ = 0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\,1}$) (Note 7)		3.0	1.5		3.0	1.5		mA
Maximum Non-Latching Current ($I_{PIN\,1}$) (Note 8)			1.5	0.8		1.5	0.8	mA
Delay to Outputs (Note 4)	**T_J = 25°C**		300	600		300	600	ns
Output Section								
Collector Emitter Voltage		40			40			V
Collector Leakage Current	V_C = 40V			200			200	µA
Output Low Level	**I_{SINK} = 20mA**		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100mA		0.4	2.1		0.4	2.1	V
Output High Level	**I_{SOURCE} = 20mA**	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		V
Rise Time (Note 4)	**C_L = 1nF, T_J = 25°C**		50	300		50	300	ns
Fall Time (Note 4)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns

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ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1846/47 SG2846/47			SG3846/47			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

Note 4. These parameters although guaranteed over the recommended operating conditions, are not tested in production.

Note 5. Parameter measured at trip point of latch with $V_{PIN\,5} = V_{REF}$, $V_{PIN\,6} = 0V$.

Note 6. Amplifier gain defined as : $G = \frac{\Delta V_{PIN\,7}}{\Delta V_{PIN\,4}}$; $V_{PIN\,4} = 0V$ to $1.0V$

Note 7. Current into Pin 1 guaranteed to latch circuit in shutdown state.

Note 8. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

Note 9. $R_T = 10K\Omega$, $C_T = 4.7nF$

CHARACTERISTIC CURVES

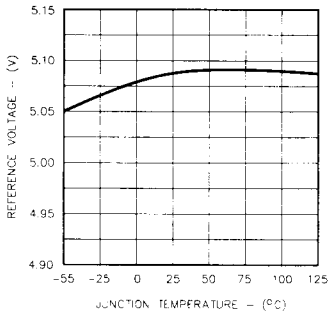


FIGURE 1.
REFERENCE VOLTAGE VS. TEMPERATURE

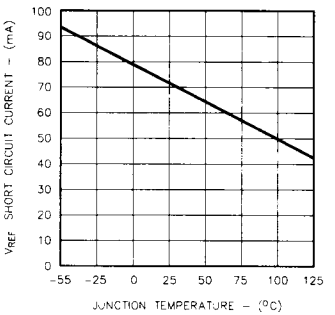


FIGURE 2.
V_{REF} SHORT CIRCUIT CURRENT VS. TEMPERATURE

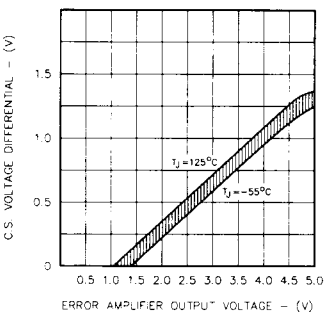


FIGURE 3.
CURRENT SENSE THRESHOLD
VS. ERROR AMPLIFIER OUTPUT

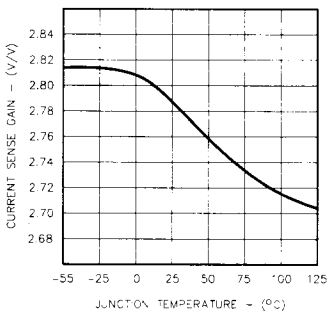


FIGURE 4.
CURRENT SENSE GAIN VS. TEMPERATURE

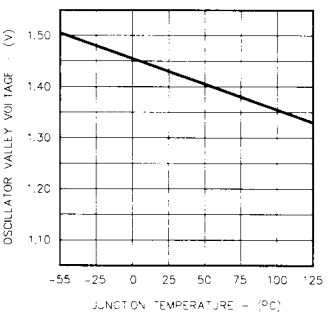


FIGURE 5.
OSCILLATOR VALLEY VOLTAGE VS. TEMPERATURE

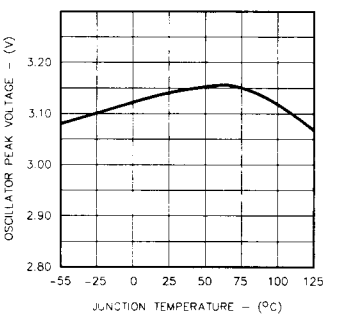


FIGURE 6.
OSCILLATOR PEAK VOLTAGE VS. TEMPERATURE

CHARACTERISTIC CURVES (continued)

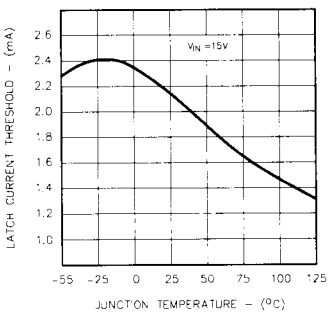


FIGURE 7.
MINIMUM SCR LATCH CURRENT

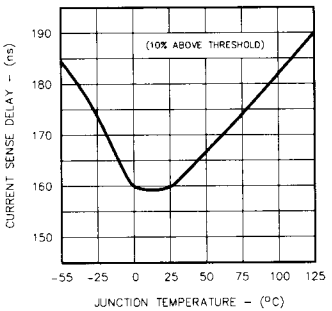


FIGURE 8.
CURRENT SENSE DELAY VS. TEMPERATURE

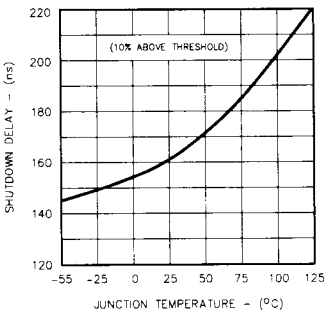


FIGURE 9.
SHUTDOWN DELAY TO OUTPUT VS. TEMPERATURE

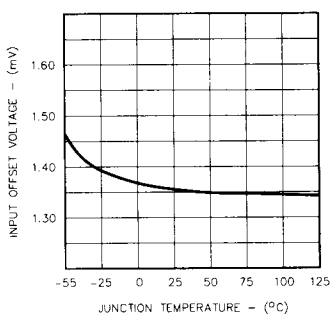


FIGURE 10.
ERROR AMPLIFIER INPUT OFFSET VOLTAGE
VS. TEMPERATURE

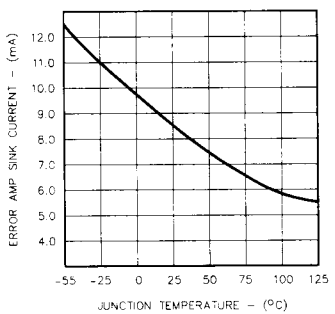


FIGURE 11.
ERROR AMP SINK CURRENT VS. TEMPERATURE

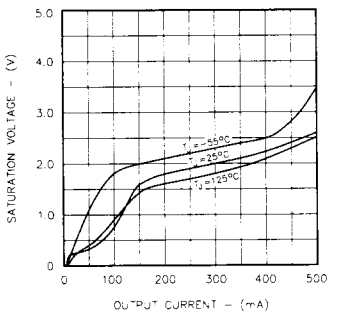


FIGURE 12.
OUTPUT TRANSISTOR SATURATION VOLTAGE
VS. OUTPUT CURRENT (SINK TRANSISTOR)

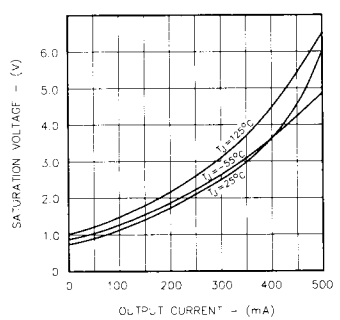


FIGURE 13.
OUTPUT TRANSISTOR SATURATION VOLTAGE
VS. OUTPUT CURRENT (SOURCE TRANSISTOR)

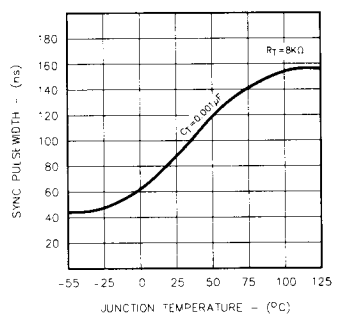


FIGURE 14.
SYNC PULSEWIDTH VS. TEMPERATURE

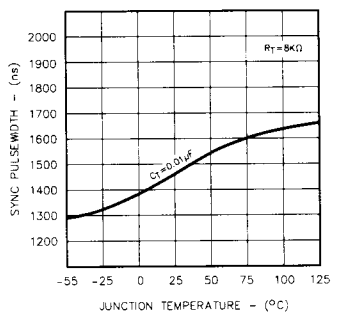


FIGURE 15.
SYNC PULSEWIDTH VS. TEMPERATURE

CHARACTERISTIC CURVES (continued)

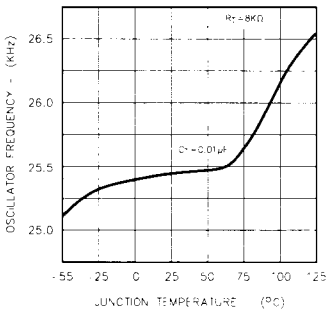


FIGURE 16.
OSCILLATOR FREQUENCY VS. TEMPERATURE

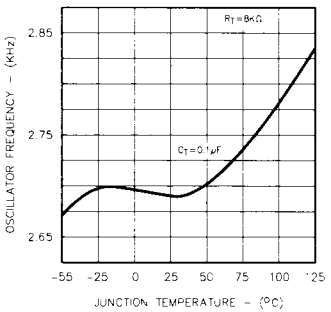


FIGURE 17.
OSCILLATOR FREQUENCY VS. TEMPERATURE

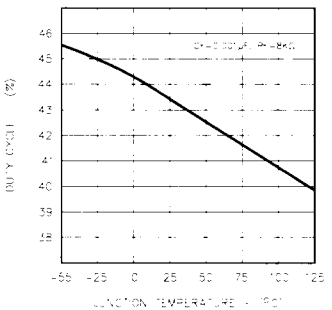


FIGURE 18.
DUTY CYCLE VS. TEMPERATURE

APPLICATION INFORMATION

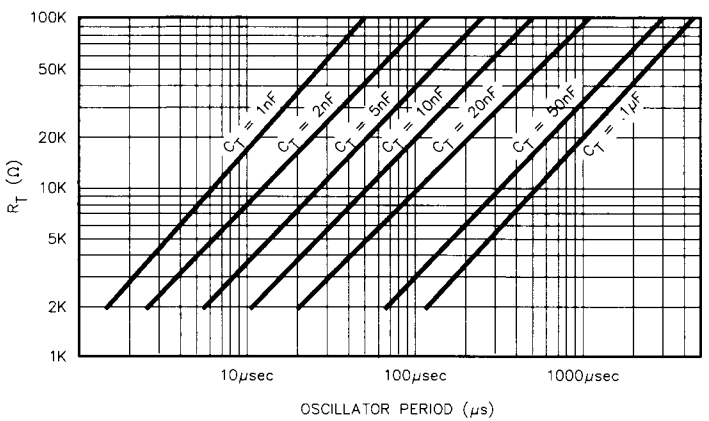
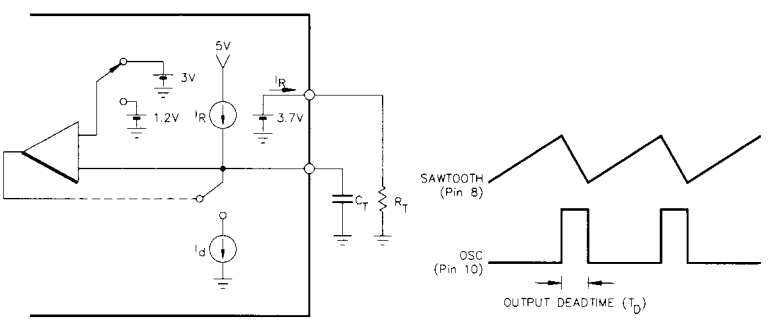


FIGURE 19- OSCILLATOR FREQUENCY CURVES



Oscillator frequency is approximated by the formula: $f_T \approx \frac{2.2}{R_T C_T}$

FIGURE 20 - OSCILLATOR CIRCUIT

APPLICATION INFORMATION (continued)

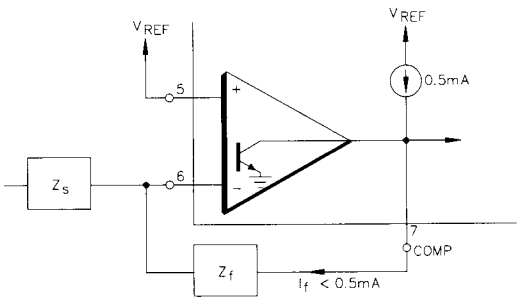


FIGURE 21 - ERROR AMP OUTPUT CONFIGURATION
(Error amplifier can source up to 0.5mA)

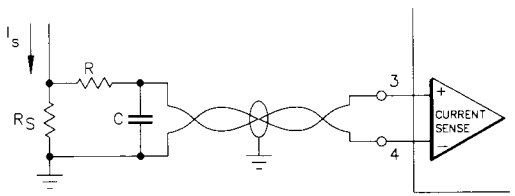


FIGURE 22 - CURRENT SENSE AMPCONNECTIONS

A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free switching.

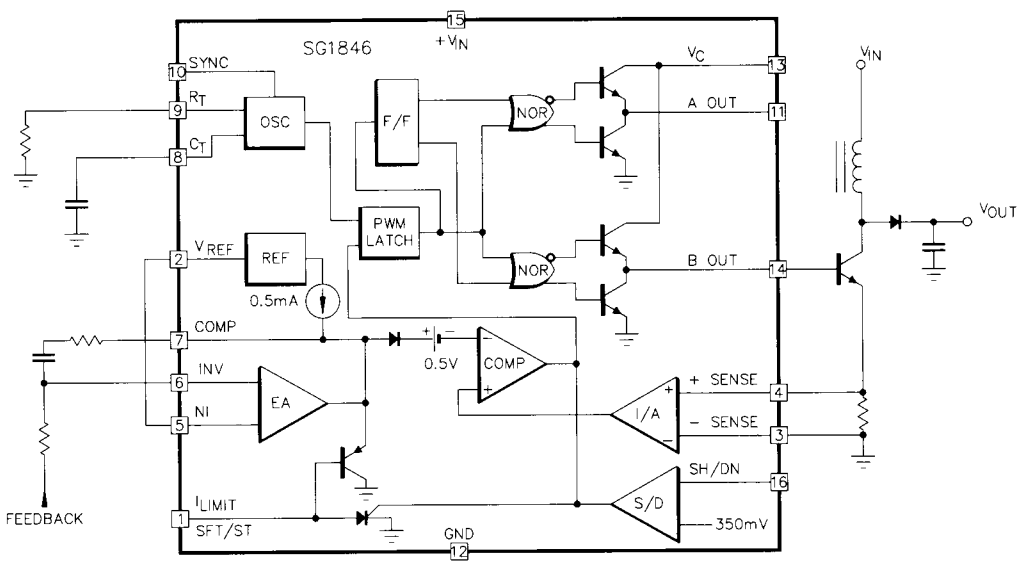


FIGURE 23 - SINGLE ENDED BOOST CONFIGURATION

APPLICATIONS INFORMATION (continued)

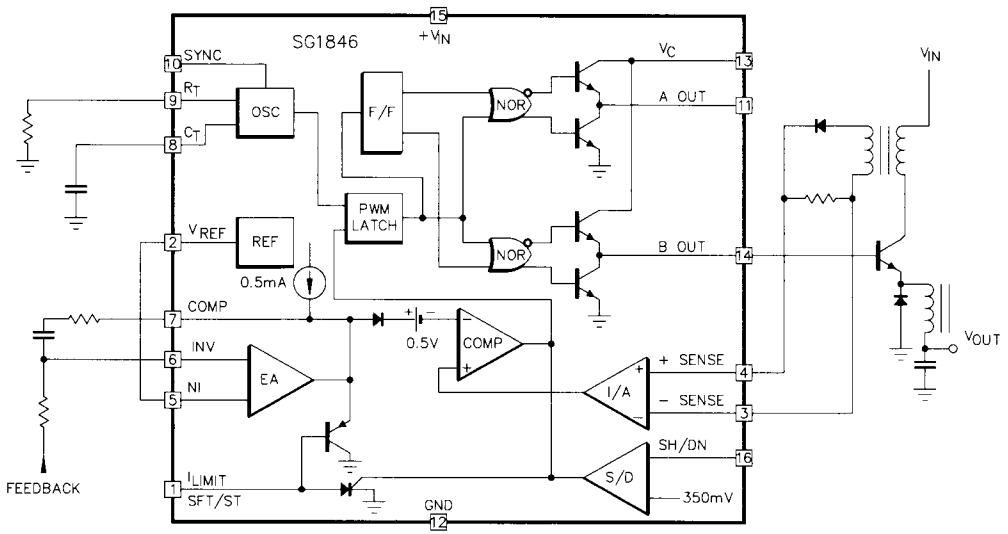


FIGURE 24 - BUCK CONVERTER WITH CURRENT SENSE WINDING

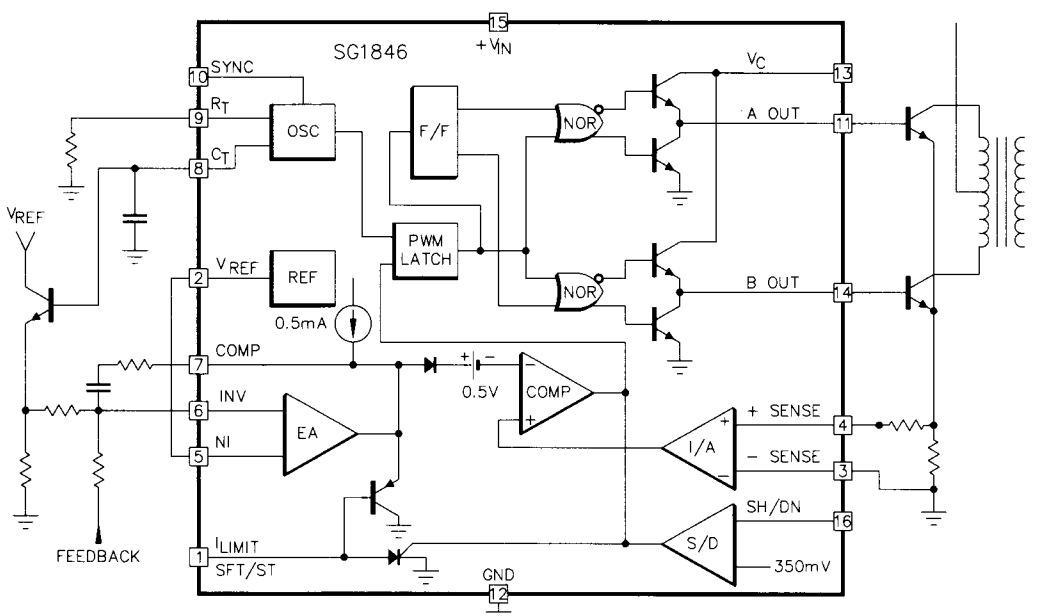
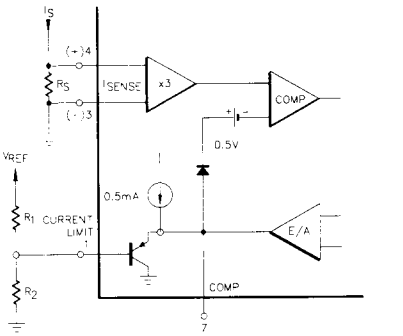


FIGURE 25 - PUSH/PULL CONVERTER WITH SLOPE COMPENSATION

APPLICATIONS INFORMATION (continued)



Peak Current (I_S) is determined by the formula: $I_S = \frac{\frac{R_2 V_{REF}}{R_1+R_2} - 0.5}{3R_S}$

FIGURE 26 - PULSE BY PULSE CURRENT LIMITING

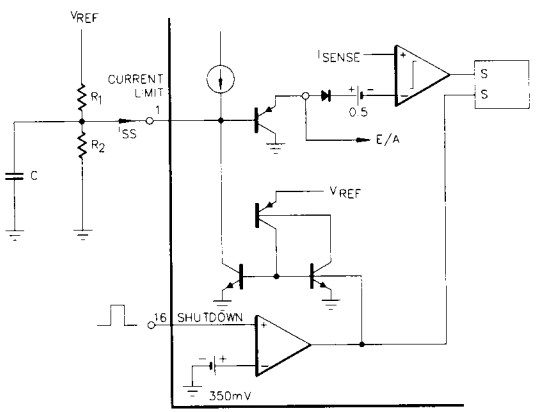
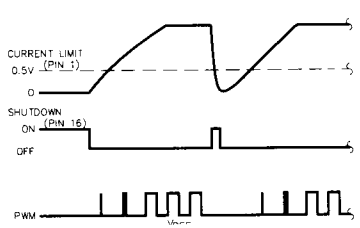
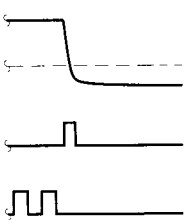


FIGURE 27 - SOFT START AND SHUTDOWN/RESTART FUNCTIONS



$\frac{V_{REF}}{R_1} < 0.8mA$

FIGURE 28 - SHUTDOWN WITH AUTO-RESTART



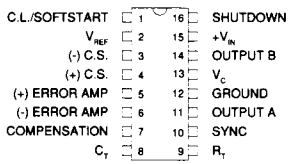
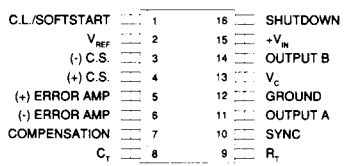
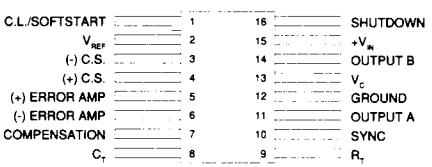
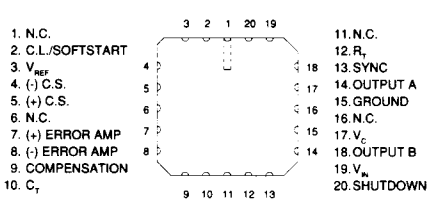
$\frac{V_{REF}}{R_1} > 3mA$ (LATCHED OFF)

FIGURE 29 - SHUTDOWN WITHOUT AUTO-RESTART (LATCHED)

If $\frac{V_{REF}}{R_1} < 0.8mA$ the shutdown latch will commutate when $I_{SS} < 0.8mA$ and a restart cycle will be initiated.

If $\frac{V_{REF}}{R_1} > 3mA$ the device will latch off until power is recycled.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1846J/883B SG1846J SG2846J SG3846J SG1847J/883B SG1847J SG2847J SG3847J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2846N SG3846N SG2847N SG3847N	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN WIDEBODY PLASTIC S.O.I.C DW - PACKAGE	SG2846DW SG3846DW SG2847DW SG3847DW	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE (Note 3)	SG1846F/883B SG1846F SG1847F/883B SG1847F	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L - PACKAGE (Note 3)	SG1846L/883B SG1846L SG1847L/883B SG1847L	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Notes: 1. Contact factory for JAN and DESC part availability.
2. All parts are viewed from the top.
3. Consult factory for product availability.