International IƆR Rectifier

IRK.71, .91 SERIES

THYRISTOR/ DIODE and
THYRISTOR/ THYRISTOR

NEW ADD-A-pak™ Power Modules

75 A
95 A

Features

■ Electrically isolated: DBC base plate
■ 3500 V_{RMS} isolating voltage
■ Standard JEDEC package
■ Simplified mechanical designs, rapid assembly
■ Auxiliary cathode terminals for wiring convenience
■ High surge capability
■ Wide choice of circuit configurations
■ Large creepage distances
■ UL E78996 approved ℝ

Description

These IRK series of NEW ADD-A-paks use power diodes and thyristors in a variety of circuit configurations. The semiconductor chips are electrically isolated from the base plate, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or AC controllers. These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, and temperature and motor speed control circuits.

Major Ratings and Characteristics

Parameters	IRK.71	IRK.91	Units
$I_{T(AV)}$ or $I_{F(AV)}$ @ 85°C	75	95	A
$I_{O(RMS)}$ (*)	165	210	A
I_{TSM} @ 50Hz	1665	1785	A
I_{FSM} @ 60Hz	1740	1870	A
I^2t @ 50Hz	13.86	15.91	KA^2s
@ 60Hz	12.56	14.52	KA^2s
$I^2\sqrt{t}$	138.6	159.1	$KA^2\sqrt{s}$
V_{RRM} range	400 to 1600		V
T_{STG}	- 40 to 125		°C
T_J	- 40 to 125		°C

(*) As AC switch.

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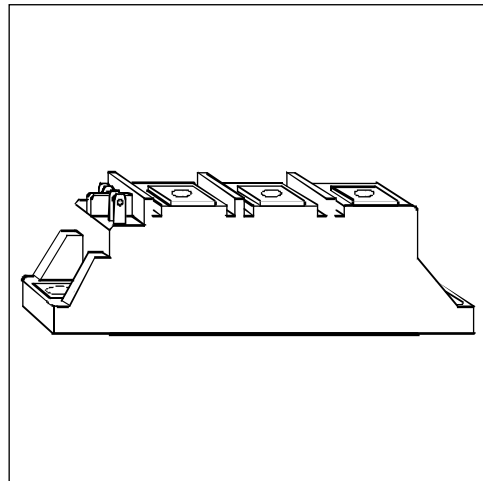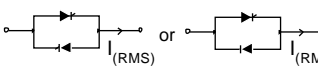
ELECTRICAL SPECIFICATIONS
Voltage Ratings

Type number	Voltage Code -	V_{RRM}, maximum repetitive peak reverse voltage V	V_{RSM}, maximum non-repetitive peak reverse voltage V	V_{DRM}, max. repetitive peak off-state voltage, gate open circuit V	I_{RRM} I_{DRM} 125°C mA
	04	400	500	400	
	06	600	700	600	
	08	800	900	800	
IRK.71/ .91	10	1000	1100	1000	15
	12	1200	1300	1200	
	14	1400	1500	1400	
	16	1600	1700	1600	

On-state Conduction

Parameters	IRK.71	IRK.91	Units	Conditions	
$I_{T(AV)}$ Max. average on-state current (Thyristors) $I_{F(AV)}$ Max. average forward current (Diodes)	75	95	A	180° conduction, half sine wave, $T_C = 85$°C	
$I_{O(RMS)}$ Max. continuous RMS on-state current. As AC switch	165	210			
I_{TSM} or I_{FSM} Max. peak, one cycle non-repetitive on-state or forward current	1665	1785		t=10ms No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max.
	1740	1870		t=8.3ms	
	1400	1500		t=10ms 100% V_{RRM}	
	1470	1570		t=8.3ms reapplied	
	1850	2000		t=10ms $T_J = 25$°C,	
	1940	2100		t=8.3ms no voltage reapplied	
I^2t Max. I^2t for fusing	13.86	15.91	KA²s	t=10ms No voltage reapplied	Initial $T_J = T_J$ max.
	12.56	14.52		t=8.3ms	
	9.80	11.25		t=10ms 100% V_{RRM}	
	8.96	10.27		t=8.3ms reapplied	
	17.11	20.00		t=10ms $T_J = 25$°C,	
	15.60	18.30		t=8.3ms no voltage reapplied	
$I^2\sqrt{t}$ Max. $I^2\sqrt{t}$ for fusing (1)	138.6	159.1	KA²√s	t=0.1 to 10ms, no voltage reapplied	
$V_{T(TO)}$ Max. value of threshold voltage (2)	0.82	0.80	V	Low level (3)	$T_J = T_J$ max
	0.85	0.85		High level (4)	
r_t Max. value of on-state slope resistance (2)	3.00	2.40	mΩ	Low level (3)	$T_J = T_J$ max
	2.90	2.25		High level (4)	
V_{TM} V_{FM} Max. peak on-state or forward voltage	1.59	1.58	V	$I_{TM} = \pi \times I_{T(AV)}$ $I_{FM} = \pi \times I_{F(AV)}$	$T_J = 25$°C
di/dt Max. non-repetitive rate of rise of turned on current	150		A/µs	$T_J = 25$°C, from 0.67 V_{DRM}, $I_{TM} = \pi \times I_{T(AV)}$, $I_g = 500$mA, $t_r < 0.5$ µs, $t_p > 6$ µs	
I_H Max. holding current	200		mA	$T_J = 25$°C, anode supply = 6V, resistive load, gate open circuit	
I_L Max. latching current	400			$T_J = 25$°C, anode supply = 6V, resistive load	

(1) I^2t for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$　　(2) Average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$　　(3) 16.7% x π x $I_{AV} < I < \pi$ x I_{AV}
(4) $I > \pi$ x I_{AV}

Triggering

	Parameters	IRK.71	IRK.91	Units	Conditions	
P_{GM}	Max. peak gate power	12	12	W		
$P_{G(AV)}$	Max. average gate power	3.0	3.0			
I_{GM}	Max. peak gate current	3.0	3.0	A		
$-V_{GM}$	Max. peak negative gate voltage	10		V		
V_{GT}	Max. gate voltage required to trigger	4.0		V	$T_J = -40°C$	Anode supply = 6V resistive load
		2.5			$T_J = 25°C$	
		1.7			$T_J = 125°C$	
I_{GT}	Max. gate current required to trigger	270		mA	$T_J = -40°C$	Anode supply = 6V resistive load
		150			$T_J = 25°C$	
		80			$T_J = 125°C$	
V_{GD}	Max. gate voltage that will not trigger	0.25		V	$T_J = 125°C$, rated V_{DRM} applied	
I_{GD}	Max. gate current that will not trigger	6		mA	$T_J = 125°C$, rated V_{DRM} applied	

Blocking

	Parameters	IRK.71	IRK.91	Units	Conditions
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	15		mA	$T_J = 125 °C$, gate open circuit
V_{INS}	RMS isolation voltage	2500 (1 min) 3500 (1 sec)		V	50 Hz, circuit to base, all terminals shorted
dv/dt	Max. critical rate of rise of off-state voltage (5)	500		V/µs	$T_J = 125°C$, linear to 0.67 V_{DRM}, gate open circuit

(5) Available with dv/dt = 1000V/µs, to complete code add S90 i.e. IRKT91/16 S90.

Thermal and Mechanical Specifications

|	Parameters	IRK.71	IRK.91	Units	Conditions
T_J	Junction operating temperature range	- 40 to 125		°C	
T_{stg}	Storage temp. range	- 40 to 125			
R_{thJC}	Max. internal thermal resistance, junction to case	0.165	0.135	K/W	Per module, DC operation
R_{thCS}	Typical thermal resistance case to heatsink	0.1			Mounting surface flat, smooth and greased. Flatness < 0.03 mm; roughness < 0.02 mm
T	Mounting torque ± 10% to heatsink	5		Nm	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound
	busbar	3			
wt	Approximate weight	83 (3)		g (oz)	
	Case style	TO-240AA			JEDEC

ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Devices	Sine half wave conduction					Rect. wave conduction					Units
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
IRK.71	0.06	0.07	0.09	0.12	0.18	0.04	0.08	0.10	0.13	0.18	°C/W
IRK.91	0.04	0.05	0.06	0.08	0.12	0.03	0.05	0.06	0.08	0.12	

Outlines Table
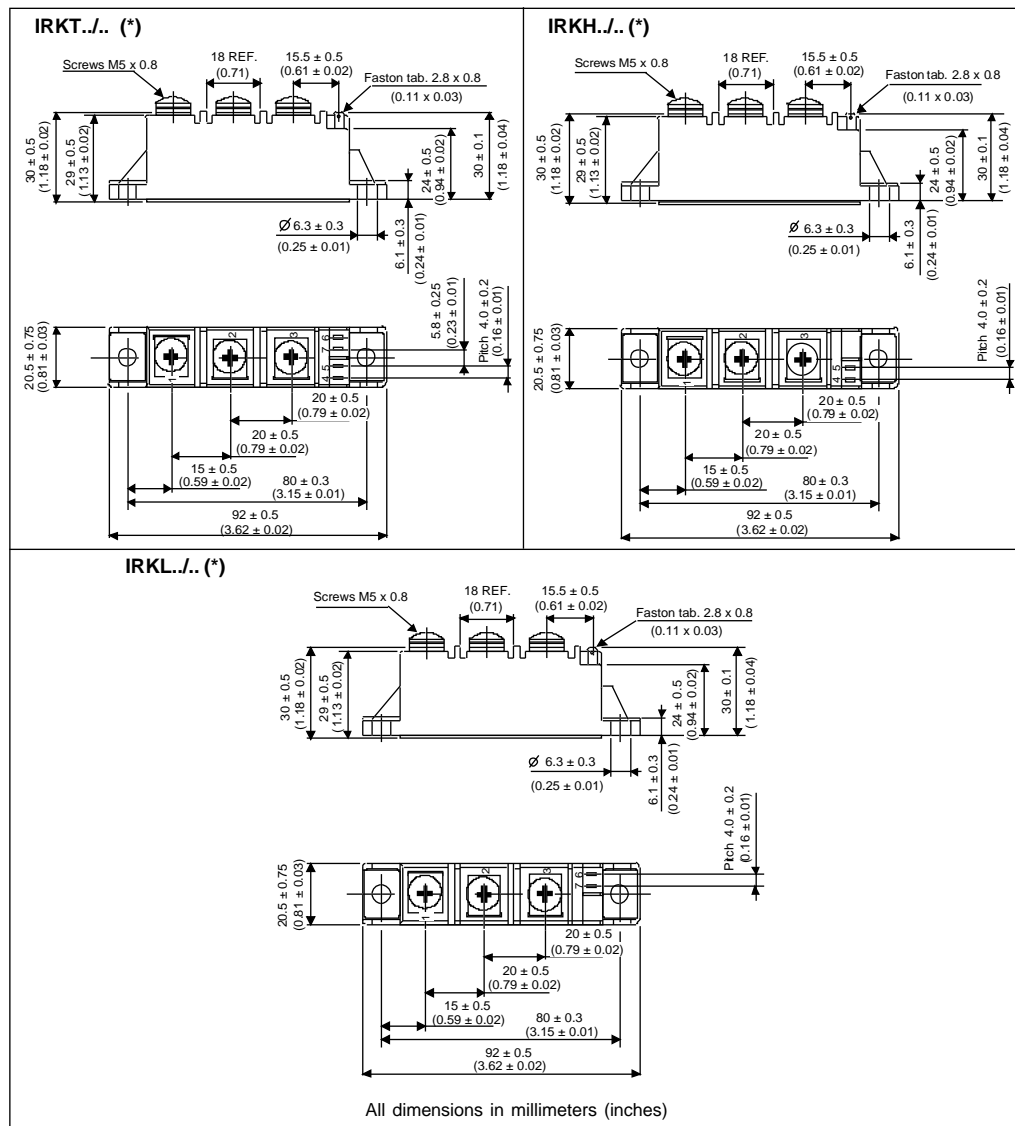
(*) For terminals connections, see Circuit configurations Table

NOTE: To order the Optional Hardware see Bulletin I27900

Circuit Configurations Table

IRKT	IRKH	IRKL

IRKT
(1) ○ ~
(2) ○ +
(3) ○ -
G1 K1 K2 G2
(4) (5) (7) (6)

IRKH
(1) ○ ~
(2) ○ +
(3) ○ -
G1 K1
(4) (5)

IRKL
(1) ○ ~
(2) ○ +
(3) ○ -
K2 G2
(7) (6)
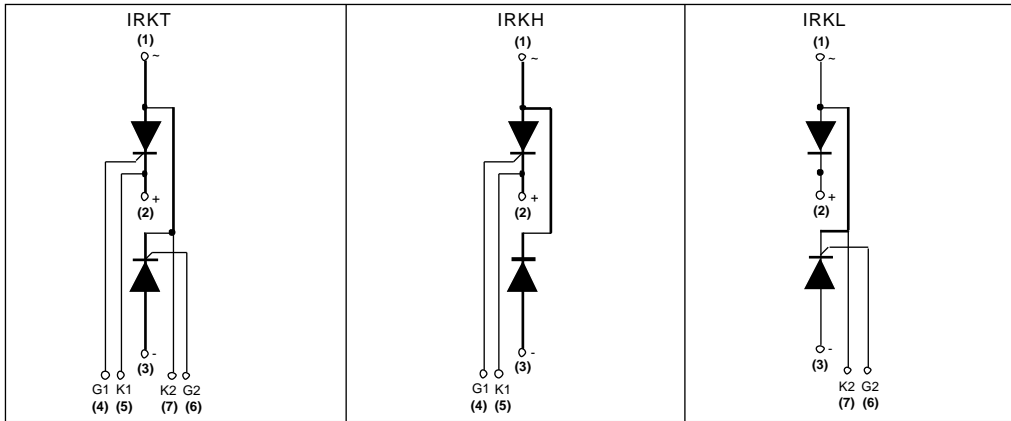
Ordering Information Table

Device Code

IRK	T	91	/	16	S90
①	②	③		④	⑤

1 - Module type
2 - Circuit configuration (See Circuit Configuration table)
3 - Current code * *
4 - Voltage code (See Voltage Ratings table)
5 - dv/dt code: S90 = dv/dt 1000 V/µs
No letter = dv/dt 500 Vµs

IRK.92 types
With no auxiliary cathode

13.8 (0.53)

* * Available with no auxiliary cathode.
To specify change: 71 to 72
91 to 92
e.g. : IRKT92/16 etc.
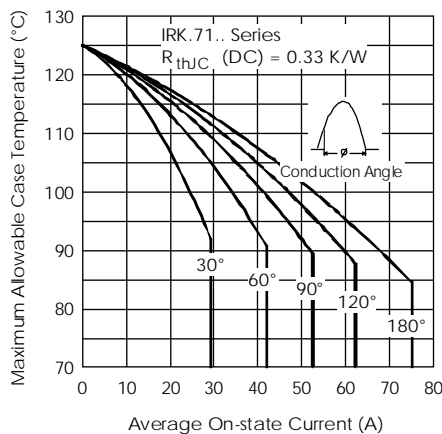
Fig. 1 - Current Ratings Characteristics

IRK.71.. Series
R_{thJC} (DC) = 0.33 K/W
Conduction Angle
30° 60° 90° 120° 180°

Fig. 2 - Current Ratings Characteristics

IRK.71.. Series
R_{thJC} (DC) = 0.33 K/W
Conduction Period
30° 60° 90° 120° 180° DC
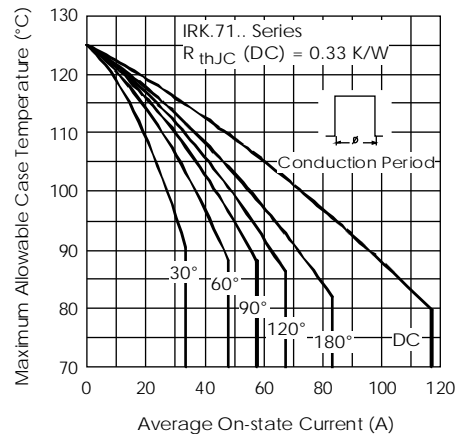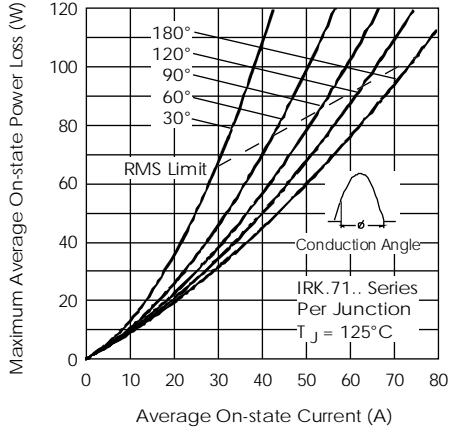
Fig. 3 - On-state Power Loss Characteristics
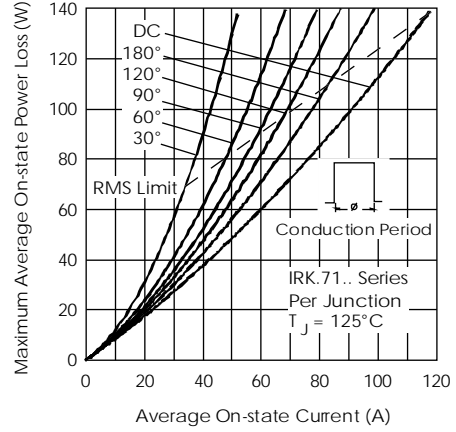
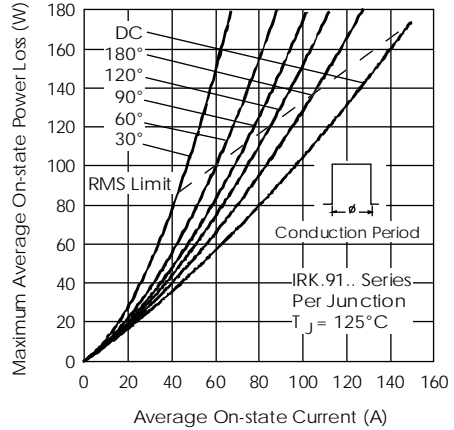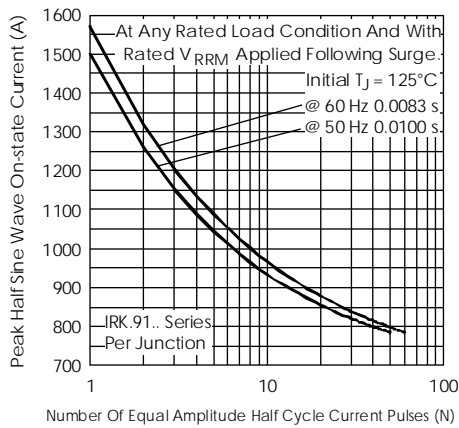
Fig. 4 - On-state Power Loss Characteristics
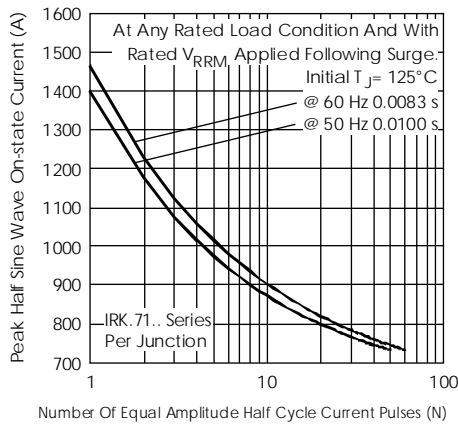
Fig. 5 - Maximum Non-Repetitive Surge Current
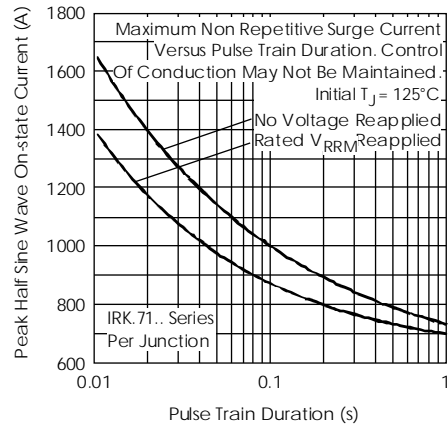
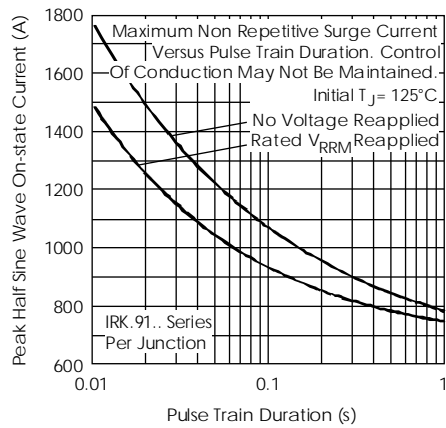Fig. 6 - Maximum Non-Repetitive Surge Current
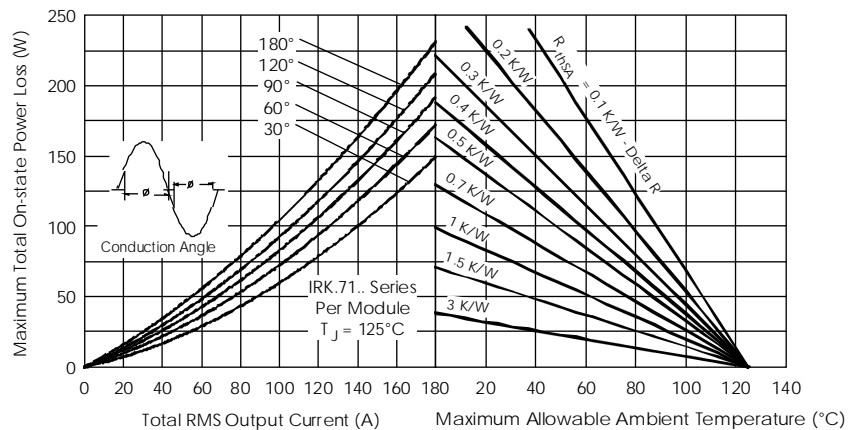
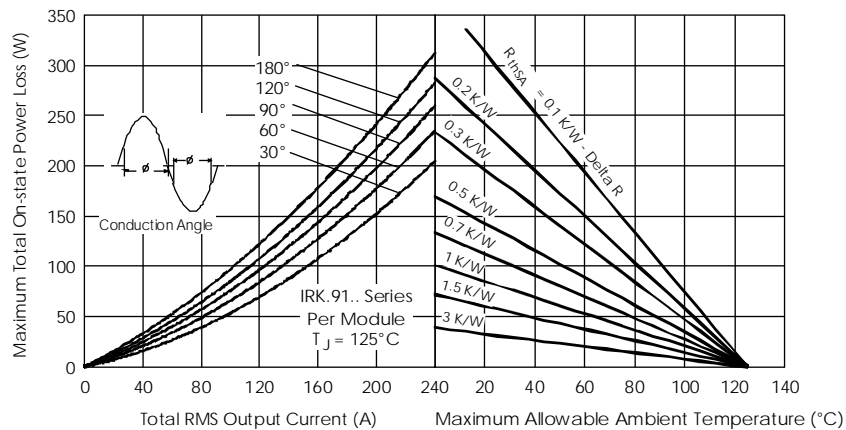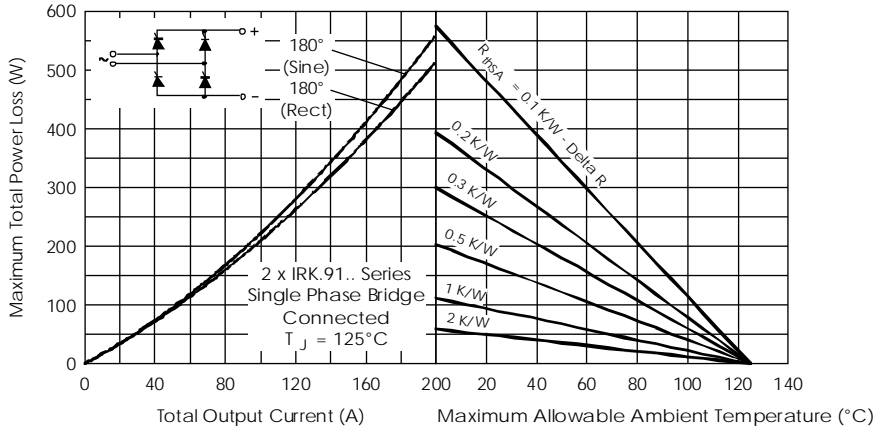Fig. 7 - On-state Power Loss Characteristics

IRK.71, .91 Series
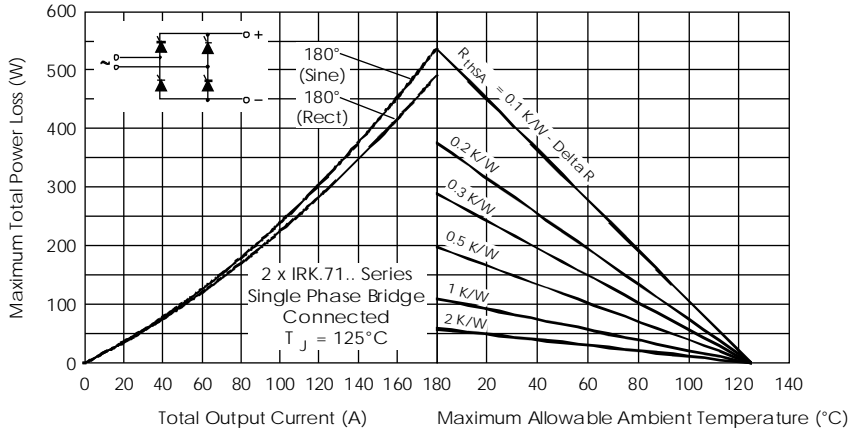
Fig. 8 - On-state Power Loss Characteristics
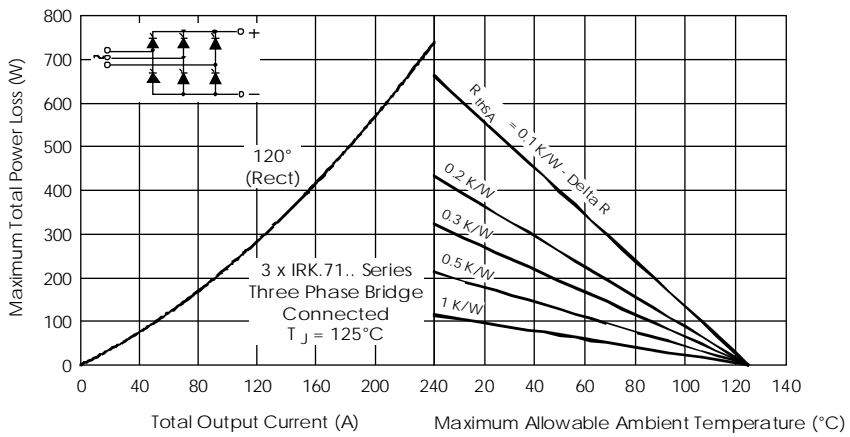
Fig. 9 - On-state Power Loss Characteristics
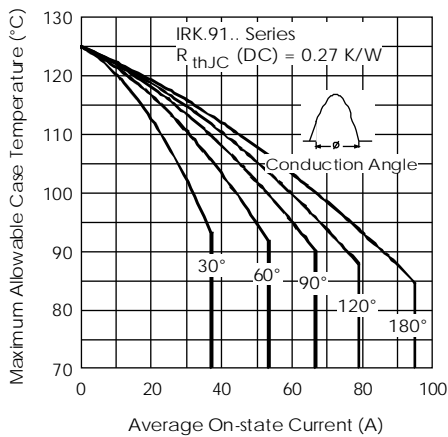
Fig. 10 - Current Ratings Characteristics
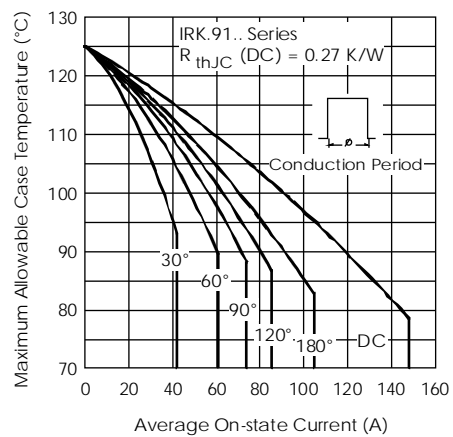
Fig. 11 - Current Ratings Characteristics
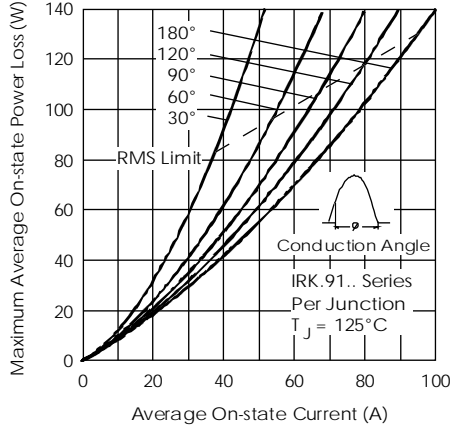
Fig. 12 - On-state Power Loss Characteristics

Fig. 13 - On-state Power Loss Characteristics

Fig. 14 - Maximum Non-Repetitive Surge Current

Fig. 15 - Maximum Non-Repetitive Surge Current

Fig. 16 - On-state Power Loss Characteristics

Fig. 17 - On-state Power Loss Characteristics
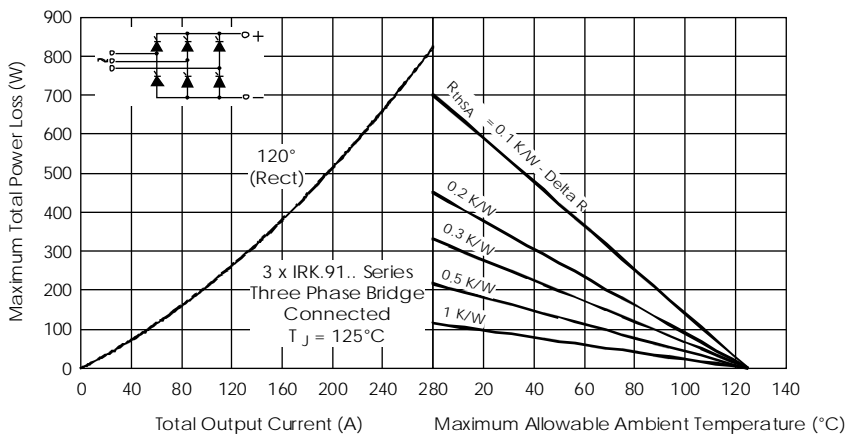
Fig. 18 - On-state Power Loss Characteristics
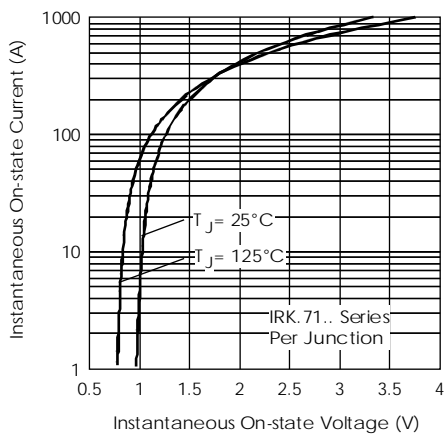
Fig. 19 - On-state Voltage Drop Characteristics

Fig. 20 - On-state Voltage Drop Characteristics
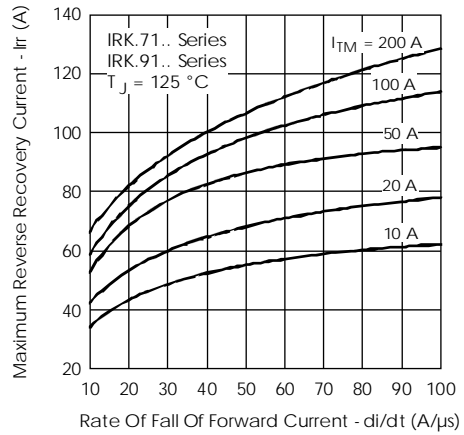
Fig. 21 - Recovery Charge Characteristics
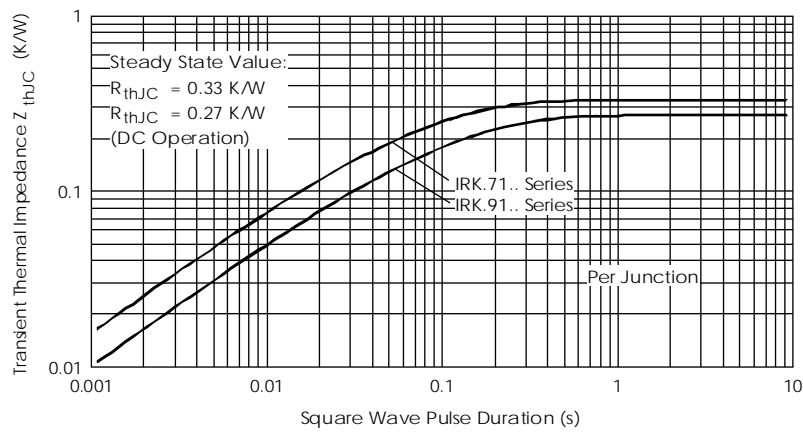
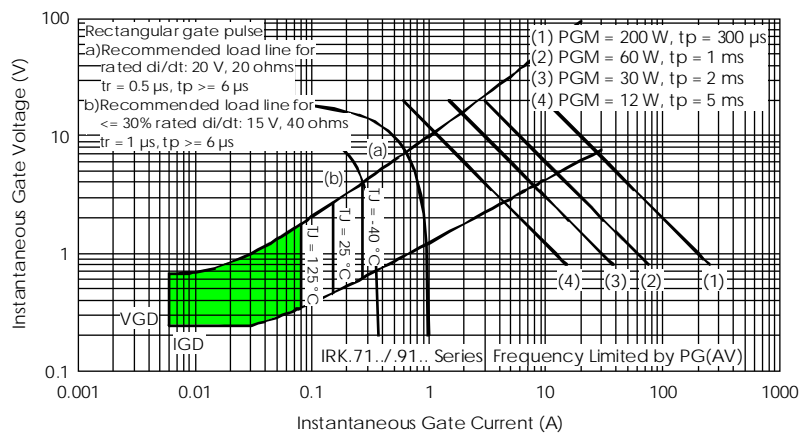Fig. 22 - Recovery Current Characteristics

Fig. 23 - Thermal Impedance Z_{thJC} Characteristics

Fig. 24 - Gate Characteristics