Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFR9130S.5

DESIGNER'S DATA SHEET

RADIATION TOLERANT
26 AMP, 100 Volts, 90 mΩ
Avalanche Rated P-MOSFET

Part Number / Ordering Information [1/]

SFR9130 S.5

Screening [2/]
- __ = Not Screened
- TX = TX Level
- TXV = TXV Level
- S = S Level

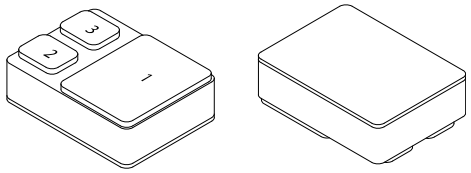
Package [3/]
- S.5 = SMD.5

Features:
- Rugged Trench Technology
- Low ON-resistance: 57mΩ typ
- Radiation tolerant: less than 0.5V typical gate threshold shift @ TID= 100kRAD
- SEU and SEGR resistant to LET 38
- Avalanche rated
- Hermetically Sealed Power Packaging
- Low Total Gate Charge, Fast Switching
- Replacement for IRF9130 types
- TX, TXV, S-Level screening available

Maximum Ratings		Symbol	Value	Units
Drain – Source Voltage		V_{DSS}	-100	V
Gate – Source Voltage, continuous Gate – Source Voltage, transient		V_{GS}	±15 ±25	V
Max. Continuous Drain Current (package limited)	@ T_C = 25ºC @ T_C = 100ºC	I_{D1} I_{D2}	26 17	A
Max. Avalanche current	@ L= 5.0 mH	I_{AR}	26	A
Max. Continuous Drain Current (Tj limited)	@ Tj= 150 ºC	I_{DM}	27	A
Single Pulse Avalanche Energy	@ L= 5.0 mH	E_{AS}	300	mJ
Total Power Dissipation	@ T_C = 25ºC	P_D	83	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	ºC
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.5 (typ 0.5)	ºC/W

NOTES:
*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @25°C.

SMD.5 (S.5)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	**DATA SHEET #: FT0045B**	**DOC**

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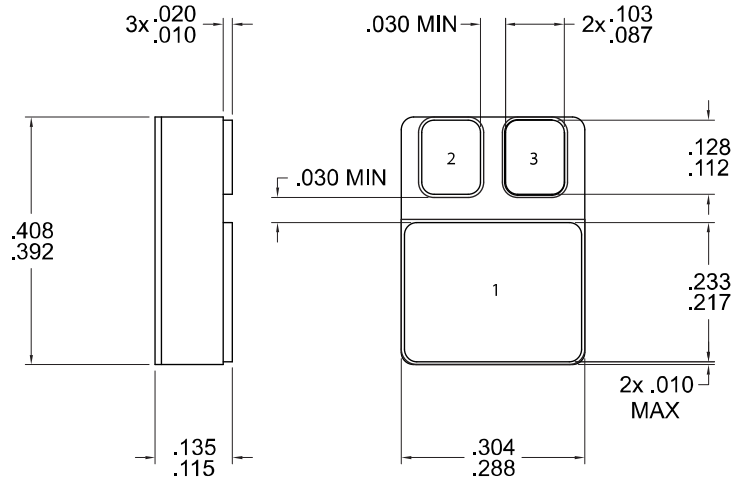
SFR9130S.5

Electrical Characteristics [3/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D =0.25 mA	BV_{DSS}	-100	-115	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 13A, Tj= 25°C V_{GS} = 10V, I_D = 13A, Tj= 125°C	$R_{DS(on)}$	— —	57 100	90 —	mΩ
Gate Threshold Voltage	V_{DS} = 5 V, I_D = 250μA, Tj= 25°C V_{DS} = 5 V, I_D = 250μA, Tj= 125°C V_{DS} = 5 V, I_D = 250μA, Tj= -55°C	$V_{GS(th)}$	-2.0 -1.0 —	-3.2 -2.5 -3.6	-4.0 — -5.0	V
Gate to Source Leakage	V_{GS} = ±15V, Tj= 25°C V_{GS} = ±15V, Tj= 125°C	I_{GSS}	—	1 10	±50 ±200	nA
Zero Gate Voltage Drain Current	V_{DS} = -100V, V_{GS} = 0V, T_j = 25°C V_{DS} = -100V, V_{GS} = 0V, T_j = 125°C	I_{DSS}	— —	0.01 5	10 250	μA μA
Forward Transconductance	V_{DS} = 10V, I_D = 10A, T_j = 25°C	g_{fs}	—	15	—	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10V V_{DS} = 80V I_D = 10A	Q_g Q_{gs} Q_{gd}	— — —	23 8.5 5	40 — —	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 10V V_{DS} = 50V I_D = 10A R_G = 10Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	65 25 75 30	100 50 150 50	nsec
Diode Forward Voltage	I_F = 10A, V_{GS} = 0V	V_{SD}	—	0.85	1.5	V
Diode Reverse Recovery Time **Peak Reverse Recovery Current** **Reverse Recovery Charge**	I_F = 10A, di/dt = 100A/usec	t_{rr} Q_{rr}	— —	60 150	85 —	nsec nC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	3500 300 110	4000 400 200	pF

PACKAGE OUTLINE:
SMD.5
PINOUT:
PIN 1: DRAIN
PIN 2: SOURCE
PIN 3: GATE



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