TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS054A – Revised March 2002

CD4069UB Types

CMOS Hex Inverter

High-Voltage Types (20-Volt Rating)

■ CD4069UB types consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

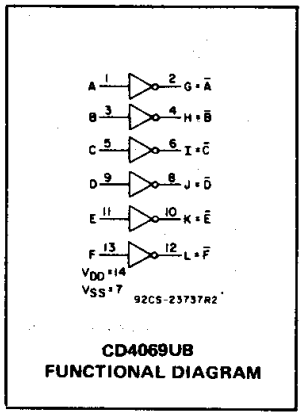
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation—t_{PHL}, t_{PLH}=30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative **Standard No. 13B,** "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



CD4069UB
FUNCTIONAL DIAGRAM

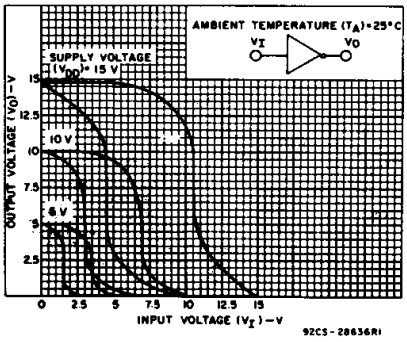


Fig. 1 – Minimum and maximum voltage transfer characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

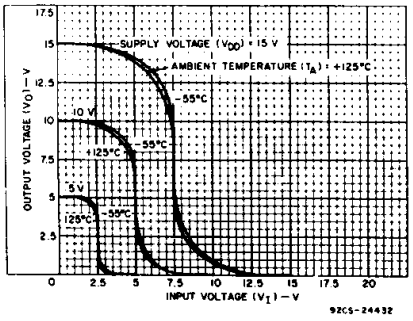


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	10	15	pF

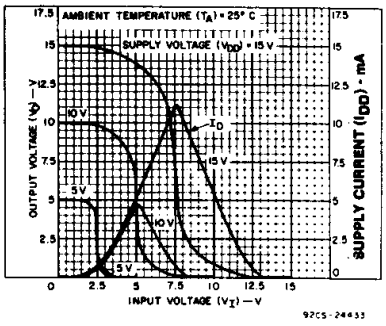


Fig. 3 – Typical current and voltage transfer characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				–	—	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

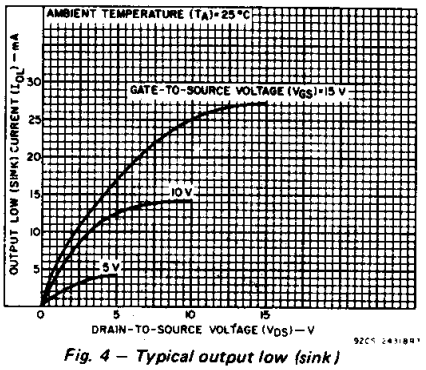


Fig. 4 – Typical output low (sink) current characteristics.

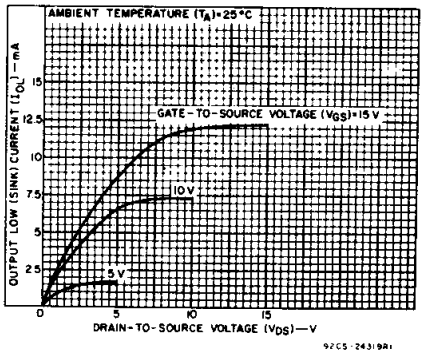


Fig. 5 – Minimum output low (sink) current characteristics.

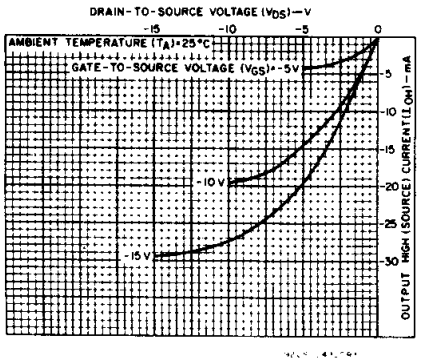


Fig. 8 – Typical output high (source) current characteristics.

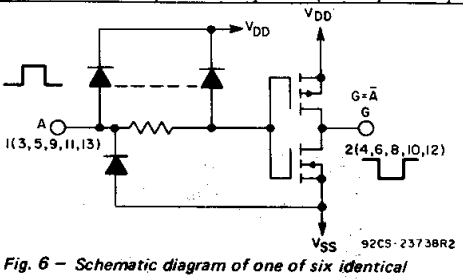


Fig. 6 – Schematic diagram of one of six identical inverters.

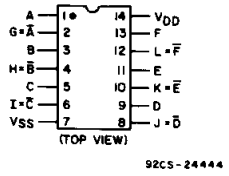


Fig. 7 – CD4069UB terminal assignment.

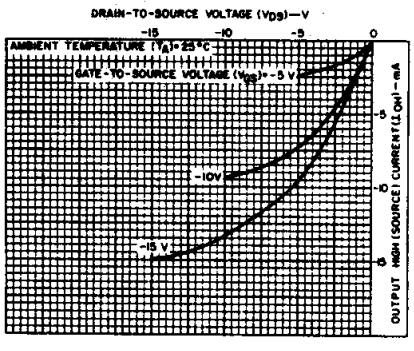


Fig. 9 – Minimum output high (source) current characteristics.

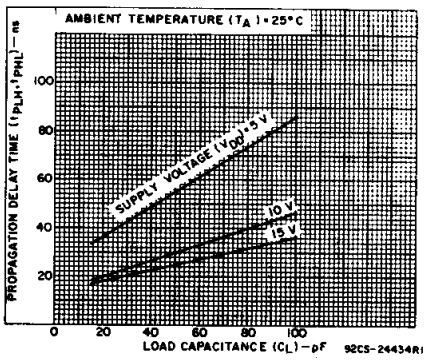


Fig. 10 – Typical propagation delay time vs. load capacitance.

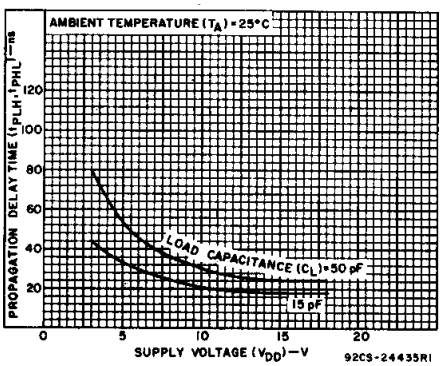


Fig. 11 – Typical propagation delay time vs. supply voltage.

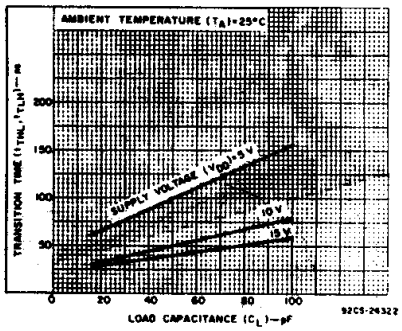


Fig. 12 – Typical transition time vs. load capacitance.

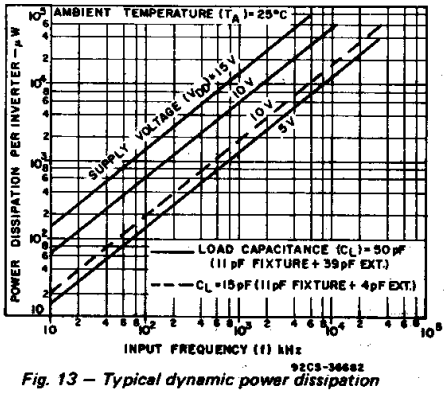


Fig. 13 – Typical dynamic power dissipation vs. frequency.

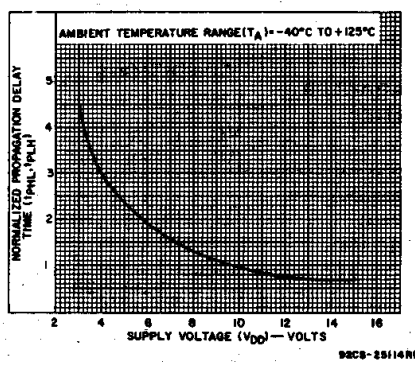


Fig. 14 – Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

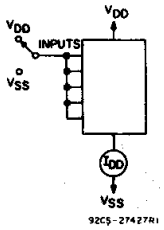


Fig. 15 – Quiescent device current test circuit.

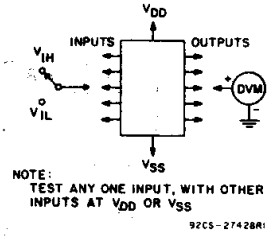


Fig. 16 – Noise immunity test circuit.

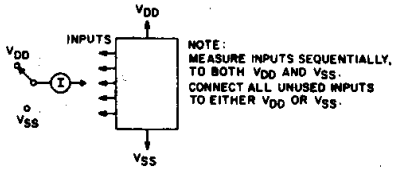
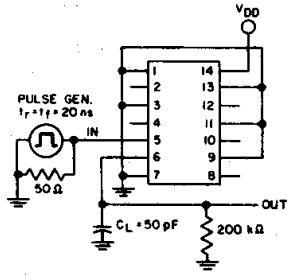


Fig. 17 – Input leakage current test circuit.



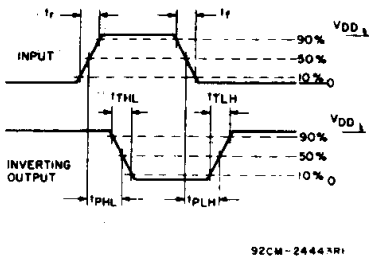


Fig. 18 – Dynamic electrical characteristics test circuit and waveforms.

APPLICATIONS

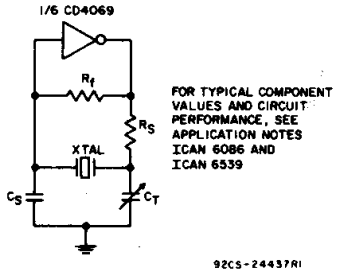


Fig. 19 – Typical crystal oscillator circuit.

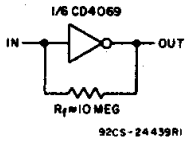


Fig. 20 – High-input impedance amplifier.

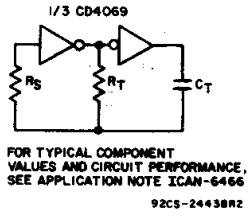


Fig. 21 – Typical RC oscillator circuit.

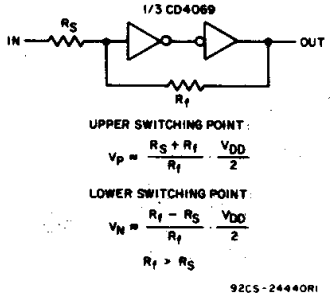


Fig. 22 – Input pulse shaping circuit (Schmitt trigger).

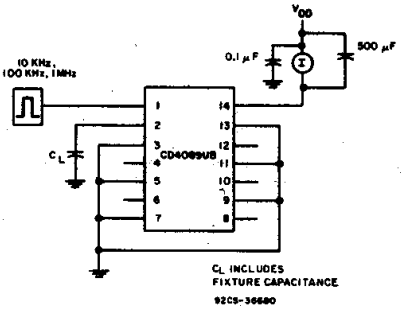
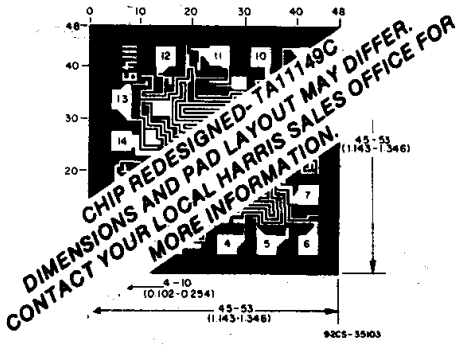


Fig. 23 – Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4069UBH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | SAMPLES | APPLICATION NOTES | USER GUIDES | MORE LITERATURE

PRODUCT SUPPORT: TRAINING

CD4069UB, CMOS Hex Inverter

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD4069UB
Voltage Nodes (V)	5, 10, 15

FEATURES

Back to Top

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- Medium Speed Operation–t_{PHL}, t_{PLH}=30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
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- Applications:
  - Logic inversion
  - Pulse shaping
  - Oscillators
  - High-input-impedance amplifiers

DESCRIPTION

Back to Top

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TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: cd4069ub.pdf (216 KB,Rev.A) (Updated: 03/15/2002)

APPLICATION NOTES

Back to Top

View Application Notes for Digital Logic

- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics (SCHA004 - Updated: 12/03/2001)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

Back to Top

- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)

Product Folder: CD4069UB, CMOS Hex Inverter

- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

Back to Top

- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)
- Signal Switch Data Book (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

Back to Top

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	DSCC NUMBER	PRODUCT CONTENT	SAMPLES
CD4069UBE	PDIP (N)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4069UBM	SOIC (D)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4069UBNSR	SOP (NS)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4069UBPWR	TSSOP (PW)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

Back to Top

DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
CD4069UBE	ACTIVE	PDIP (N) | 14	-55 TO 125		View Contents	1KU | 0.08	25
CD4069UBF	ACTIVE	CDIP (J) | 14	-55 TO 125		View Contents	1KU | 2.06	1
CD4069UBF3A	ACTIVE	CDIP (J) | 14	-55 TO 125		View Contents	1KU | 2.42	1
CD4069UBM	ACTIVE	SOIC (D) | 14	-55 TO 125		View Contents	1KU | 0.08	50

TI INVENTORY STATUS
As Of 08:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
>10k*	>10k | 16 Apr	4 WKS
2691*	196 | 05 May	8 WKS
	>10k | 20 May	
3172*	>10k | 20 May	8 WKS
8000*	207 | 21 Apr	4 WKS
	>10k | 12 May	

REPORTED DISTRIBUTOR INVENTORY
As Of 08:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
Avnet | Americas	>1k	BUY NOW
EBV Electronik | Europe	>1k	BUY NOW
DigiKey | Americas	>1k	BUY NOW
Newark Electronics | Americas	910	BUY NOW
Insight | Americas	200	BUY NOW
Avnet-SILICA | Europe	24	BUY NOW
Avnet | Americas	905	BUY NOW
Avnet | Americas	208	BUY NOW
Avnet-SILICA | Europe	15	BUY NOW
EBV Electronik | Europe	4	BUY NOW
Avnet | Americas	>1k	BUY NOW

Product Folder: CD4069UB, CMOS Hex Inverter

											DigiKey | Americas	>1k	BUY NOW
											Avnet-SILICA | Europe	>1k	BUY NOW
CD4069UBM96	ACTIVE	SOIC (D)	14	-55 TO 125		View Contents	1KU | 0.08	2500	0*	>10k | 16 Apr	2 WKS	Newark Electronics | Americas	23	BUY NOW
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CD4069UBPW	ACTIVE	TSSOP (PW)	14	-55 TO 125		View Contents	1KU | 0.17	90	0*	540 | 16 Apr	4 WKS	DigiKey | Americas	>1k	BUY NOW
										>10k | 08 May		None Reported View Distributors		
CD4069UBPWR	ACTIVE	TSSOP (PW)	14	-55 TO 125		View Contents	1KU | 0.08	2000	0*	>10k | 16 Apr	2 WKS			
JM38510/17401BCA	ACTIVE	CDIP (J)	14	-55 TO 125		View Contents	1KU | 15.66	1	442*	547 | 05 May	8 WKS	DigiKey | Americas	822	BUY NOW
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